

HD74LV221A

Dual Monostable Multivibrators

REJ03D0326-0600Z
(Previous ADE-205-271D (Z))
Rev.6.00
Jun. 23, 2004

Description

The HD74LV221A features output pulse-duration control by three methods. In the first method, the \overline{A} input is low and the B input goes high. In the second method, the B input is high and the \overline{A} input goes low. In the third method, the \overline{A} input is low, the B input is high, and the clear (CLR) input goes high.

The basic pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between Cext and Rext/Cext (positive) and an external resistor connected between Rext/Cext and V_{CC} .

To obtain variable pulse durations, connect an external variable resistance between Rext/Cext and V_{CC} . Pulse duration can be reduced by taking \overline{CLR} low.

Features

- $V_{CC} = 2.0\text{ V}$ to 5.5 V operation
- All inputs $V_{IH}(\text{Max.}) = 5.5\text{ V}$ (@ $V_{CC} = 0\text{ V}$ to 5.5 V)
- All outputs $V_O(\text{Max.}) = 5.5\text{ V}$ (@ $V_{CC} = 0\text{ V}$)
- Output current $\pm 6\text{ mA}$ (@ $V_{CC} = 3.0\text{ V}$ to 3.6 V), $\pm 12\text{ mA}$ (@ $V_{CC} = 4.5\text{ V}$ to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV221AFPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74LV221ARPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)
HD74LV221ATELL	TSSOP-16 pin	TTP-16DAV	T	ELL (2,000 pcs/reel)

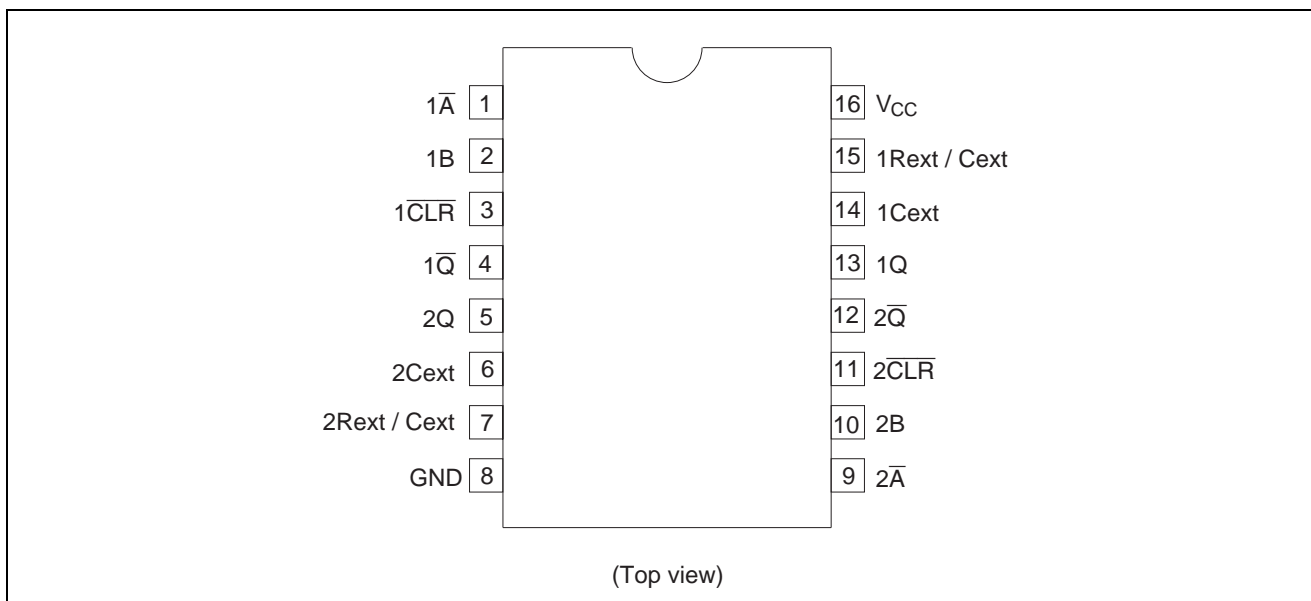
Note: Please consult the sales office for the above package availability.

Function Table

Inputs			Outputs	
CLR	\overline{A}	B	Q	\overline{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	\uparrow	HL	HL
H	\downarrow	H	HL	HL
\uparrow	L	H	HL	HL

Note: H: High level
L: Low level
X: Immaterial
 \uparrow : Low to high transition
 \downarrow : High to low transition
 HL : High level pulse
 HL : Low level pulse

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range* ¹	V_I	-0.5 to 7.0	V	
Output voltage range* ^{1, 2}	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L V_{CC} : OFF
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785 500	mW	SOP TSSOP
Storage temperature	T_{stg}	-65 to 150	°C	

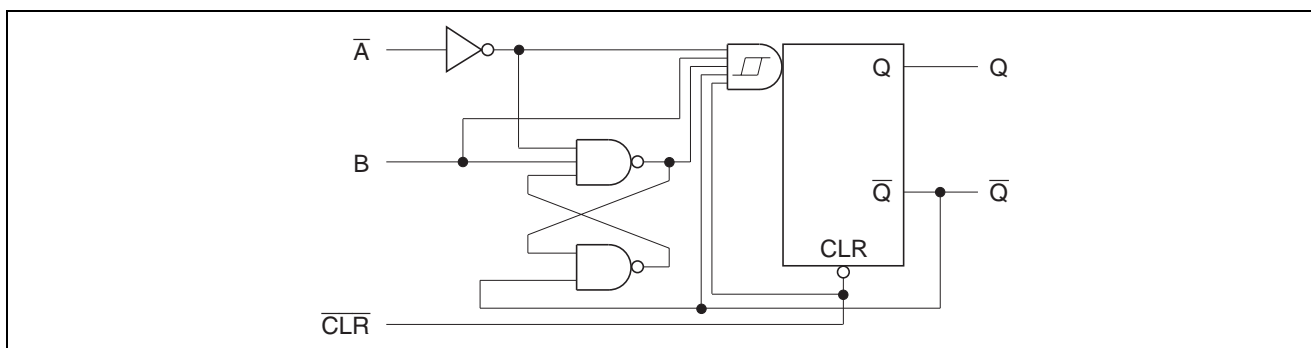
Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	—	5.5	V	
Input voltage range	V_I	0	—	5.5	V	
Output voltage range	V_O	0	—	V_{CC}	V	
Output current	I_{OH}	—	—	-50	μA	$V_{CC} = 2.0 V$
		—	—	-2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	—	-6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	—	-12		$V_{CC} = 4.5 \text{ to } 5.5 V$
	I_{OL}	—	—	50	μA	$V_{CC} = 2.0 V$
		—	—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	—	6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	—	12		$V_{CC} = 4.5 \text{ to } 5.5 V$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	—	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	—	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	—	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
External timing resistance	R_{ext}	5	—	—	k Ω	$V_{CC} = 2.0 V$
		1	—	—		$V_{CC} \geq 2.3 V$
External timing capacitance	C_{ext}	—	unlimited	—	F	
Power-up ramp rate	$\Delta t / \Delta V_{CC}$	1	—	—	ms/V	
Operating free-air temperature	T_a	-40	—	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram


DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	V _{CC} × 0.7	—	—		
		3.0 to 3.6	V _{CC} × 0.7	—	—		
		4.5 to 5.5	V _{CC} × 0.7	—	—		
	V _{IL}	2.0	—	—	0.5	V	
		2.3 to 2.7	—	—	V _{CC} × 0.3		
		3.0 to 3.6	—	—	V _{CC} × 0.3		
		4.5 to 5.5	—	—	V _{CC} × 0.3		
Output voltage	V _{OH}	Min to Max	V _{CC} - 0.1	—	—	V	I _{OH} = -50 μA
		2.3	2.0	—	—		I _{OH} = -2 mA
		3.0	2.48	—	—		I _{OH} = -6 mA
		4.5	3.8	—	—		I _{OH} = -12 mA
	V _{OL}	Min to Max	—	—	0.1	V	I _{OL} = 50 μA
		2.3	—	—	0.4		I _{OL} = 2 mA
		3.0	—	—	0.44		I _{OL} = 6 mA
		4.5	—	—	0.55		I _{OL} = 12 mA
Input current	I _{IN}	0 to 5.5	—	—	±1	μA	V _{IN} = 5.5 V or GND
Input current Rext / Cext	I _{IN}	5.5	—	—	±2.5	μA	V _{IN} = V _{CC} or GND
Quiescent supply current	I _{CC}	5.5	—	—	20	μA	V _{IN} = V _{CC} or GND, I _O = 0
Active state supply current (per circuit)	ΔI _{CC}	2.3	—	—	220	μA	V _{IN} = V _{CC} or GND Rext/Cext = 0.5 V _{CC}
		3.0	—	—	280		
		4.5	—	—	650		
		5.5	—	—	975		
Output leakage current	I _{OFF}	0	—	—	5	μA	V _I or V _O = 0 V to 5.5 V
Input capacitance	C _{IN}	3.3	—	4.0	—	pF	V _I = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

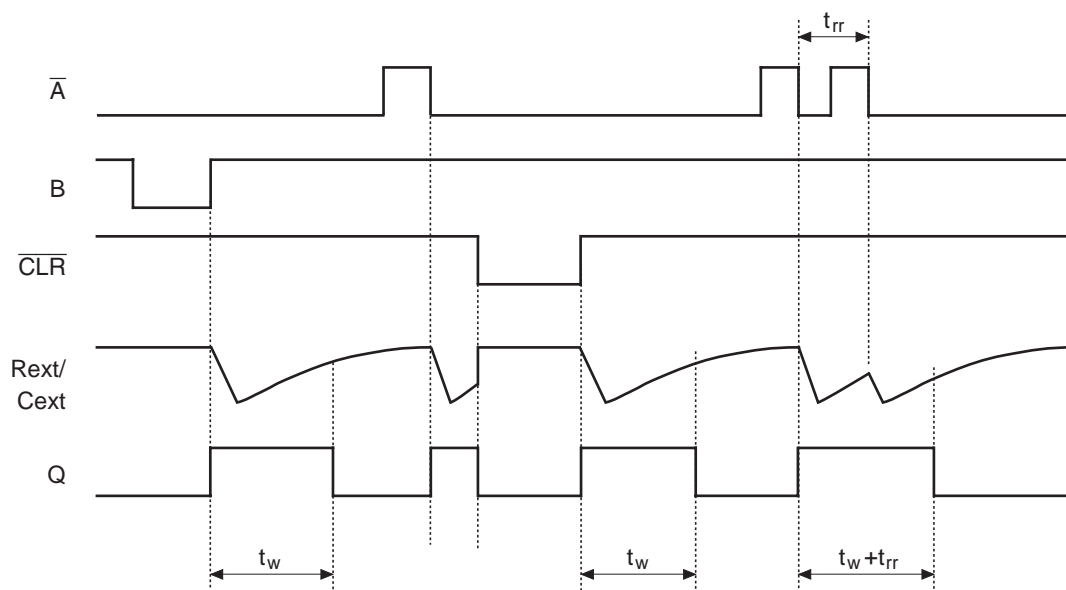
$$V_{CC} = 2.5 \pm 0.2 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	13.3	31.4	1.0	37.0	ns	C _L = 15 pF	A or B	Q or \bar{Q}
	t _{PHL}	—	15.5	36.0	1.0	42.0		C _L = 50 pF		
		—	10.9	25.0	1.0	29.5		C _L = 15 pF	\bar{CLR}	Q or \bar{Q}
		—	12.5	32.8	1.0	34.5		C _L = 50 pF		
		—	13.5	33.4	1.0	39.0		C _L = 15 pF	\bar{CLR}	Q or \bar{Q}
		—	15.9	38.0	1.0	44.0		C _L = 50 pF	(Trigger)	
Pulse width	t _w	6.0	—	—	6.5	—	ns	\bar{A} , B or \bar{CLR}		
Output pulse width	t _{wQ}	—	170	260	—	320	ns	C _L = 50 pF, Cext = 28 pF, Rext = 2 kΩ		
		90	100	110	90	110	μs	C _L = 50 pF, Cext = 0.01 μF, Rext = 10 kΩ		
		0.9	1.0	1.1	0.9	1.1	ms	C _L = 50 pF, Cext = 0.1 μF, Rext = 10 kΩ		
	Δt _{wQ}	—	±1	—	—	—	%	C _L = 50 pF		

$$V_{CC} = 3.3 \pm 0.3 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	9.9	20.6	1.0	24.0	ns	C _L = 15 pF	A or B	Q or \bar{Q}
	t _{PHL}	—	11.6	24.1	1.0	27.5		C _L = 50 pF		
		—	8.3	15.8	1.0	18.5		C _L = 15 pF	\bar{CLR}	Q or \bar{Q}
		—	9.7	19.3	1.0	22.0		C _L = 50 pF		
		—	9.9	22.4	1.0	26.0		C _L = 15 pF	\bar{CLR}	Q or \bar{Q}
		—	11.6	25.9	1.0	29.5		C _L = 50 pF	(Trigger)	
Pulse width	t _w	5.0	—	—	5.0	—	ns	\bar{A} , B or \bar{CLR}		
Output pulse width	t _{wQ}	—	150	240	—	300	ns	C _L = 50 pF, Cext = 28 pF, Rext = 2 kΩ		
		90	100	110	90	110	μs	C _L = 50 pF, Cext = 0.01 μF, Rext = 10 kΩ		
		0.9	1.0	1.1	0.9	1.1	ms	C _L = 50 pF, Cext = 0.1 μF, Rext = 10 kΩ		
	Δt _{wQ}	—	±1	—	—	—	%	C _L = 50 pF		

Timing diagram



Caution in use

In order to prevent any malfunctions due to noise, connect a high frequency performance capacitor between Vcc and GND, and keep the wiring between the External components and Cext, Rext/Cext pins as short as possible.

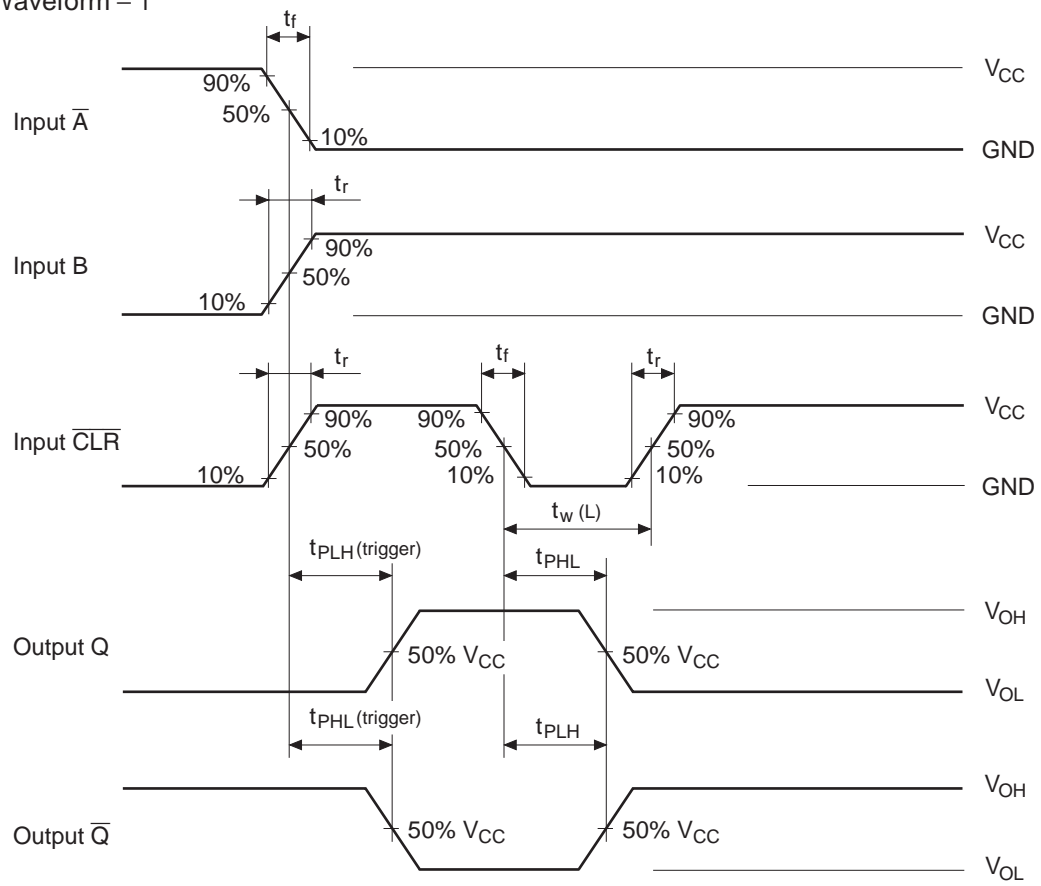
Large values of Cext may cause problems when powering down the HD74LV221A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from Vcc through the protection diodes at pin 7 or pin 15.

Current through the input protection diodes must be limited to 20 mA; therefore, the turn-off time of the Vcc power supply must not be faster than $t = V_{cc} \cdot C_{ext} / (20 \text{ mA})$. For example, if $V_{cc} = 5 \text{ V}$ and $C_{ext} = 22 \mu\text{F}$, the Vcc supply must turn off no faster than $t = (5 \text{ V}) \cdot (22 \mu\text{F}) / 20 \text{ mA} = 5.5 \text{ ms}$. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

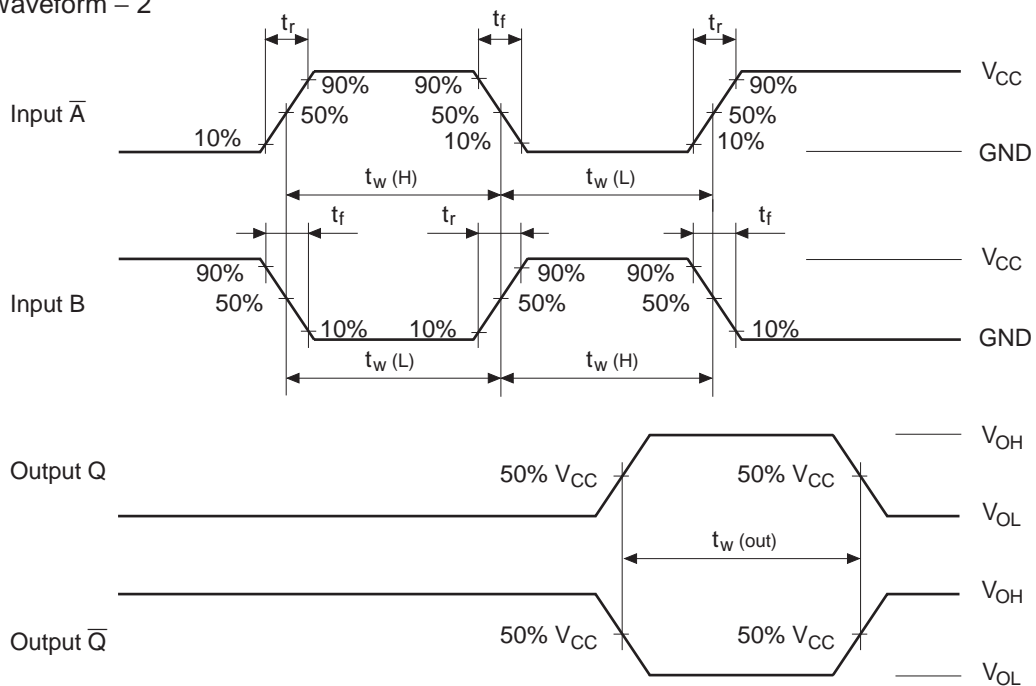
When a more rapid decrease of Vcc to zero volts occurs, the HD74LV221A may sustain damage. To avoid this possibility, use an external clamping diode.

The input pins for unused circuit should be used under conditions to fix the outputs to avoid malfunction caused by noises. Also, it's recommended that Rext / Cext terminals are open and external parts are not connected to.

• Waveform – 1

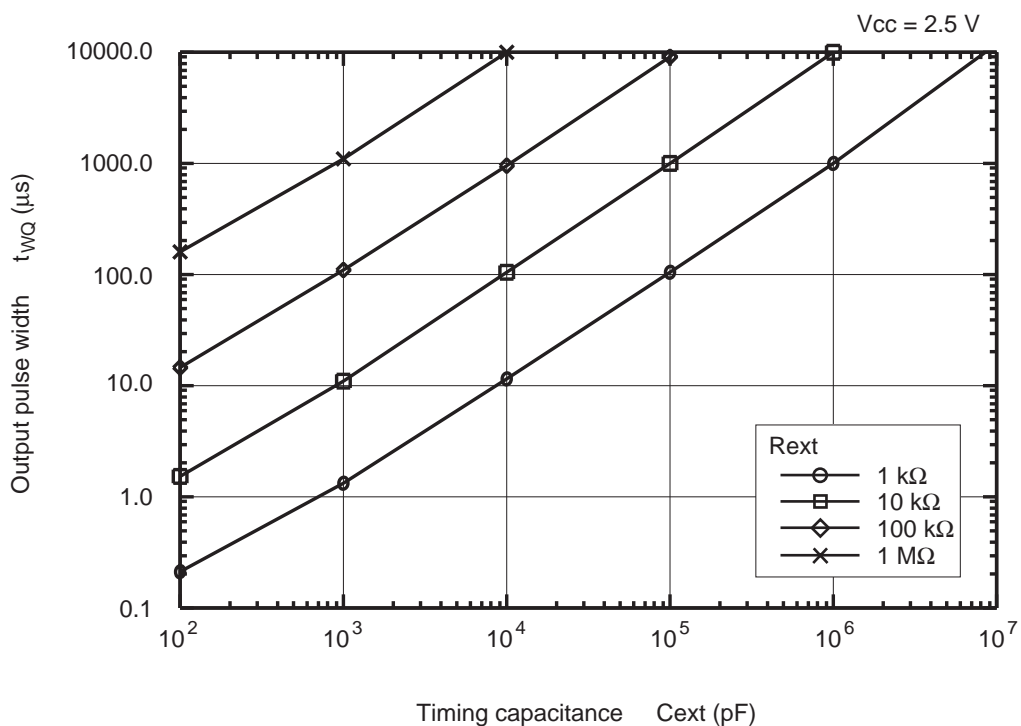


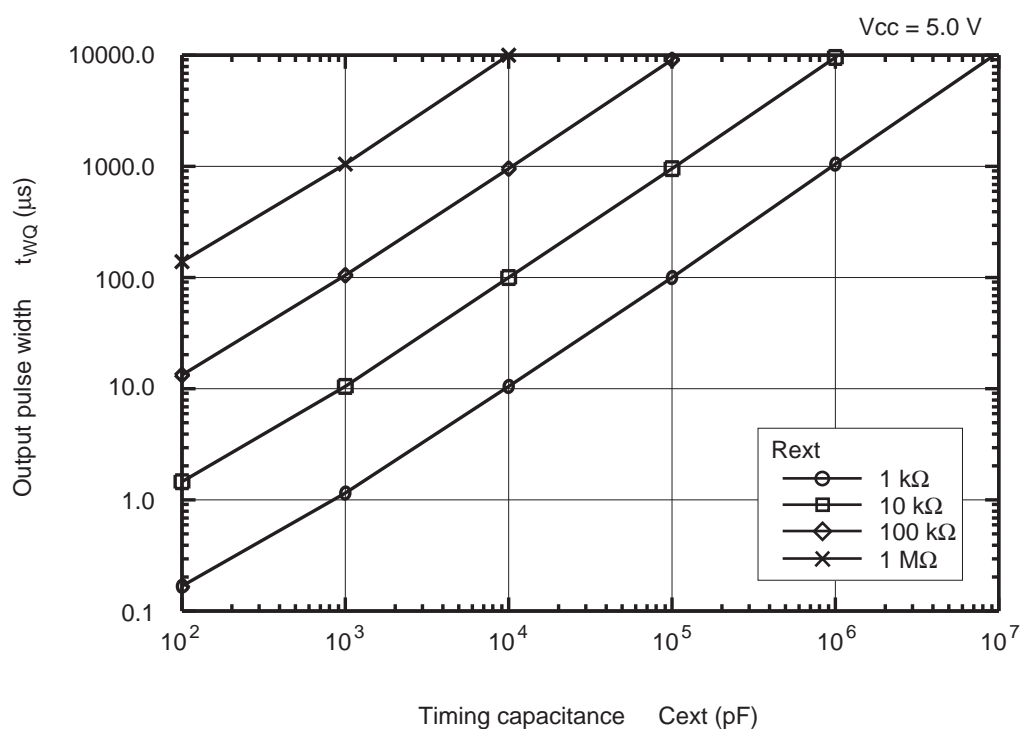
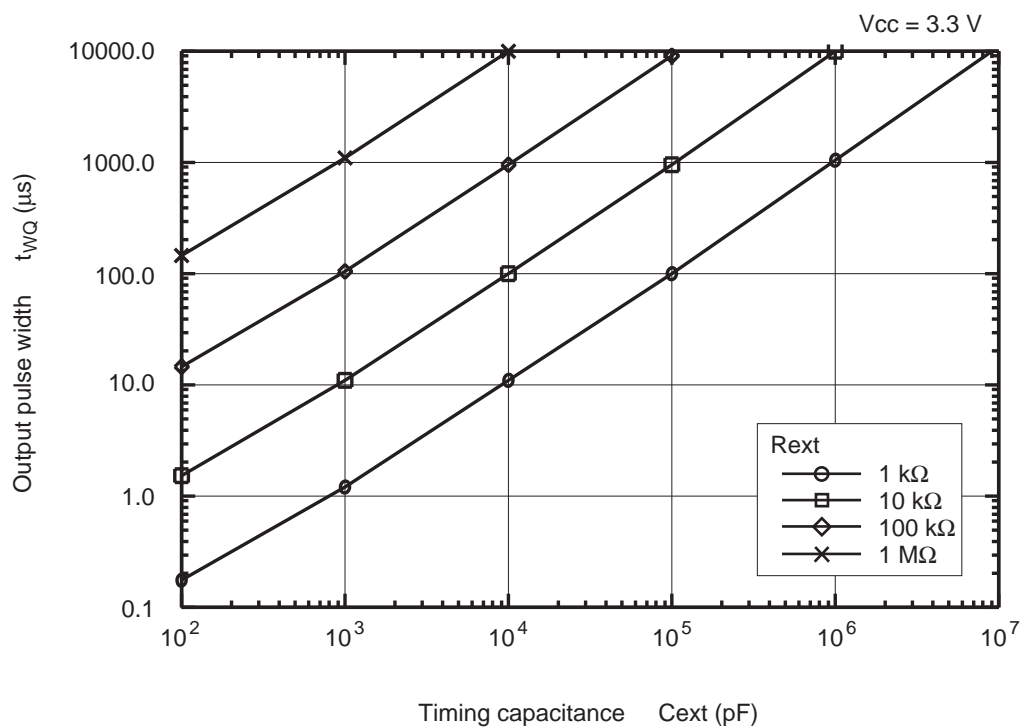
• Waveform – 2

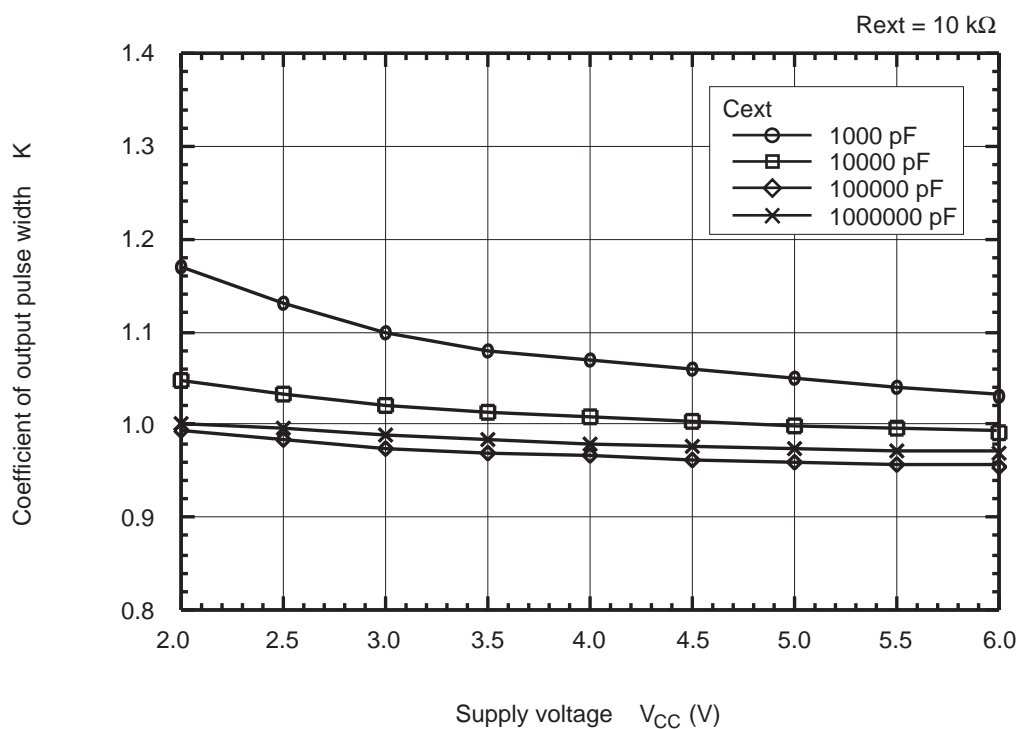
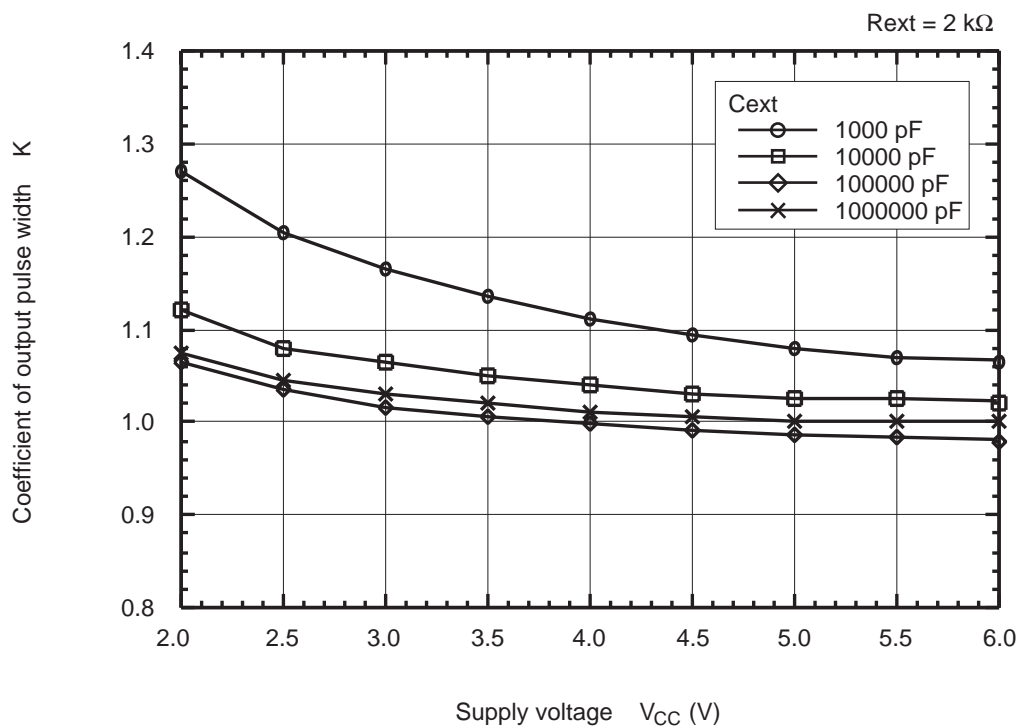


Notes: 1. Input waveform: PRR \leq 1 MHz, $Z_o = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns
2. The output are measured one at a time with one transition per measurement.

Application Data



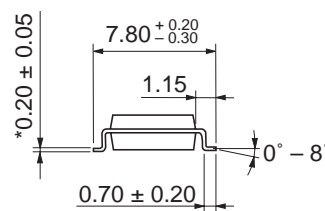
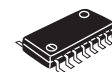
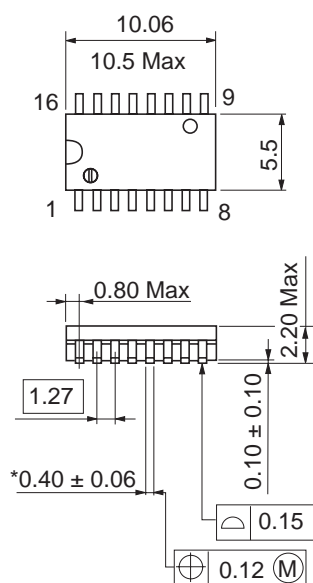




Package Dimensions

As of January, 2003

Unit: mm

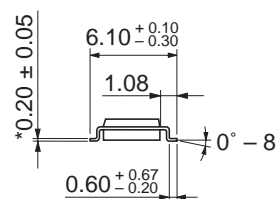
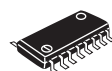
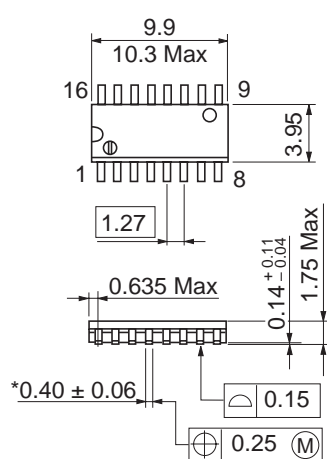


*Ni/Pd/Au plating

Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

As of January, 2003

Unit: mm

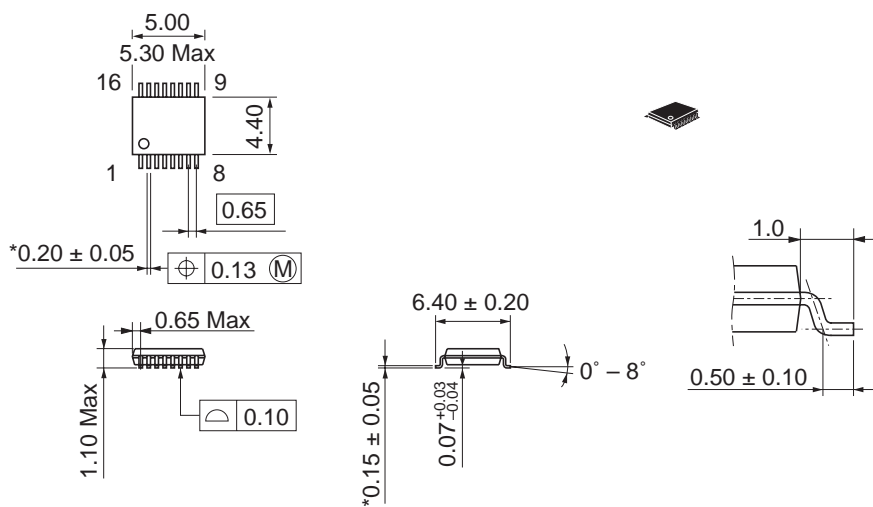


*Ni/Pd/Au plating

Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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