HD74LV221A

Dual Monostable Multivibrators

REJ03D0326–0600Z
(Previous ADE-205-271D (Z))
Rev.6.00
Jun. 23, 2004

Description

The HD74LV221A features output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low and the B input goes high. In the second method, the B input is high and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

The basic pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between Cext and Rext/Cext (positive) and an external resistor connected between Rext/Cext and V_{CC}.

To obtain variable pulse durations, connect an external variable resistance between Rext/Cext and V_{CC}. Pulse duration can be reduced by taking $\overline{CLR}$ low.

Features

- V_{CC} = 2.0 V to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Output current ±6 mA (@V_{CC} = 3.0 V to 3.6 V), ±12 mA (@V_{CC} = 4.5 V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV221AFPEL	SOP–16 pin (JEITA)	FP–16DAV	FP	EL (2,000 pcs/reel)
HD74LV221ARPEL	SOP–16 pin (JEDEC)	FP–16DNV	RP	EL (2,500 pcs/reel)
HD74LV221ATELL	TSSOP–16 pin	TTP–16DAV	T	ELL (2,000 pcs/reel)

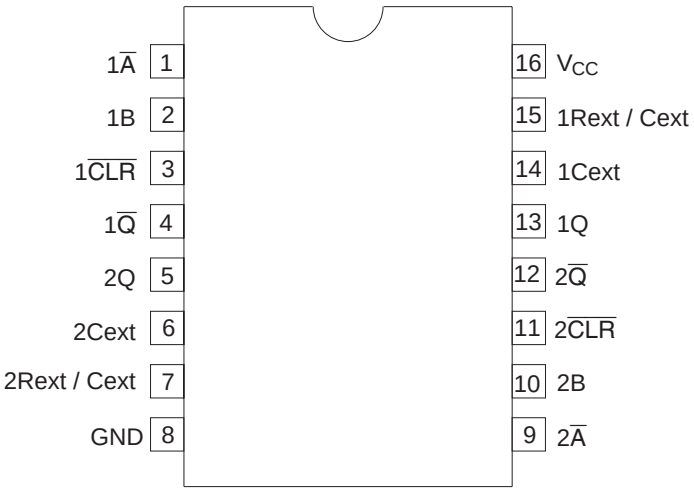
Note: Please consult the sales office for the above package availability.

Function Table

Inputs			Outputs	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎌
H	↓	H	⎍	⎌
↑	L	H	⎍	⎌

Note: H: High level
L: Low level
X: Immaterial
↑: Low to high transition
↓: High to low transition
⎍: High level pulse
⎌: Low level pulse

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range*[1]	V_I	–0.5 to 7.0	V	
Output voltage range*[1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output: H or L
		–0.5 to 7.0		V_{CC}: OFF
Input clamp current	I_{IK}	–20	mA	V_I < 0
Output clamp current	I_{OK}	±50	mA	V_O < 0 or V_O > V_{CC}
Continuous output current	I_O	±25	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at Ta = 25°C (in still air)*[3]	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

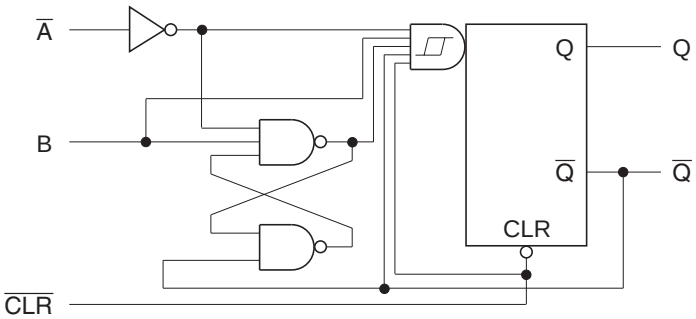
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	—	5.5	V	
Input voltage range	V_I	0	—	5.5	V	
Output voltage range	V_O	0	—	V_{CC}	V	
Output current	I_{OH}	—	—	–50	µA	V_{CC} = 2.0 V
		—	—	–2	mA	V_{CC} = 2.3 to 2.7 V
		—	—	–6		V_{CC} = 3.0 to 3.6 V
		—	—	–12		V_{CC} = 4.5 to 5.5 V
	I_{OL}	—	—	50	µA	V_{CC} = 2.0 V
		—	—	2	mA	V_{CC} = 2.3 to 2.7 V
		—	—	6		V_{CC} = 3.0 to 3.6 V
		—	—	12		V_{CC} = 4.5 to 5.5 V
Input transition rise or fall rate	Δt /Δv	0	—	200	ns/V	V_{CC} = 2.3 to 2.7 V
		0	—	100		V_{CC} = 3.0 to 3.6 V
		0	—	20		V_{CC} = 4.5 to 5.5 V
External timing resistance	Rext	5	—	—	kΩ	V_{CC} = 2.0 V
		1	—	—		V_{CC} ≥ 2.3 V
External timing capacitance	Cext	—	unlimited	—	F	
Power-up ramp rate	$\Delta t / \Delta V_{CC}$	1	—	—	ms/V	
Operating free-air temperature	Ta	–40	—	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

Ta = –40 to 85°C

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	Min to Max	V_{CC} – 0.1	—	—	V	I_{OH} = –50 µA
		2.3	2.0	—	—		I_{OH} = –2 mA
		3.0	2.48	—	—		I_{OH} = –6 mA
		4.5	3.8	—	—		I_{OH} = –12 mA
	V_{OL}	Min to Max	—	—	0.1	V	I_{OL} = 50 µA
		2.3	—	—	0.4		I_{OL} = 2 mA
		3.0	—	—	0.44		I_{OL} = 6 mA
		4.5	—	—	0.55		I_{OL} = 12 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	µA	V_{IN} = 5.5 V or GND
Input current Rext / Cext	I_{IN}	5.5	—	—	±2.5	µA	V_{IN} = V_{CC} or GND
Quiescent supply current	I_{CC}	5.5	—	—	20	µA	V_{IN} = V_{CC} or GND, I_O = 0
Active state supply current (per circuit)	ΔI_{CC}	2.3	—	—	220	µA	V_{IN} = V_{CC} or GND Rext/Cext = 0.5 V_{CC}
		3.0			280		
		4.5			650		
		5.5			975		
Output leakage current	I_{OFF}	0	—	—	5	µA	V_I or V_O = 0 V to 5.5 V
Input capacitance	C_{IN}	3.3	—	4.0	—	pF	V_I = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	13.3	31.4	1.0	37.0	ns	C_L = 15 pF	A or B	Q or $\overline{Q}$
	t_{PHL}	—	15.5	36.0	1.0	42.0		C_L = 50 pF		
		—	10.9	25.0	1.0	29.5		C_L = 15 pF	$\overline{CLR}$	Q or $\overline{Q}$
		—	12.5	32.8	1.0	34.5		C_L = 50 pF		
		—	13.5	33.4	1.0	39.0		C_L = 15 pF	$\overline{CLR}$	Q or $\overline{Q}$
		—	15.9	38.0	1.0	44.0		C_L = 50 pF	(Trigger)	
Pulse width	t_w	6.0	—	—	6.5	—	ns	$\overline{A}$, B or $\overline{CLR}$		
Output pulse width	t_{wQ}	—	170	260	—	320	ns	C_L = 50 pF, Cext = 28 pF, Rext = 2 kΩ		
		90	100	110	90	110	µs	C_L = 50 pF, Cext = 0.01 µF, Rext = 10 kΩ		
		0.9	1.0	1.1	0.9	1.1	ms	C_L = 50 pF, Cext = 0.1 µF, Rext = 10 kΩ		
	Δt_{wQ}	—	±1	—	—	—	%	C_L = 50 pF		

V_{CC} = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	9.9	20.6	1.0	24.0	ns	C_L = 15 pF	A or B	Q or $\overline{Q}$
	t_{PHL}	—	11.6	24.1	1.0	27.5		C_L = 50 pF		
		—	8.3	15.8	1.0	18.5		C_L = 15 pF	$\overline{CLR}$	Q or $\overline{Q}$
		—	9.7	19.3	1.0	22.0		C_L = 50 pF		
		—	9.9	22.4	1.0	26.0		C_L = 15 pF	$\overline{CLR}$	Q or $\overline{Q}$
		—	11.6	25.9	1.0	29.5		C_L = 50 pF	(Trigger)	
Pulse width	t_w	5.0	—	—	5.0	—	ns	$\overline{A}$, B or $\overline{CLR}$		
Output pulse width	t_{wQ}	—	150	240	—	300	ns	C_L = 50 pF, Cext = 28 pF, Rext = 2 kΩ		
		90	100	110	90	110	µs	C_L = 50 pF, Cext = 0.01 µF, Rext = 10 kΩ		
		0.9	1.0	1.1	0.9	1.1	ms	C_L = 50 pF, Cext = 0.1 µF, Rext = 10 kΩ		
	Δt_{wQ}	—	±1	—	—	—	%	C_L = 50 pF		

Switching Characteristics (cont)

V_{CC} = 5.0 ± 0.5 V

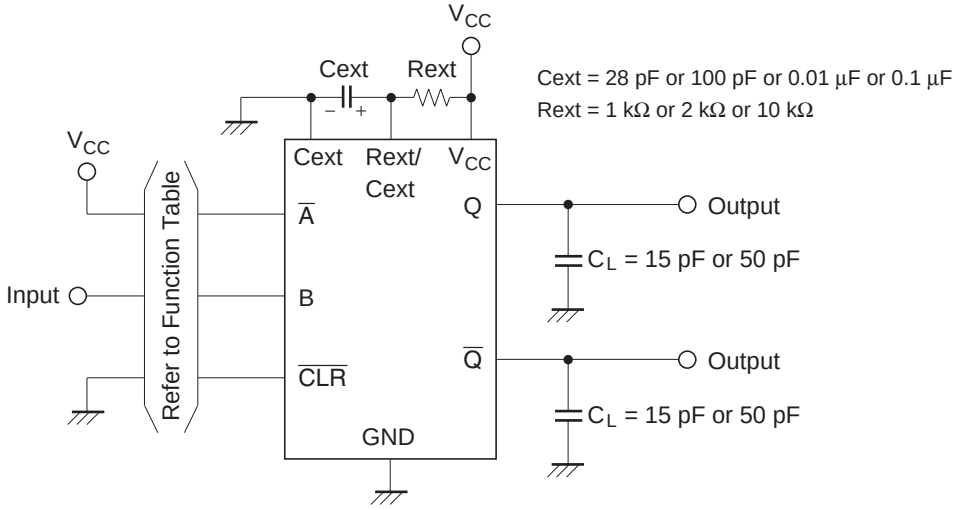
Item	Symbol	Ta = 25°C Min	Typ	Max	Ta = –40 to 85°C Min	Max	Unit	Test Conditions	FROM (Input)	TO (Output)
Propagation delay time	t_{PLH}	—	7.3	12.0	1.0	14.0	ns	C_L = 15 pF	A or B	Q or $\overline{Q}$
	t_{PHL}	—	8.7	14.0	1.0	16.0		C_L = 50 pF		
		—	6.2	9.4	1.0	11.0		C_L = 15 pF	$\overline{CLR}$	Q or $\overline{Q}$
		—	7.4	11.4	1.0	13.0		C_L = 50 pF		
		—	7.3	12.9	1.0	15.0		C_L = 15 pF	$\overline{CLR}$	Q or $\overline{Q}$
		—	8.6	14.9	1.0	17.0		C_L = 50 pF	(Trigger)	
Pulse width	t_w	5.0	—	—	5.0	—	ns	$\overline{A}$, B or $\overline{CLR}$		
Output pulse width	t_{wQ}	—	140	200	—	240	ns	C_L = 50 pF, Cext = 28 pF, Rext = 2 kΩ		
		90	100	110	90	110	µs	C_L = 50 pF, Cext = 0.01 µF, Rext = 10 kΩ		
		0.9	1.0	1.1	0.9	1.1	ms	C_L = 50 pF, Cext = 0.1 µF, Rext = 10 kΩ		
	Δt_{wQ}	—	±1	—	—	—	%	CL = 50 pF		

Operating Characteristics

C_L = 50 pF

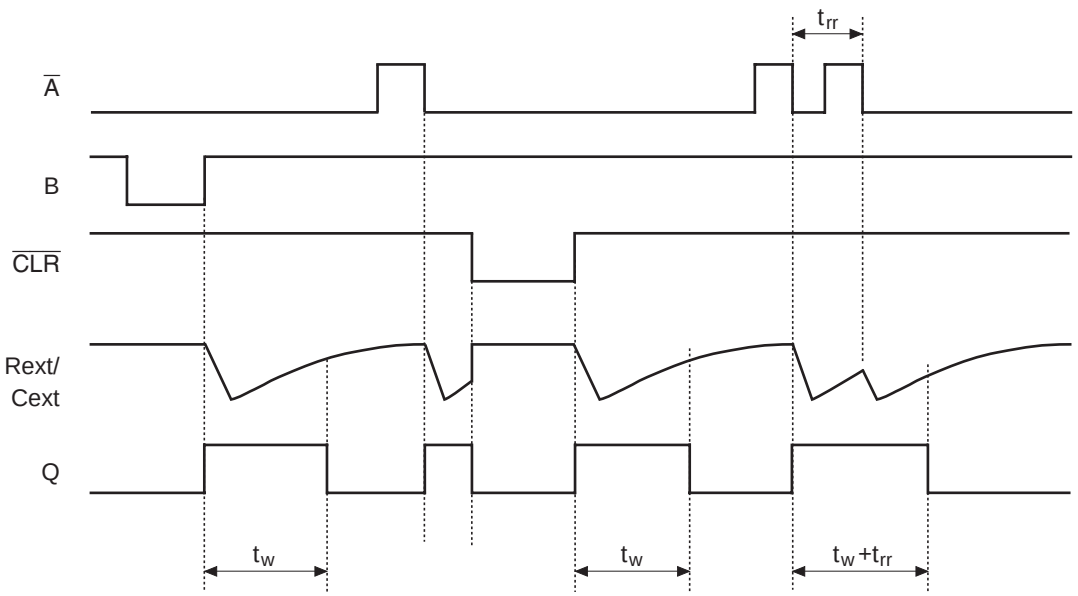
Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Unit	Test Conditions
Power dissipation capacitance	C_{PD}	3.3	—	74.0	—	pF	f = 10 MHz
		5.0	—	86.0	—		

Test Circuit



Note : C_L includes the probe and jig capacitance.

Timing diagram



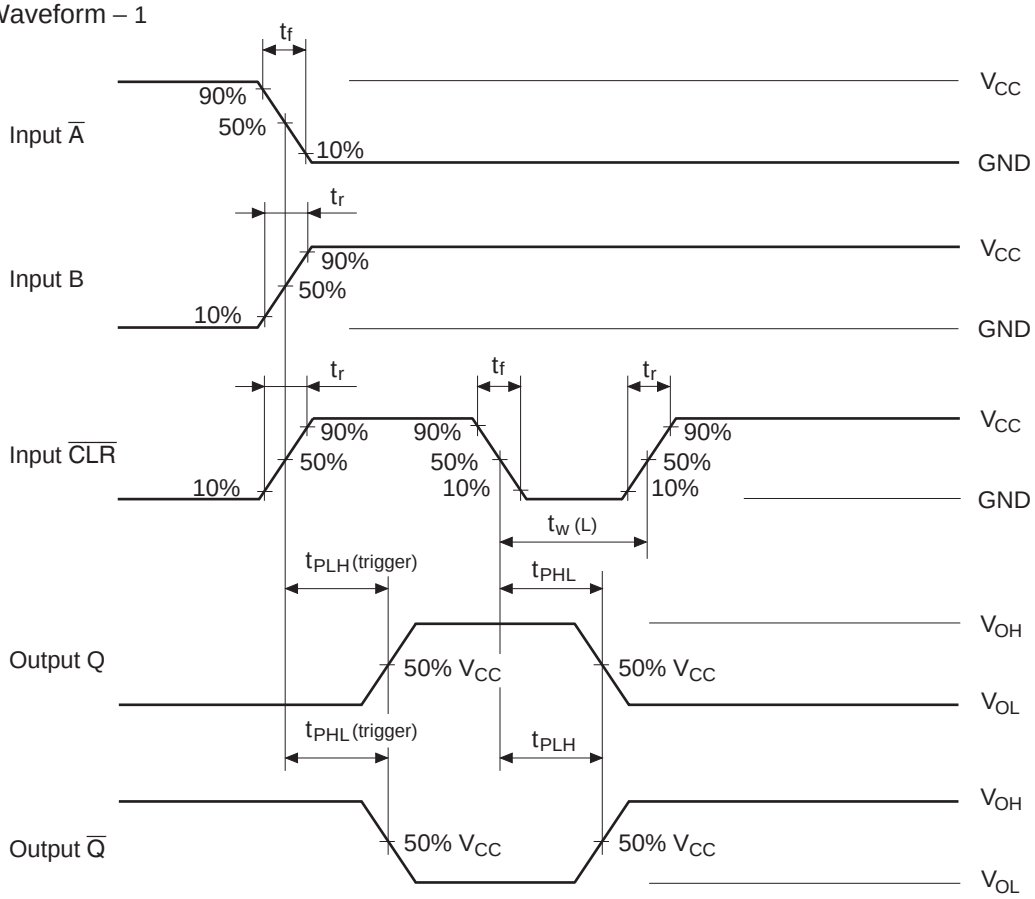
Caution in use

In order to prevent any malfunctions due to noise, connect a high frequency performance capacitor between Vcc and GND, and keep the wiring between the External components and Cext, Rext/Cext pins as short as possible.

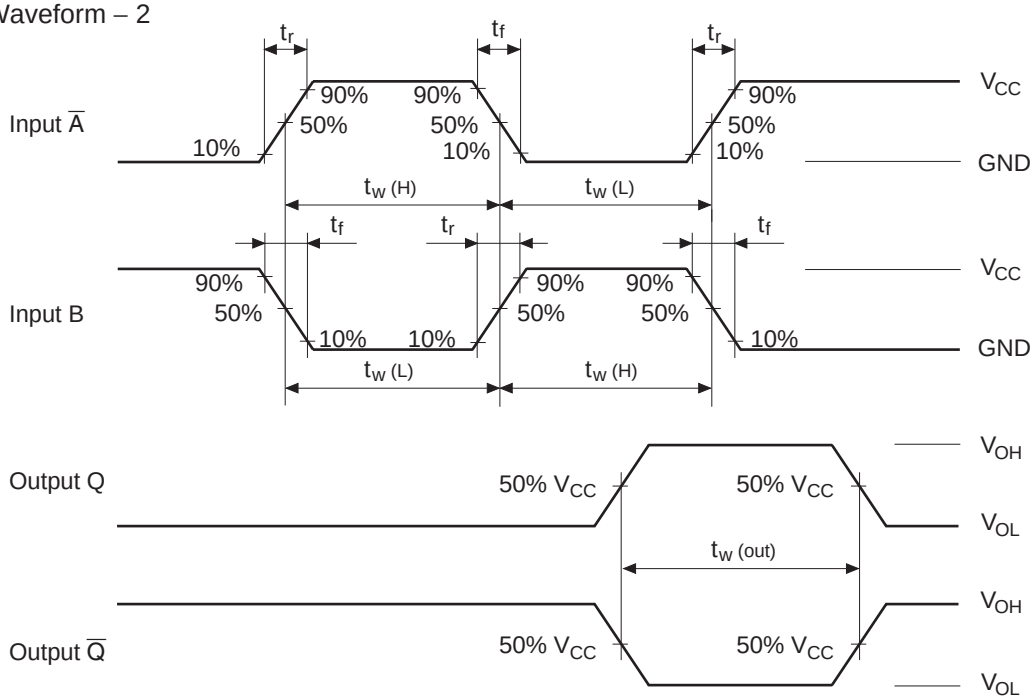
Large values of Cext may cause problems when powering down the HD74LV221A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from Vcc through the protection diodes at pin 7 or pin 15.
Current through the input protection diodes must be limited to 20 mA; therefore, the turn-off time of the Vcc power supply must not be faster than t = Vcc • Cext/(20 mA). For example, if Vcc = 5 V and Cext = 22 µF, the Vcc supply must turn off no faster than t = (5 V) • (22 µF)/ 20 mA = 5.5 ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.
When a more rapid decrease of Vcc to zero volts occurs, the HD74LV221A may sustain damage. To avoid this possibility, use an external calmping diode.

The input pins for unused circuit should be used under conditions to fix the outputs to avoid malfunction cased by noises. Also, it's recommended that Rext / Cext terminals are open and external parts are not connected to.

• Waveform – 1

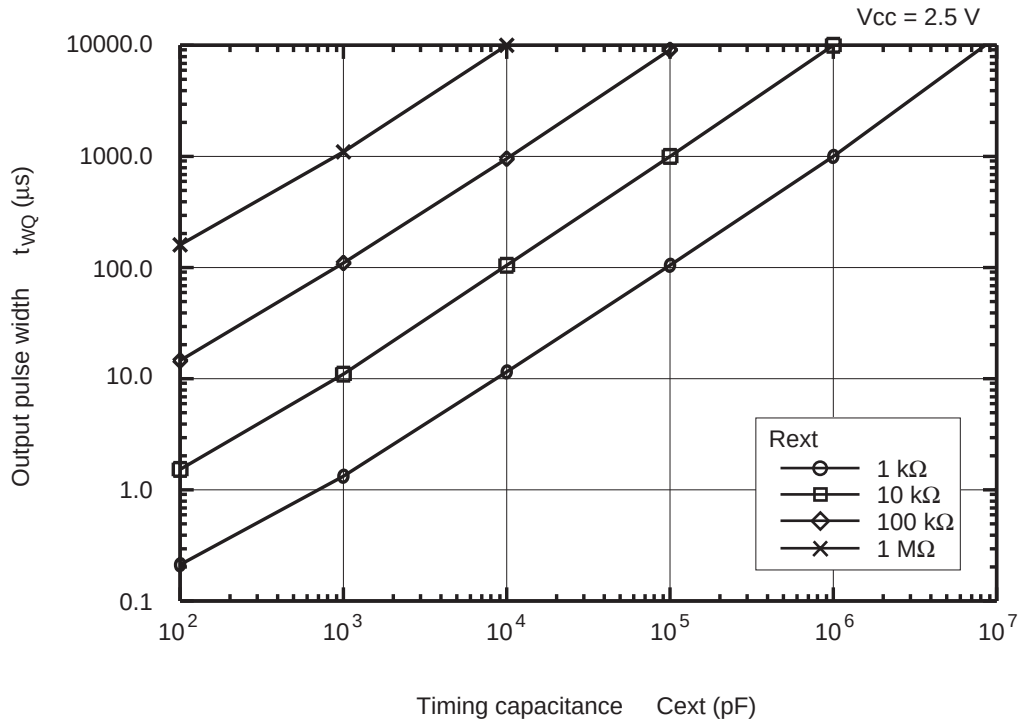

tf
90%
50%
10%
Input $\overline{A}$
VCC
GND
tr
Input B
VCC
GND
Input $\overline{CLR}$
VCC
GND
tw (L)
tPLH (trigger)
tPHL
Output Q
VOH
VOL
50% VCC
tPHL (trigger)
tPLH
Output $\overline{Q}$
VOH
VOL

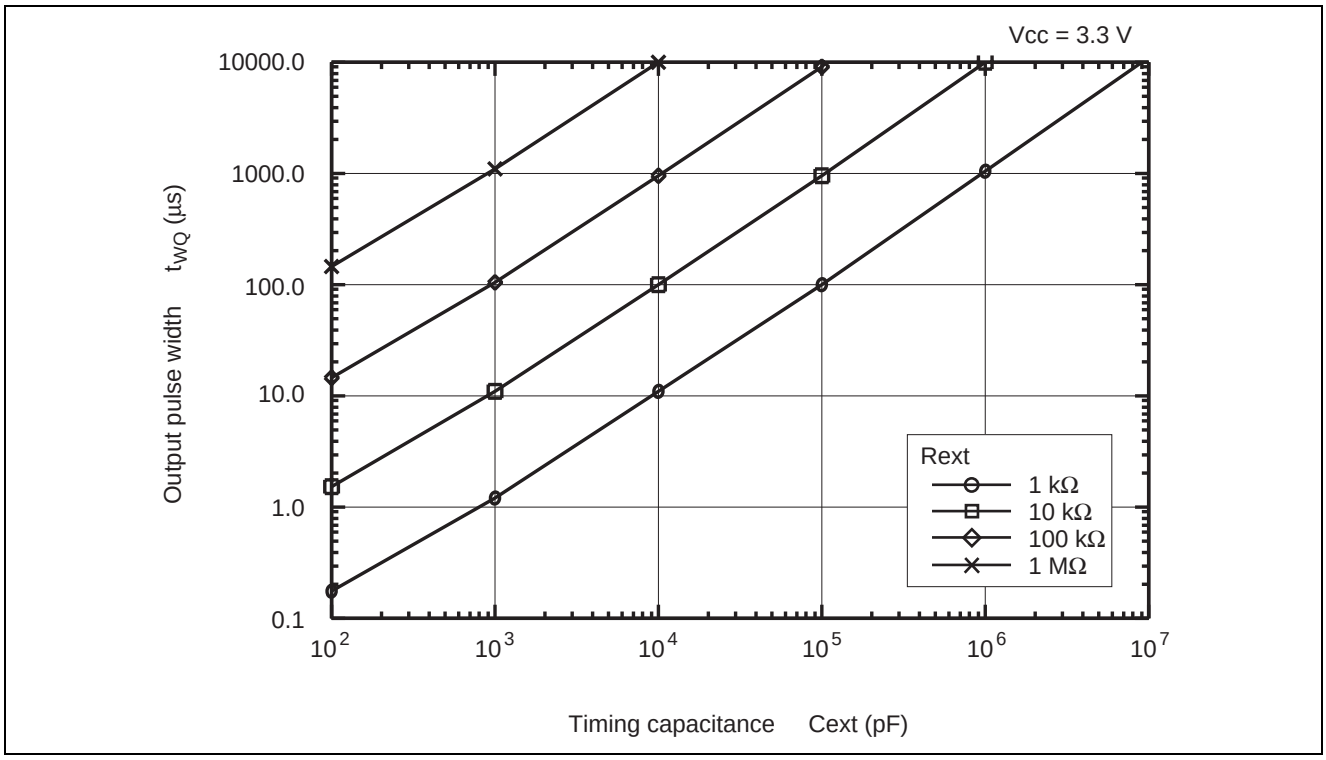
• Waveform – 2

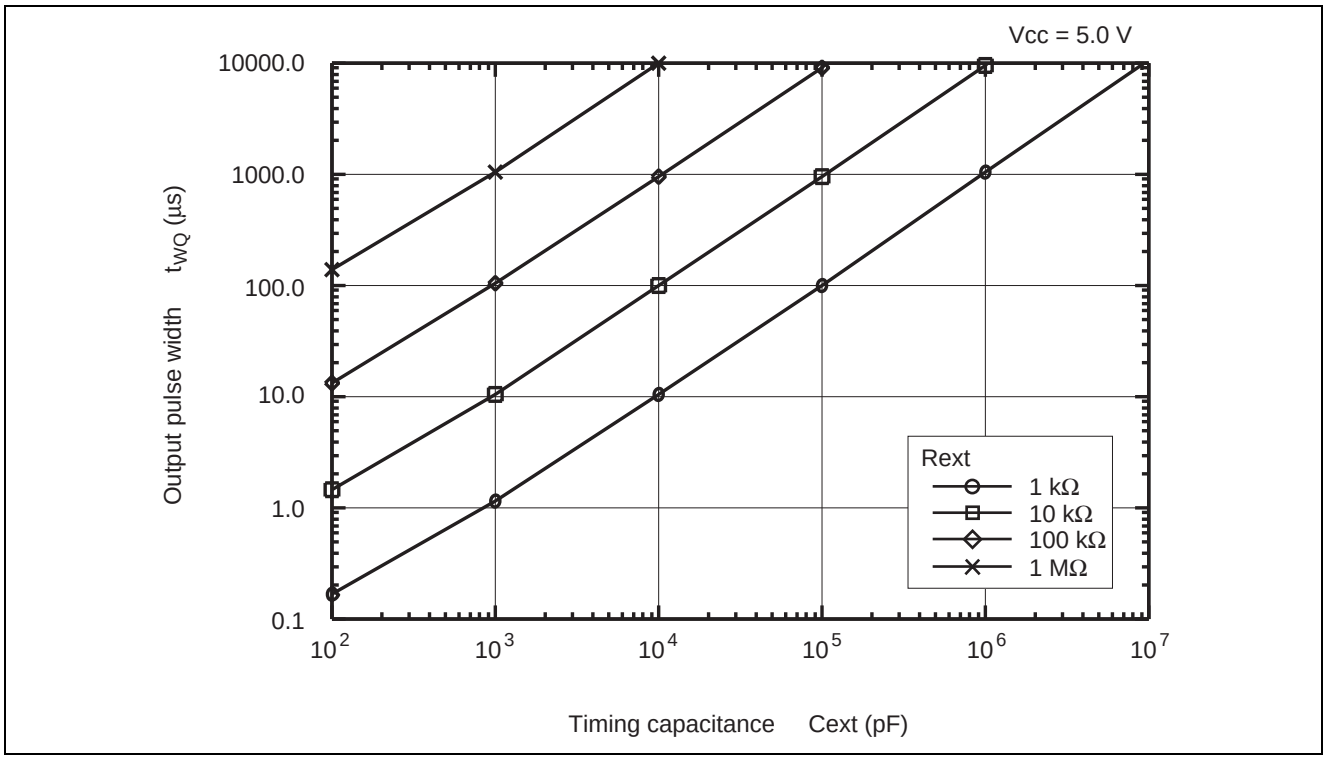


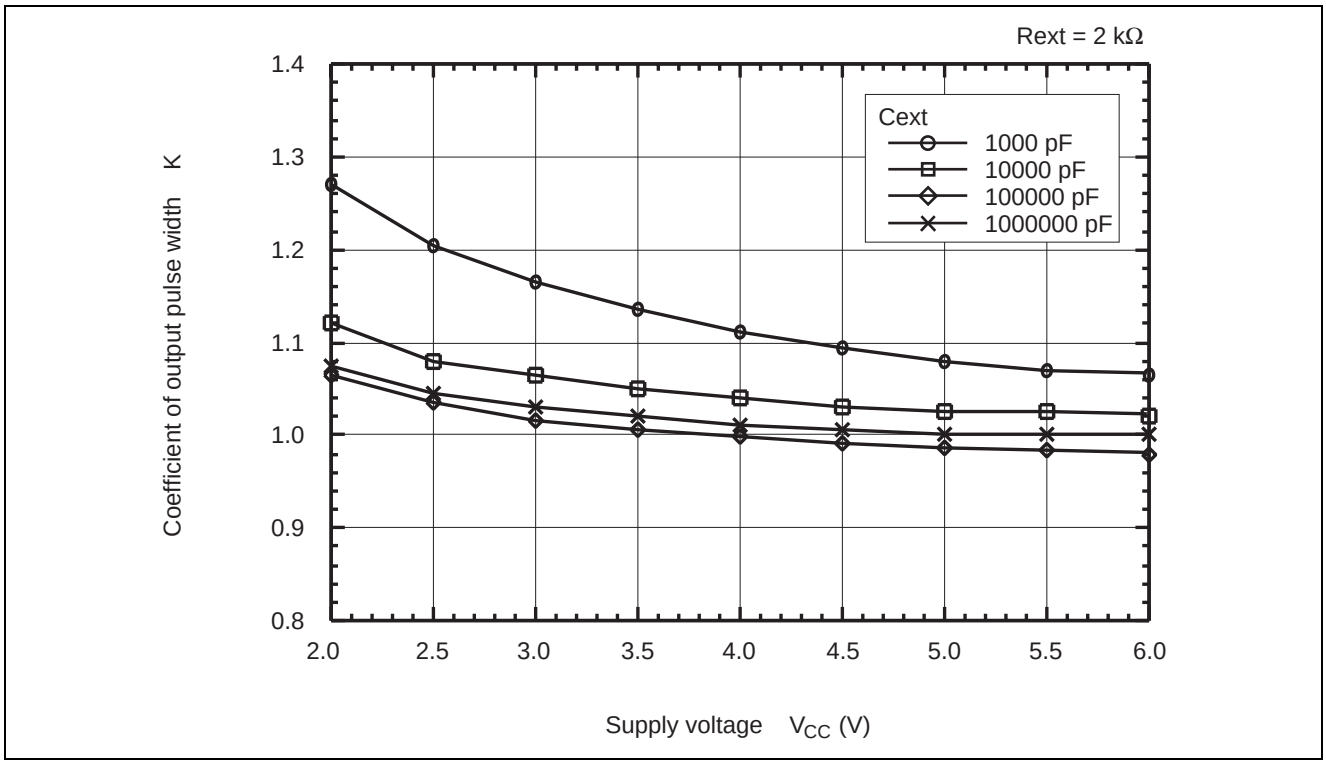
Notes: 1. Input waveform: PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns
2. The output are measured one at a time with one transition per measurement.

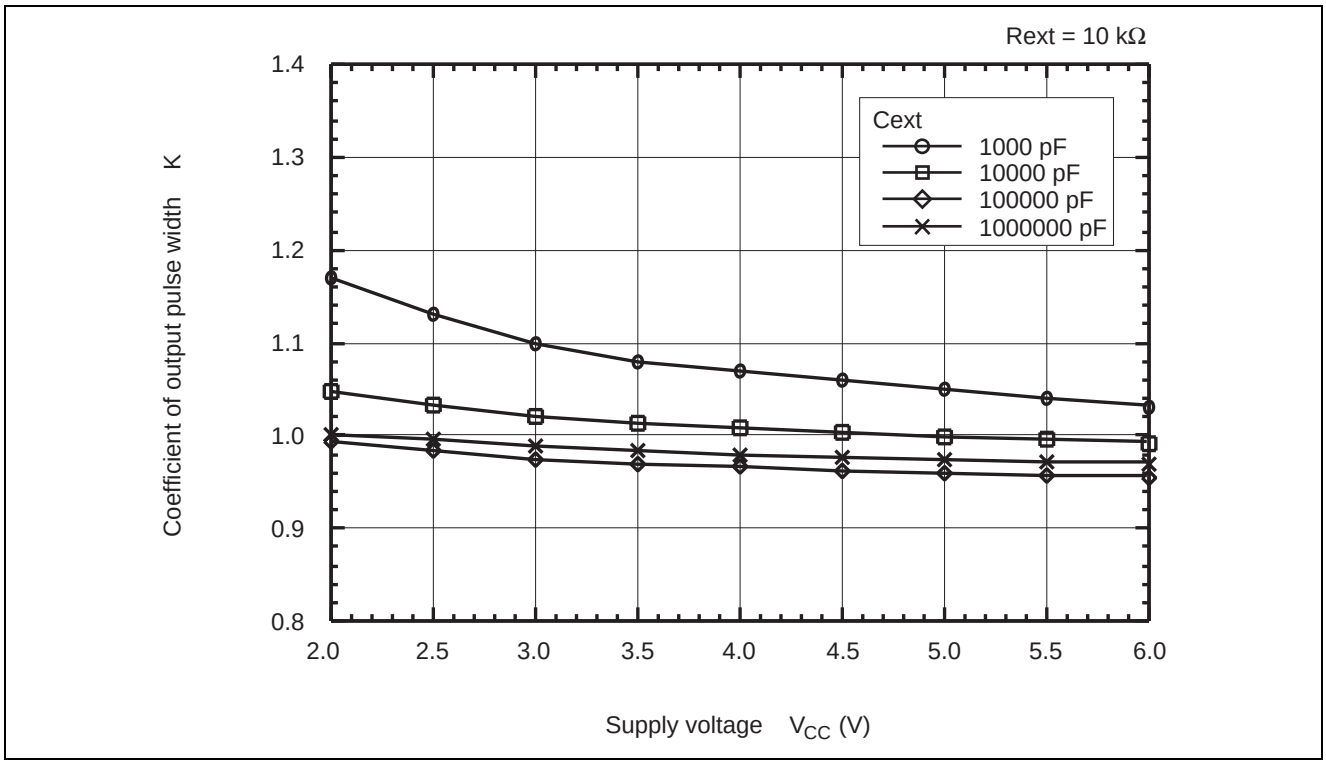
Application Data




Vcc = 3.3 V
10000.0
1000.0
100.0
10.0
1.0
0.1
Output pulse width tWQ (µs)
Rext
1 kΩ
10 kΩ
100 kΩ
1 MΩ
10^2
10^3
10^4
10^5
10^6
10^7
Timing capacitance Cext (pF)


Vcc = 5.0 V
10000.0
1000.0
100.0
10.0
1.0
0.1
Output pulse width tWQ (µs)
Rext
1 kΩ
10 kΩ
100 kΩ
1 MΩ
10^2
10^3
10^4
10^5
10^6
10^7
Timing capacitance Cext (pF)

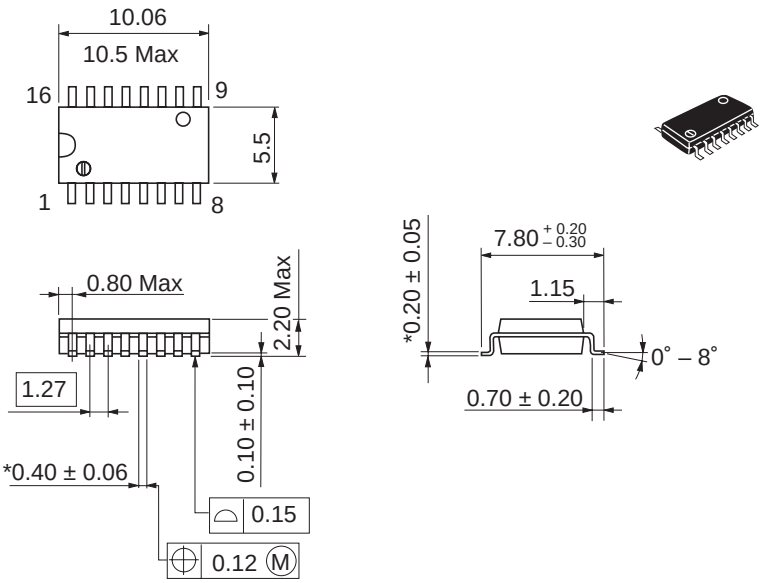

Rext = 2 kΩ
Coefficient of output pulse width K
1.4
1.3
1.2
1.1
1.0
0.9
0.8
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
Supply voltage V_{CC} (V)
Cext
1000 pF
10000 pF
100000 pF
1000000 pF


Rext = 10 kΩ
Coefficient of output pulse width K
1.4
1.3
1.2
1.1
1.0
0.9
0.8
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
Supply voltage V_{CC} (V)
Cext
1000 pF
10000 pF
100000 pF
1000000 pF

Package Dimensions

As of January, 2003

Unit: mm

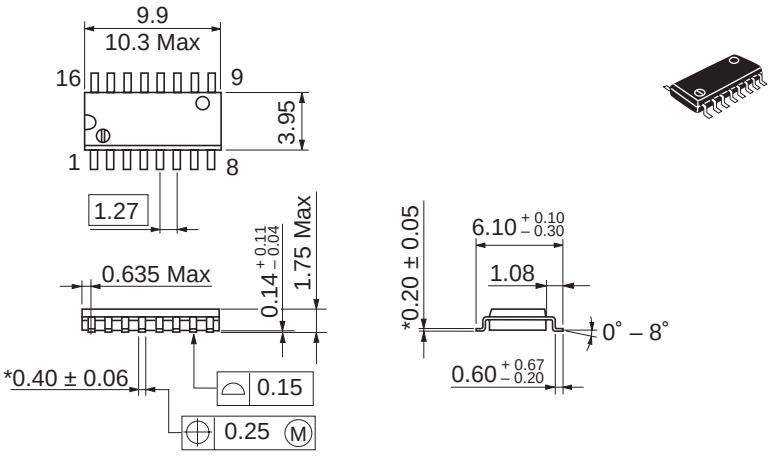


Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm

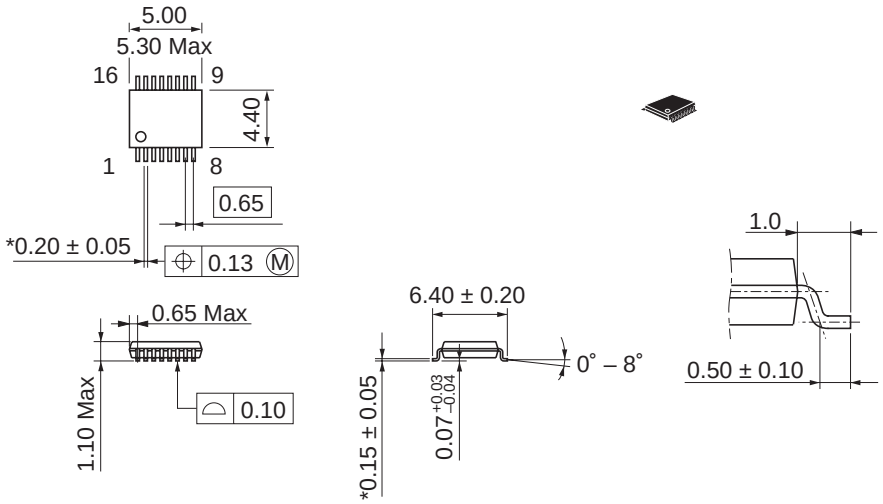


Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Colophon .1.0