INTERSIL

U1897-U1899
N-Channel JFET

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FEATURES

- **Low Insertion Loss**
  $r_{DS(on)} < 30\Omega$ (U1897)
- **No Error or Offset Voltage Generated by Closed Switch**

APPLICATIONS

Analog, Switches, Choppers, Communicators

ABSOLUTE MAXIMUM RATINGS (25°)

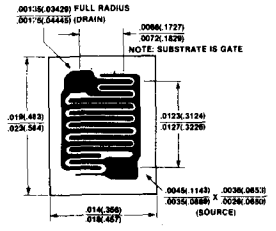
Gate-Drain or Gate-Source Voltage..... −40V
Forward Gate Current.....10mA
Total Continuous Device Dissipation
at (or Below) $T_A = 25°C$
(Derate 3.5mW/°C to 125°C).....350mW
Storage Temperature Range..... −55 to +125°C
Operating Temperature Range..... −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds.....300°C

PIN CONFIGURATION

TO-92

CHIP TOPOGRAPHY

5001B



ORDERING INFORMATION

TO-92	WAFER	DICE
U1897	U1897/W	U1897/D
U1898	U1898/W	U1898/D
U1899	U1899/W	U1899/D

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

		PARAMETERS	U1897 MIN	U1897 MAX	U1898 MIN	U1898 MAX	U1899 MIN	U1899 MAX	UNIT	TEST CONDITIONS
STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	$I_G = -1\mu A$, $V_{DS} = 0$
	BV_{DGO}	Drain-Gate Breakdown Voltage	40		40		40			$I_G = -1\mu A$, $I_S = 0$
	BV_{SGO}	Source-Gate Breakdown Voltage	40		40		40			$I_G = -1\mu A$, $I_D = 0$
	I_{GSS}	Gate Reverse Current		−400		−400		−400	pA	$V_{GS} = -20V$, $V_{DS} = 0$
	I_{DGO}	Drain-Gate Leakage Current		200		200		200		$V_{DG} = 20V$, $I_S = 0$
	I_{SGO}	Source-Gate Leakage Current		200		200		200		$V_{SG} = 20V$, $I_D = 0$
	$I_{D(off)}$	Drain Cutoff Current		200		200		200		$V_{DS} = 20V$, $V_{GS} = -12V$ (U1897)
				10		10		10	nA	$V_{GS} = -8V$ (U1898)
										$V_{GS} = -6V$ (U1899) $T_A = 85°C$
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−5.0	−10	−2.0	−7.0	−1.0	−5.0	V	$V_{DS} = 20V$, $I_D = 1$ na
	I_{DSS}	Saturation Drain Current (Note 1)	30		15		8.0		mA	$V_{DS} = 20V$, $V_{GS} = 0$
	$V_{DS(on)}$	Drain-Source ON Voltage		0.2		0.2		0.2	V	$V_{GS} = 0$, $I_D = 6.6mA$ (U1897) $I_D = 4.0mA$ (U1898) $I_D = 2.5mA$ (U1899)
	$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$I_D = 1mA$, $V_{GS} = 0$
DYNAMIC	C_{DG}	Drain-Gate Capacitance		5		5		5	pF	$V_{DG} = 20V$, $I_S = 0$ f = 1 MHz
	C_{SG}	Source-Gate Capacitance		5		5		5		$V_{SG} = 20V$, $I_D = 0$ f = 1 MHz
	C_{ISS}	Common-Source Input Capacitance		16		16		16		$V_{DS} = 20V$, $V_{GS} = 0$ f = 1 MHz
	C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5		3.5		$V_{DS} = 20V$, $V_{GS} = 0$ f = 1 MHz
	$t_{d(on)}$	Turn ON Delay Time		15		15		20	ns	Switching Time Test Conditions
	t_r	Rise Time		10		20		40		
	t_{off}	Turn OFF Time		40		60		80		

Switching Time Test Conditions	U1897	U1898	U1899
V_{DD}	3V	3V	3V
$V_{GS(on)}$	0	0	0
$V_{GS(off)}$	−12V	−8V	−6V
R_L	430Ω	700Ω	1100Ω
$I_{D(on)}$	6.6mA	4mA	2.5mA

NOTE: 1. Pulse test pulsewidth = 300 μs; duty cycle < 3%