



# PCU9955A

16-channel U<sup>F</sup>m 5 MHz I<sup>2</sup>C-bus 57 mA/20 V constant current LED driver

Rev. 3.1 — 29 June 2015

Product data sheet

## 1. General description

The PCU9955A is an Ultra Fast-mode (U<sup>F</sup>m) I<sup>2</sup>C-bus controlled 16-channel constant current LED driver optimized for dimming and blinking 57 mA Red/Green/Blue/Amber (RGBA) LEDs in amusement products. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 31.25 kHz with a duty cycle that is adjustable from 0 % to 100 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 122 Hz and an adjustable frequency between 15 Hz to once every 16.8 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCU9955A operates with a supply voltage range of 3 V to 5.5 V and the constant current sink LED outputs allow up to 20 V for the LED supply. The output peak current is adjustable with an 8-bit linear DAC from 225  $\mu$ A to 57 mA.

Gradation control for all current sources is achieved via the I<sup>2</sup>C-bus serial interface and allows user to ramp current automatically without MCU intervention. 8-bit DACs are available to adjust brightness levels for each LED current source. There are four selectable gradation control groups and each group has independently four registers to control ramp-up and ramp-down rate, step time, hold ON/OFF time and final hold ON output current. Two gradation operation modes are available for each group, one is single shot mode (output pattern once) and the other is continuous mode (output pattern repeat). Each channel can be set to either gradation mode or normal mode and assigned to any one of these four gradation control groups.

This device has built-in overtemperature detection circuitry. A thermal shutdown feature protects the device when internal junction temperature exceeds the limit allowed for the process.

The PCU9955A device is the first LED controller device in a new Ultra Fast-mode (U<sup>F</sup>m) I<sup>2</sup>C-bus family. U<sup>F</sup>m I<sup>2</sup>C-bus devices offer higher frequency (up to 5 MHz). The U<sup>F</sup>m I<sup>2</sup>C-bus slave devices operate in receive-only mode. That is, only I<sup>2</sup>C writes to the PCU9955A are supported. As such, there are no status registers in PCU9955A. The PCU9955A allows significantly higher data transfer rate compared to the Fast-mode Plus version (PCA9955A).

The active LOW output enable input pin ( $\overline{\text{OE}}$ ) blinks all the LED outputs and can be used to externally PWM the outputs, which is useful when multiple devices must be dimmed or blinked together without using software control.



Software programmable LED Group and three Sub Call I<sup>2</sup>C-bus addresses allow all or defined groups of PCU9955A devices to respond to a common I<sup>2</sup>C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I<sup>2</sup>C-bus commands. On power-up, PCU9955A has a unique Sub Call address to identify it as a 16-channel LED driver. This allows mixing of devices with different channel widths. Three hardware address pins on PCU9955A allow up to 125 devices on the same bus.

The Software Reset (SWRST) function allows the master to perform a reset of the PCU9955A through the I<sup>2</sup>C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the output current switches to be OFF (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

## 2. Features and benefits

- 16 LED drivers. Each output programmable at:
  - ◆ Off
  - ◆ On
  - ◆ Programmable LED brightness
  - ◆ Programmable group dimming/blinking mixed with individual LED brightness
  - ◆ Programmable LED output delay to reduce EMI and surge currents
- Gradation control for all channels
  - ◆ Each channel can assign to one of four gradation control groups
  - ◆ Programmable gradation time and rate for ramp-up and/or ramp-down operations
  - ◆ Programmable step time (6-bit) from 0.5 ms (minimum) to 512 ms (maximum)
  - ◆ Programmable hold-on time after ramp-up and hold-off time after ramp-down (3-bit) from 0 s to 6 s
  - ◆ Programmable final ramp-up and hold-on current
  - ◆ Programmable brightness current output adjustment, either linear or exponential curve
- 16 constant current output channels can sink up to 57 mA, tolerate up to 20 V when OFF
- Output current adjusted through an external resistor (REXT input)
- Output current accuracy
  - ◆ ±4 % between output channels
  - ◆ ±6 % between PCU9955A devices
- Thermal shutdown for overtemperature
- 5 MHz Ultra Fast-mode I<sup>2</sup>C-bus interface
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness fully ON using a 31.25 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 122 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 15 Hz to 16.8 s and duty cycle from 0 % to 99.6 %

- Output state change programmable on the Acknowledge (bit 9, this bit is always set to 1 by I<sup>2</sup>C-bus master) or the STOP condition to update outputs byte-by-byte or all at the same time (default to 'Change on STOP').
- Active LOW Output Enable ( $\overline{OE}$ ) input pin allows for hardware blinking and dimming of the LEDs
- Three quinary hardware address pins allow 125 PCU9955A devices to be connected to the same I<sup>2</sup>C-bus and to be individually programmed
- 4 software programmable I<sup>2</sup>C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for 'All Call' so that all the PCU9955As on the I<sup>2</sup>C-bus can be addressed at the same time and the second register used for three different addresses so that  $\frac{1}{3}$  of all devices on the bus can be addressed at the same time in a group). Software enable and disable for each programmable I<sup>2</sup>C-bus address.
- Unique power-up default Sub Call address allows mixing of devices with different channel widths
- Software Reset feature (SWRST Call) allows the device to be reset through the I<sup>2</sup>C-bus
- 8 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on USDA/USCL inputs
- No glitch on LEDn outputs on power-up
- Low standby current
- Operating power supply voltage ( $V_{DD}$ ) range of 3 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- -40 °C to +85 °C operation
- ESD protection exceeds 4000 V HBM per JESD22-A114
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: HTSSOP28

### 3. Applications

- Amusement products
- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices
- Fade-in and fade-out for breathlight control

## 4. Ordering information

Table 1. Ordering information

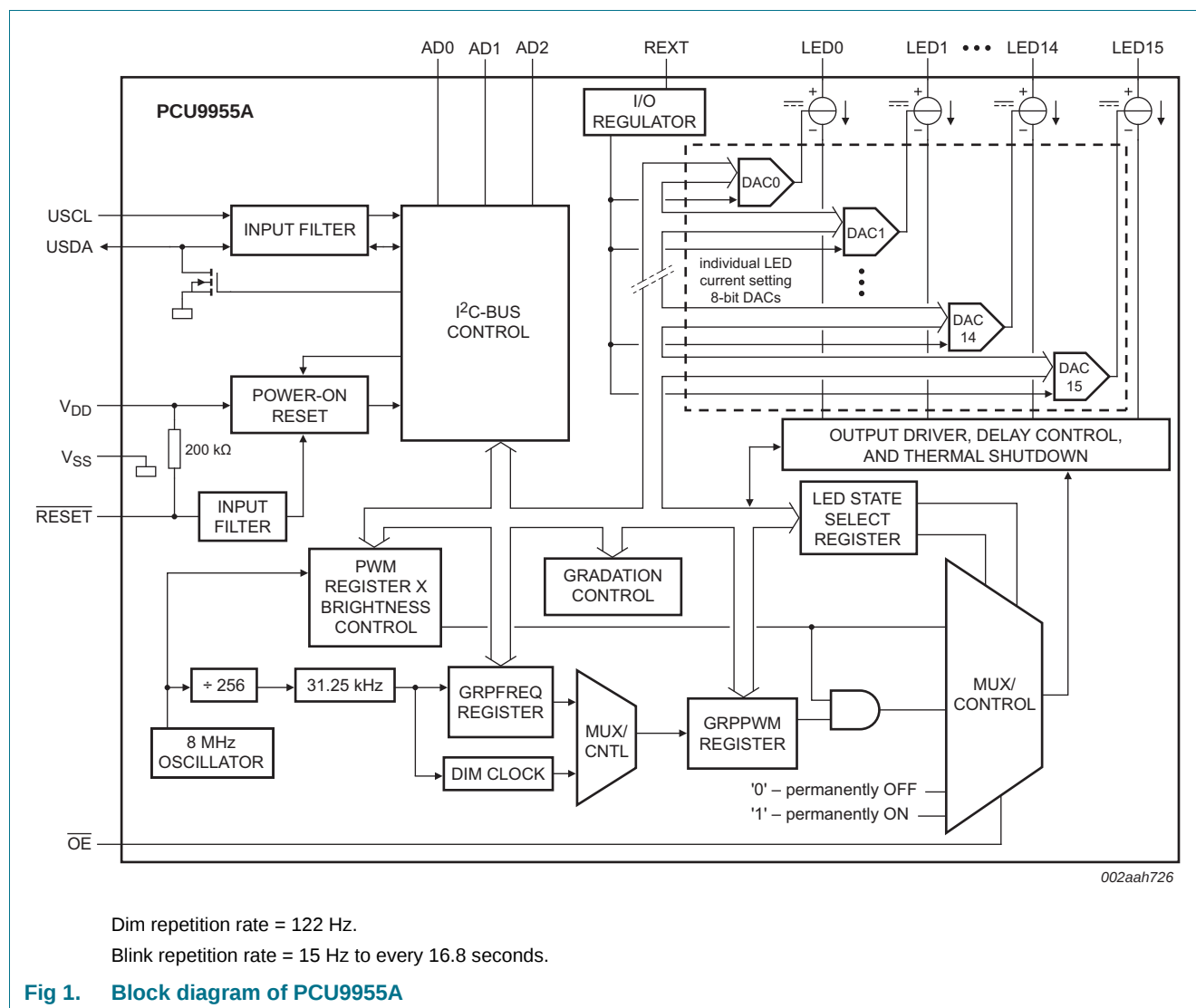
| Type number | Topside mark | Package  |                                                                                                                              |           |
|-------------|--------------|----------|------------------------------------------------------------------------------------------------------------------------------|-----------|
|             |              | Name     | Description                                                                                                                  | Version   |
| PCU9955ATW  | PCU9955ATW   | HTSSOP28 | plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad | SOT1172-3 |

### 4.1 Ordering options

Table 2. Ordering options

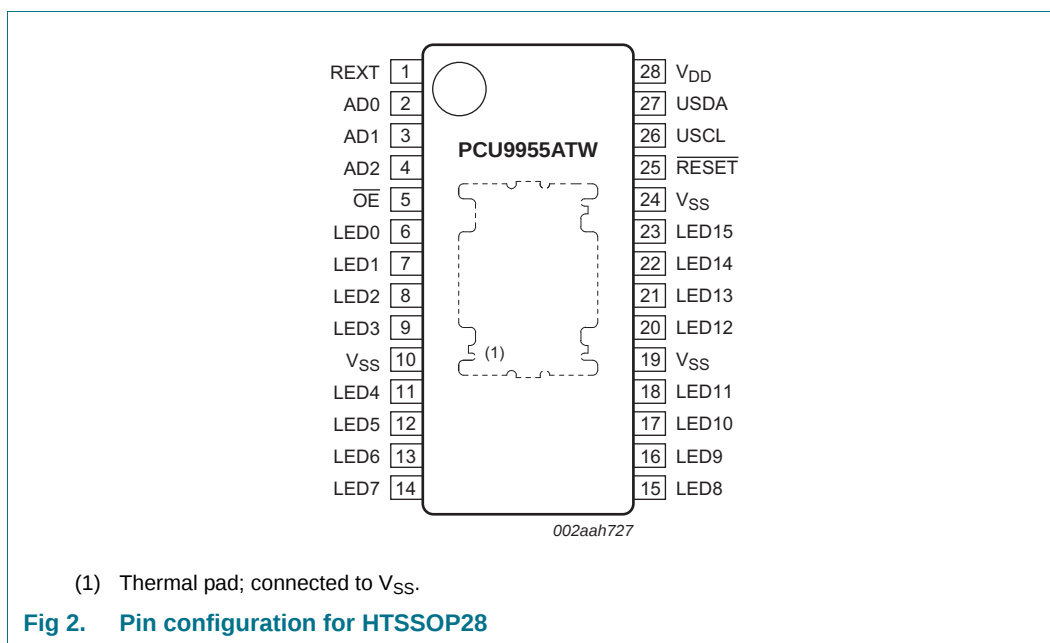
| Type number | Orderable part number | Package  | Packing method                       | Minimum order quantity | Temperature                         |
|-------------|-----------------------|----------|--------------------------------------|------------------------|-------------------------------------|
| PCU9955ATW  | PCU9955ATWJ           | HTSSOP28 | Reel 13" Q1/T1<br>*Standard mark SMD | 2500                   | T <sub>amb</sub> = -40 °C to +85 °C |

## 5. Block diagram



## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3. Pin description

| Symbol | Pin | Type | Description                                    |
|--------|-----|------|------------------------------------------------|
| REXT   | 1   | I    | current set resistor input; resistor to ground |
| AD0    | 2   | I    | address input 0                                |
| AD1    | 3   | I    | address input 1                                |
| AD2    | 4   | I    | address input 2                                |
| OE     | 5   | I    | active LOW output enable for LEDs              |
| LED0   | 6   | O    | LED driver 0                                   |
| LED1   | 7   | O    | LED driver 1                                   |
| LED2   | 8   | O    | LED driver 2                                   |
| LED3   | 9   | O    | LED driver 3                                   |
| LED4   | 11  | O    | LED driver 4                                   |
| LED5   | 12  | O    | LED driver 5                                   |
| LED6   | 13  | O    | LED driver 6                                   |
| LED7   | 14  | O    | LED driver 7                                   |
| LED8   | 15  | O    | LED driver 8                                   |
| LED9   | 16  | O    | LED driver 9                                   |
| LED10  | 17  | O    | LED driver 10                                  |
| LED11  | 18  | O    | LED driver 11                                  |
| LED12  | 20  | O    | LED driver 12                                  |

Table 3. Pin description ...continued

| Symbol          | Pin            | Type         | Description                        |
|-----------------|----------------|--------------|------------------------------------|
| LED13           | 21             | O            | LED driver 13                      |
| LED14           | 22             | O            | LED driver 14                      |
| LED15           | 23             | O            | LED driver 15                      |
| RESET           | 25             | I            | active LOW reset input             |
| USCL            | 26             | I            | U <sup>2</sup> C serial clock line |
| USDA            | 27             | I/O          | U <sup>2</sup> C serial data line  |
| V <sub>SS</sub> | 10, 19, 24 [1] | ground       | supply ground                      |
| V <sub>DD</sub> | 28             | power supply | supply voltage                     |

[1] HTSSOP28 package supply ground is connected to both V<sub>SS</sub> pins and exposed center pad. V<sub>SS</sub> pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias must be incorporated in the printed-circuit board in the thermal pad region.

## 7. Functional description

Refer to [Figure 1 “Block diagram of PCU9955A”](#).

### 7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

For PCU9955A there are a maximum of 125 possible programmable addresses using the three quinary hardware address pins.

#### 7.1.1 Regular I<sup>2</sup>C-bus slave address

The I<sup>2</sup>C-bus slave address of the PCU9955A is shown in [Figure 3](#). The 7-bit slave address is determined by the quinary input pads AD0, AD1 and AD2. Each pad can have one of five states (GND, pull-up, floating, pull-down, and V<sub>DD</sub>) based on how the input pad is connected on the board. At power-up or hardware/software reset, the quinary input pads are sampled and set the slave address of the device internally. To conserve power, once the slave address is determined, the quinary input pads are turned off and will not be sampled until the next time the device is power cycled. [Table 4](#) lists the five possible connections for the quinary input pads along with the external resistor values that must be used.

Table 4. Quinary input pad connection

| Pad connection<br>(pins AD2, AD1, AD0)[1] | Mnemonic        | External resistor (kΩ) |      |
|-------------------------------------------|-----------------|------------------------|------|
|                                           |                 | Min.                   | Max. |
| tie to ground                             | GND             | 0                      | 17.9 |
| resistor pull-down to ground              | PD              | 34.8                   | 270  |
| open (floating)                           | FLT             | 503                    | ∞    |
| resistor pull-up to V <sub>DD</sub>       | PU              | 31.7                   | 340  |
| tie to V <sub>DD</sub>                    | V <sub>DD</sub> | 0                      | 22.1 |

[1] These AD[2:0] inputs must be stable before the supply V<sub>DD</sub> to the chip.

[Table 5](#) lists all 125 possible slave addresses of the device based on all combinations of the five states connected to three address input pins AD0, AD1 and AD2.

**Table 5. I<sup>2</sup>C-bus slave address**

| Hardware selectable input pins |                 |                 | I <sup>2</sup> C-bus slave address for PCU9955A |             |                        |                   |
|--------------------------------|-----------------|-----------------|-------------------------------------------------|-------------|------------------------|-------------------|
| AD2                            | AD1             | AD0             | Decimal                                         | Hexadecimal | Binary (A[6:0])        | Address (R/W = 0) |
| GND                            | GND             | GND             | 1                                               | 01          | 0000001 <sup>[1]</sup> | 02h               |
| GND                            | GND             | PD              | 2                                               | 02          | 0000010 <sup>[1]</sup> | 04h               |
| GND                            | GND             | FLT             | 3                                               | 03          | 0000011 <sup>[1]</sup> | 06h               |
| GND                            | GND             | PU              | 4                                               | 04          | 0000100 <sup>[1]</sup> | 08h               |
| GND                            | GND             | V <sub>DD</sub> | 5                                               | 05          | 0000101 <sup>[1]</sup> | 0Ah               |
| GND                            | PD              | GND             | 6                                               | 06          | 0000110 <sup>[1]</sup> | 0Ch               |
| GND                            | PD              | PD              | 7                                               | 07          | 0000111 <sup>[1]</sup> | 0Eh               |
| GND                            | PD              | FLT             | 8                                               | 08          | 0001000                | 10h               |
| GND                            | PD              | PU              | 9                                               | 09          | 0001001                | 12h               |
| GND                            | PD              | V <sub>DD</sub> | 10                                              | 0A          | 0001010                | 14h               |
| GND                            | FLT             | GND             | 11                                              | 0B          | 0001011                | 16h               |
| GND                            | FLT             | PD              | 12                                              | 0C          | 0001100                | 18h               |
| GND                            | FLT             | FLT             | 13                                              | 0D          | 0001101                | 1Ah               |
| GND                            | FLT             | PU              | 14                                              | 0E          | 0001110                | 1Ch               |
| GND                            | FLT             | V <sub>DD</sub> | 15                                              | 0F          | 0001111                | 1Eh               |
| GND                            | PU              | GND             | 16                                              | 10          | 0010000                | 20h               |
| GND                            | PU              | PD              | 17                                              | 11          | 0010001                | 22h               |
| GND                            | PU              | FLT             | 18                                              | 12          | 0010010                | 24h               |
| GND                            | PU              | PU              | 19                                              | 13          | 0010011                | 26h               |
| GND                            | PU              | V <sub>DD</sub> | 20                                              | 14          | 0010100                | 28h               |
| GND                            | V <sub>DD</sub> | GND             | 21                                              | 15          | 0010101                | 2Ah               |
| GND                            | V <sub>DD</sub> | PD              | 22                                              | 16          | 0010110                | 2Ch               |
| GND                            | V <sub>DD</sub> | FLT             | 23                                              | 17          | 0010111                | 2Eh               |
| GND                            | V <sub>DD</sub> | PU              | 24                                              | 18          | 0011000                | 30h               |
| GND                            | V <sub>DD</sub> | V <sub>DD</sub> | 25                                              | 19          | 0011001                | 32h               |
| PD                             | GND             | GND             | 26                                              | 1A          | 0011010                | 34h               |
| PD                             | GND             | PD              | 27                                              | 1B          | 0011011                | 36h               |
| PD                             | GND             | FLT             | 28                                              | 1C          | 0011100                | 38h               |
| PD                             | GND             | PU              | 29                                              | 1D          | 0011101                | 3Ah               |
| PD                             | GND             | V <sub>DD</sub> | 30                                              | 1E          | 0011110                | 3Ch               |
| PD                             | PD              | GND             | 31                                              | 1F          | 0011111                | 3Eh               |
| PD                             | PD              | PD              | 32                                              | 20          | 0100000                | 40h               |
| PD                             | PD              | FLT             | 33                                              | 21          | 0100001                | 42h               |
| PD                             | PD              | PU              | 34                                              | 22          | 0100010                | 44h               |
| PD                             | PD              | V <sub>DD</sub> | 35                                              | 23          | 0100011                | 46h               |
| PD                             | FLT             | GND             | 36                                              | 24          | 0100100                | 48h               |
| PD                             | FLT             | PD              | 37                                              | 25          | 0100101                | 4Ah               |
| PD                             | FLT             | FLT             | 38                                              | 26          | 0100110                | 4Ch               |

Table 5. I<sup>2</sup>C-bus slave address ...continued

| Hardware selectable input pins |                 |                 | I <sup>2</sup> C-bus slave address for PCU9955A |             |                 |                   |
|--------------------------------|-----------------|-----------------|-------------------------------------------------|-------------|-----------------|-------------------|
| AD2                            | AD1             | AD0             | Decimal                                         | Hexadecimal | Binary (A[6:0]) | Address (R/W = 0) |
| PD                             | FLT             | PU              | 39                                              | 27          | 0100111         | 4Eh               |
| PD                             | FLT             | V <sub>DD</sub> | 40                                              | 28          | 0101000         | 50h               |
| PD                             | PU              | GND             | 41                                              | 29          | 0101001         | 52h               |
| PD                             | PU              | PD              | 42                                              | 2A          | 0101010         | 54h               |
| PD                             | PU              | FLT             | 43                                              | 2B          | 0101011         | 56h               |
| PD                             | PU              | PU              | 44                                              | 2C          | 0101100         | 58h               |
| PD                             | PU              | V <sub>DD</sub> | 45                                              | 2D          | 0101101         | 5Ah               |
| PD                             | V <sub>DD</sub> | GND             | 46                                              | 2E          | 0101110         | 5Ch               |
| PD                             | V <sub>DD</sub> | PD              | 47                                              | 2F          | 0101111         | 5Eh               |
| PD                             | V <sub>DD</sub> | FLT             | 48                                              | 30          | 0110000         | 60h               |
| PD                             | V <sub>DD</sub> | PU              | 49                                              | 31          | 0110001         | 62h               |
| PD                             | V <sub>DD</sub> | V <sub>DD</sub> | 50                                              | 32          | 0110010         | 64h               |
| FLT                            | GND             | GND             | 51                                              | 33          | 0110011         | 66h               |
| FLT                            | GND             | PD              | 52                                              | 34          | 0110100         | 68h               |
| FLT                            | GND             | FLT             | 53                                              | 35          | 0110101         | 6Ah               |
| FLT                            | GND             | PU              | 54                                              | 36          | 0110110         | 6Ch               |
| FLT                            | GND             | V <sub>DD</sub> | 55                                              | 37          | 0110111         | 6Eh               |
| FLT                            | PD              | GND             | 56                                              | 38          | 0111000         | 70h               |
| FLT                            | PD              | PD              | 57                                              | 39          | 0111001         | 72h               |
| FLT                            | PD              | FLT             | 58                                              | 3A          | 0111010         | 74h               |
| FLT                            | PD              | PU              | 59                                              | 3B          | 0111011         | 76h               |
| FLT                            | PD              | V <sub>DD</sub> | 60                                              | 3C          | 0111100         | 78h               |
| FLT                            | FLT             | GND             | 61                                              | 3D          | 0111101         | 7Ah               |
| FLT                            | FLT             | PD              | 62                                              | 3E          | 0111110         | 7Ch               |
| FLT                            | FLT             | FLT             | 63                                              | 3F          | 0111111         | 7Eh               |
| FLT                            | FLT             | PU              | 64                                              | 40          | 1000000         | 80h               |
| FLT                            | FLT             | V <sub>DD</sub> | 65                                              | 41          | 1000001         | 82h               |
| FLT                            | PU              | GND             | 66                                              | 42          | 1000010         | 84h               |
| FLT                            | PU              | PD              | 67                                              | 43          | 1000011         | 86h               |
| FLT                            | PU              | FLT             | 68                                              | 44          | 1000100         | 88h               |
| FLT                            | PU              | PU              | 69                                              | 45          | 1000101         | 8Ah               |
| FLT                            | PU              | V <sub>DD</sub> | 70                                              | 46          | 1000110         | 8Ch               |
| FLT                            | V <sub>DD</sub> | GND             | 71                                              | 47          | 1000111         | 8Eh               |
| FLT                            | V <sub>DD</sub> | PD              | 72                                              | 48          | 1001000         | 90h               |
| FLT                            | V <sub>DD</sub> | FLT             | 73                                              | 49          | 1001001         | 92h               |
| FLT                            | V <sub>DD</sub> | PU              | 74                                              | 4A          | 1001010         | 94h               |
| FLT                            | V <sub>DD</sub> | V <sub>DD</sub> | 75                                              | 4B          | 1001011         | 96h               |
| PU                             | GND             | GND             | 76                                              | 4C          | 1001100         | 98h               |
| PU                             | GND             | PD              | 77                                              | 4D          | 1001101         | 9Ah               |
| PU                             | GND             | FLT             | 78                                              | 4E          | 1001110         | 9Ch               |

Table 5. I<sup>2</sup>C-bus slave address ...continued

| Hardware selectable input pins |                 |                 | I <sup>2</sup> C-bus slave address for PCU9955A |             |                 |                   |
|--------------------------------|-----------------|-----------------|-------------------------------------------------|-------------|-----------------|-------------------|
| AD2                            | AD1             | AD0             | Decimal                                         | Hexadecimal | Binary (A[6:0]) | Address (R/W = 0) |
| PU                             | GND             | PU              | 79                                              | 4F          | 1001111         | 9Eh               |
| PU                             | GND             | V <sub>DD</sub> | 80                                              | 50          | 1010000         | A0h               |
| PU                             | PD              | GND             | 81                                              | 51          | 1010001         | A2h               |
| PU                             | PD              | PD              | 82                                              | 52          | 1010010         | A4h               |
| PU                             | PD              | FLT             | 83                                              | 53          | 1010011         | A6h               |
| PU                             | PD              | PU              | 84                                              | 54          | 1010100         | A8h               |
| PU                             | PD              | V <sub>DD</sub> | 85                                              | 55          | 1010101         | AAh               |
| PU                             | FLT             | GND             | 86                                              | 56          | 1010110         | ACH               |
| PU                             | FLT             | PD              | 87                                              | 57          | 1010111         | AEnh              |
| PU                             | FLT             | FLT             | 88                                              | 58          | 1011000         | B0h               |
| PU                             | FLT             | PU              | 89                                              | 59          | 1011001         | B2h               |
| PU                             | FLT             | V <sub>DD</sub> | 90                                              | 5A          | 1011010         | B4h               |
| PU                             | PU              | GND             | 91                                              | 5B          | 1011011         | B6h               |
| PU                             | PU              | PD              | 92                                              | 5C          | 1011100         | B8h               |
| PU                             | PU              | FLT             | 93                                              | 5D          | 1011101         | BAh               |
| PU                             | PU              | PU              | 94                                              | 5E          | 1011110         | BCh               |
| PU                             | PU              | V <sub>DD</sub> | 95                                              | 5F          | 1011111         | BEh               |
| PU                             | V <sub>DD</sub> | GND             | 96                                              | 60          | 1100000         | C0h               |
| PU                             | V <sub>DD</sub> | PD              | 97                                              | 61          | 1100001         | C2h               |
| PU                             | V <sub>DD</sub> | FLT             | 98                                              | 62          | 1100010         | C4h               |
| PU                             | V <sub>DD</sub> | PU              | 99                                              | 63          | 1100011         | C6h               |
| PU                             | V <sub>DD</sub> | V <sub>DD</sub> | 100                                             | 64          | 1100100         | C8h               |
| V <sub>DD</sub>                | GND             | GND             | 101                                             | 65          | 1100101         | CAh               |
| V <sub>DD</sub>                | GND             | PD              | 102                                             | 66          | 1100110         | CCh               |
| V <sub>DD</sub>                | GND             | FLT             | 103                                             | 67          | 1100111         | CEh               |
| V <sub>DD</sub>                | GND             | PU              | 104                                             | 68          | 1101000         | D0h               |
| V <sub>DD</sub>                | GND             | V <sub>DD</sub> | 105                                             | 69          | 1101001         | D2h               |
| V <sub>DD</sub>                | PD              | GND             | 106                                             | 6A          | 1101010         | D4h               |
| V <sub>DD</sub>                | PD              | PD              | 107                                             | 6B          | 1101011         | D6h               |
| V <sub>DD</sub>                | PD              | FLT             | 108                                             | 6C          | 1101100         | D8h               |
| V <sub>DD</sub>                | PD              | PU              | 109                                             | 6D          | 1101101         | DAh               |
| V <sub>DD</sub>                | PD              | V <sub>DD</sub> | 110                                             | 6E          | 1101110         | DCh               |
| V <sub>DD</sub>                | FLT             | GND             | 111                                             | 6F          | 1101111         | DEh               |
| V <sub>DD</sub>                | FLT             | PD              | 112                                             | 70          | 1110000         | E0h               |
| V <sub>DD</sub>                | FLT             | FLT             | 113                                             | 71          | 1110001         | E2h               |
| V <sub>DD</sub>                | FLT             | PU              | 114                                             | 72          | 1110010         | E4h               |
| V <sub>DD</sub>                | FLT             | V <sub>DD</sub> | 115                                             | 73          | 1110011         | E6h               |
| V <sub>DD</sub>                | PU              | GND             | 116                                             | 74          | 1110100         | E8h               |
| V <sub>DD</sub>                | PU              | PD              | 117                                             | 75          | 1110101         | EAh               |
| V <sub>DD</sub>                | PU              | FLT             | 118                                             | 76          | 1110110         | ECh               |

Table 5. I<sup>2</sup>C-bus slave address ...continued

| Hardware selectable input pins |                 |                 | I <sup>2</sup> C-bus slave address for PCU9955A |             |                        |                   |
|--------------------------------|-----------------|-----------------|-------------------------------------------------|-------------|------------------------|-------------------|
| AD2                            | AD1             | AD0             | Decimal                                         | Hexadecimal | Binary (A[6:0])        | Address (R/W = 0) |
| V <sub>DD</sub>                | PU              | PU              | 119                                             | 77          | 1110111                | EEh               |
| V <sub>DD</sub>                | PU              | V <sub>DD</sub> | 120                                             | 78          | 1111000 <sup>[1]</sup> | F0h               |
| V <sub>DD</sub>                | V <sub>DD</sub> | GND             | 121                                             | 79          | 1111001 <sup>[1]</sup> | F2h               |
| V <sub>DD</sub>                | V <sub>DD</sub> | PD              | 122                                             | 7A          | 1111010 <sup>[1]</sup> | F4h               |
| V <sub>DD</sub>                | V <sub>DD</sub> | FLT             | 123                                             | 7B          | 1111011 <sup>[1]</sup> | F6h               |
| V <sub>DD</sub>                | V <sub>DD</sub> | PU              | 124                                             | 7C          | 1111100 <sup>[1]</sup> | F8h               |
| V <sub>DD</sub>                | V <sub>DD</sub> | V <sub>DD</sub> | 125                                             | 7D          | 1111101 <sup>[1]</sup> | FAh               |

[1] See 'Remark' below.

**Remark:** Reserved I<sup>2</sup>C-bus addresses must be used with caution since they can interfere with:

- 'reserved for future use' I<sup>2</sup>C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)

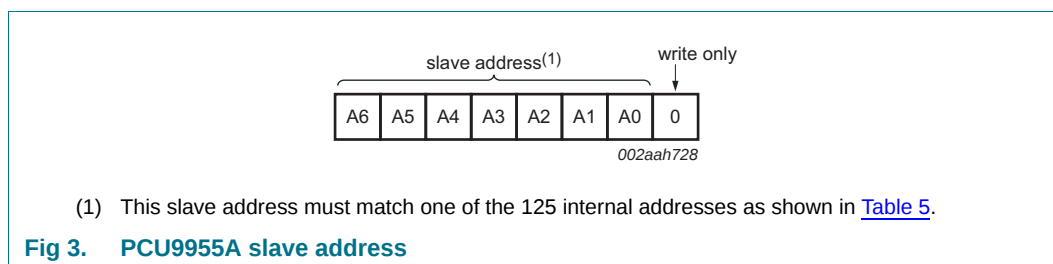


Fig 3. PCU9955A slave address

The last bit of the address byte defines the operation to be performed. Only writes to PCU9955A are supported, therefore the last bit is set to 0. No read available with UfM I<sup>2</sup>C-bus.

### 7.1.2 LED All Call I<sup>2</sup>C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000X
- Programmable through I<sup>2</sup>C-bus (volatile programming)
- At power-up, LED All Call I<sup>2</sup>C-bus address is enabled

See [Section 7.3.11 "ALLCALLADR, LED All Call I<sup>2</sup>C-bus address"](#) for more detail.

**Remark:** The default LED All Call I<sup>2</sup>C-bus address (E0h or 1110 000X) must not be used as a regular I<sup>2</sup>C-bus slave address since this address is enabled at power-up. All of the PCU9955As on the I<sup>2</sup>C-bus recognize the address if sent by the I<sup>2</sup>C-bus master.

### 7.1.3 LED Sub Call I<sup>2</sup>C-bus addresses

- 3 different I<sup>2</sup>C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: ECh or 1110 110X
  - SUBADR2 register: ECh or 1110 110X
  - SUBADR3 register: ECh or 1110 110X
- Programmable through I<sup>2</sup>C-bus (volatile programming)
- At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 I<sup>2</sup>C-bus addresses are disabled.

**Remark:** At power-up SUBADR1 identifies this device as a 16-channel driver.

See [Section 7.3.10 “LED Sub Call I<sup>2</sup>C-bus addresses for PCU9955A”](#) for more detail.

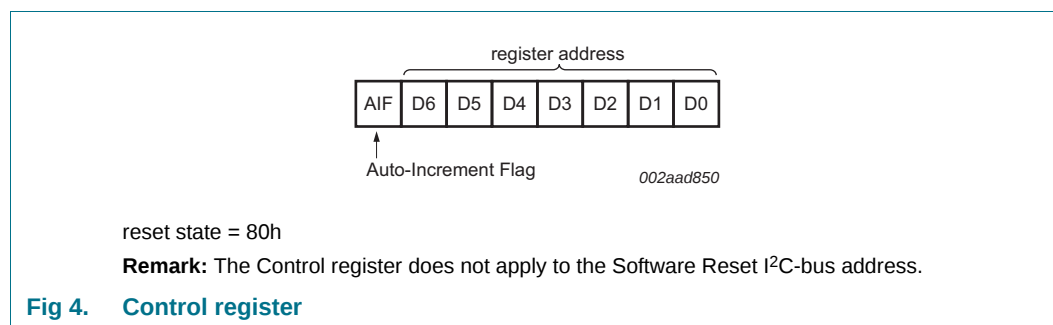
**Remark:** The default LED Sub Call I<sup>2</sup>C-bus addresses may be used as regular I<sup>2</sup>C-bus slave addresses as long as they are disabled.

## 7.2 Control register

Following the slave address, LED All Call address or LED Sub Call address, the bus master sends a byte to the PCU9955A, which is stored in the Control register.

The lowest 7 bits are used as a pointer to determine which register is accessed (D[6:0]). The highest bit is used as Auto-Increment Flag (AIF).

This bit along with the MODE1 register bit 5 and bit 6 provide the Auto-Increment feature.



When the Auto-Increment Flag is set (AIF = logic 1), the seven low-order bits of the Control register are automatically incremented after a write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values of MODE1 register.

Table 6. Auto-Increment options

| AIF | AI1 <sup>[1]</sup> | AI0 <sup>[1]</sup> | Function                                                                                                                                                         |
|-----|--------------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | 0                  | 0                  | no Auto-Increment                                                                                                                                                |
| 1   | 0                  | 0                  | Auto-Increment for registers (00h to 43h). D[6:0] roll over to 00h after the last register 43h is accessed.                                                      |
| 1   | 0                  | 1                  | Auto-Increment for individual brightness registers only (08h to 17h). D[6:0] roll over to 08h after the last register (17h) is accessed.                         |
| 1   | 1                  | 0                  | Auto-Increment for MODE1 to IREF15 control registers (00h to 27h). D[6:0] roll over to 00h after the last register (27h) is accessed.                            |
| 1   | 1                  | 1                  | Auto-Increment for global control registers and individual brightness registers (06h to 17h). D[6:0] roll over to 06h after the last register (17h) is accessed. |

[1] AI1 and AI0 come from MODE1 register.

**Remark:** Other combinations not shown in [Table 6](#) (AIF + AI[1:0] = 001b, 010b and 011b) are reserved and must not be used for proper device operation.

AIF + AI[1:0] = 000b is used when the same register must be accessed several times during a single I<sup>2</sup>C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AIF + AI[1:0] = 100b is used when all the registers must be sequentially accessed, for example, power-up programming.

AIF + AI[1:0] = 101b is used when the 16 LED drivers must be individually programmed with different values during the same I<sup>2</sup>C-bus communication, for example, changing color setting to another color setting.

AIF + AI[1:0] = 110b is used when MODE1 to IREF15 registers must be programmed with different settings during the same I<sup>2</sup>C-bus communication.

AIF + AI[1:0] = 111b is used when the 16 LED drivers must be individually programmed with different values in addition to global programming.

Only the 7 least significant bits D[6:0] are affected by the AIF, AI1 and AI0 bits.

When the Control register is written, the register entry point determined by D[6:0] is the first register that is addressed (write operation), and can be anywhere between 00h and 49h (as defined in [Table 7](#)). When AIF = 1, the Auto-Increment Flag is set and the rollover value at which the register increment stops and goes to the next one is determined by AIF, AI1 and AI0. See [Table 6](#) for rollover values. For example, if MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1001 0000, then the register addressing sequence is (in hexadecimal):  
 10 → 11 → ... → 17 → 08 → 09 → ... → 17 → 08 → 09 → ... as long as the master keeps sending data.

If MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1010 0010, then the register addressing sequence is (in hexadecimal):  
 22 → 23 → ... → 43 → 00 → 01 → ... → 17 → 08 → 09 → ... as long as the master keeps sending data.

If MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1000 0101, then the register addressing sequence is (in hexadecimal):

05 → 06 → ... → 17 → 08 → 09 → ... → 17 → 08 → 09 → ... as long as the master keeps sending data.

**Remark:** Writing to registers marked 'not used' are ignored.

### 7.3 Register definitions

**Table 7. Register summary**

| Register number (hexadecimal) | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Name    | Type       | Function                       |
|-------------------------------|----|----|----|----|----|----|----|---------|------------|--------------------------------|
| 00h                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | MODE1   | write only | Mode register 1                |
| 01h                           | 0  | 0  | 0  | 0  | 0  | 0  | 1  | MODE2   | write only | Mode register 2                |
| 02h                           | 0  | 0  | 0  | 0  | 0  | 1  | 0  | LEDOUT0 | write only | LED output state 0             |
| 03h                           | 0  | 0  | 0  | 0  | 0  | 1  | 1  | LEDOUT1 | write only | LED output state 1             |
| 04h                           | 0  | 0  | 0  | 0  | 1  | 0  | 0  | LEDOUT2 | write only | LED output state 2             |
| 05h                           | 0  | 0  | 0  | 0  | 1  | 0  | 1  | LEDOUT3 | write only | LED output state 3             |
| 06h                           | 0  | 0  | 0  | 0  | 1  | 1  | 0  | GRPPWM  | write only | group duty cycle control       |
| 07h                           | 0  | 0  | 0  | 0  | 1  | 1  | 1  | GRPFREQ | write only | group frequency                |
| 08h                           | 0  | 0  | 0  | 1  | 0  | 0  | 0  | PWM0    | write only | brightness control LED0        |
| 09h                           | 0  | 0  | 0  | 1  | 0  | 0  | 1  | PWM1    | write only | brightness control LED1        |
| 0Ah                           | 0  | 0  | 0  | 1  | 0  | 1  | 0  | PWM2    | write only | brightness control LED2        |
| 0Bh                           | 0  | 0  | 0  | 1  | 0  | 1  | 1  | PWM3    | write only | brightness control LED3        |
| 0Ch                           | 0  | 0  | 0  | 1  | 1  | 0  | 0  | PWM4    | write only | brightness control LED4        |
| 0Dh                           | 0  | 0  | 0  | 1  | 1  | 0  | 1  | PWM5    | write only | brightness control LED5        |
| 0Eh                           | 0  | 0  | 0  | 1  | 1  | 1  | 0  | PWM6    | write only | brightness control LED6        |
| 0Fh                           | 0  | 0  | 0  | 1  | 1  | 1  | 1  | PWM7    | write only | brightness control LED7        |
| 10h                           | 0  | 0  | 1  | 0  | 0  | 0  | 0  | PWM8    | write only | brightness control LED8        |
| 11h                           | 0  | 0  | 1  | 0  | 0  | 0  | 1  | PWM9    | write only | brightness control LED9        |
| 12h                           | 0  | 0  | 1  | 0  | 0  | 1  | 0  | PWM10   | write only | brightness control LED10       |
| 13h                           | 0  | 0  | 1  | 0  | 0  | 1  | 1  | PWM11   | write only | brightness control LED11       |
| 14h                           | 0  | 0  | 1  | 0  | 1  | 0  | 0  | PWM12   | write only | brightness control LED12       |
| 15h                           | 0  | 0  | 1  | 0  | 1  | 0  | 1  | PWM13   | write only | brightness control LED13       |
| 16h                           | 0  | 0  | 1  | 0  | 1  | 1  | 0  | PWM14   | write only | brightness control LED14       |
| 17h                           | 0  | 0  | 1  | 0  | 1  | 1  | 1  | PWM15   | write only | brightness control LED15       |
| 18h                           | 0  | 0  | 1  | 1  | 0  | 0  | 0  | IREF0   | write only | output gain control register 0 |
| 19h                           | 0  | 0  | 1  | 1  | 0  | 0  | 1  | IREF1   | write only | output gain control register 1 |
| 1Ah                           | 0  | 0  | 1  | 1  | 0  | 1  | 0  | IREF2   | write only | output gain control register 2 |
| 1Bh                           | 0  | 0  | 1  | 1  | 0  | 1  | 1  | IREF3   | write only | output gain control register 3 |
| 1Ch                           | 0  | 0  | 1  | 1  | 1  | 0  | 0  | IREF4   | write only | output gain control register 4 |
| 1Dh                           | 0  | 0  | 1  | 1  | 1  | 0  | 1  | IREF5   | write only | output gain control register 5 |
| 1Eh                           | 0  | 0  | 1  | 1  | 1  | 1  | 0  | IREF6   | write only | output gain control register 6 |
| 1Fh                           | 0  | 0  | 1  | 1  | 1  | 1  | 1  | IREF7   | write only | output gain control register 7 |

Table 7. Register summary ...continued

| Register number (hexadecimal) | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Name           | Type       | Function                                                   |
|-------------------------------|----|----|----|----|----|----|----|----------------|------------|------------------------------------------------------------|
| 20h                           | 0  | 1  | 0  | 0  | 0  | 0  | 0  | IREF8          | write only | output gain control register 8                             |
| 21h                           | 0  | 1  | 0  | 0  | 0  | 0  | 1  | IREF9          | write only | output gain control register 9                             |
| 22h                           | 0  | 1  | 0  | 0  | 0  | 1  | 0  | IREF10         | write only | output gain control register 10                            |
| 23h                           | 0  | 1  | 0  | 0  | 0  | 1  | 1  | IREF11         | write only | output gain control register 11                            |
| 24h                           | 0  | 1  | 0  | 0  | 1  | 0  | 0  | IREF12         | write only | output gain control register 12                            |
| 25h                           | 0  | 1  | 0  | 0  | 1  | 0  | 1  | IREF13         | write only | output gain control register 13                            |
| 26h                           | 0  | 1  | 0  | 0  | 1  | 1  | 0  | IREF14         | write only | output gain control register 14                            |
| 27h                           | 0  | 1  | 0  | 0  | 1  | 1  | 1  | IREF15         | write only | output gain control register 15                            |
| 28h                           | 0  | 1  | 0  | 1  | 0  | 0  | 0  | RAMP_RATE_GRP0 | write only | ramp enable and rate control for group 0                   |
| 29h                           | 0  | 1  | 0  | 1  | 0  | 0  | 1  | STEP_TIME_GRP0 | write only | step time control for group 0                              |
| 2Ah                           | 0  | 1  | 0  | 1  | 0  | 1  | 0  | HOLD_CNTL_GRP0 | write only | hold ON/OFF time control for group 0                       |
| 2Bh                           | 0  | 1  | 0  | 1  | 0  | 1  | 1  | IREF_GRP0      | write only | output gain control for group 0                            |
| 2Ch                           | 0  | 1  | 0  | 1  | 1  | 0  | 0  | RAMP_RATE_GRP1 | write only | ramp enable and rate control for group 1                   |
| 2Dh                           | 0  | 1  | 0  | 1  | 1  | 0  | 1  | STEP_TIME_GRP1 | write only | step time control for group 1                              |
| 2Eh                           | 0  | 1  | 0  | 1  | 1  | 1  | 0  | HOLD_CNTL_GRP1 | write only | hold ON/OFF time control for group 1                       |
| 2Fh                           | 0  | 1  | 0  | 1  | 1  | 1  | 1  | IREF_GRP1      | write only | output gain control for group 1                            |
| 30h                           | 0  | 1  | 1  | 0  | 0  | 0  | 0  | RAMP_RATE_GRP2 | write only | ramp enable and rate control for group 2                   |
| 31h                           | 0  | 1  | 1  | 0  | 0  | 0  | 1  | STEP_TIME_GRP2 | write only | step time control for group 2                              |
| 32h                           | 0  | 1  | 1  | 0  | 0  | 1  | 0  | HOLD_CNTL_GRP2 | write only | hold ON/OFF time control for group 2                       |
| 33h                           | 0  | 1  | 1  | 0  | 0  | 1  | 1  | IREF_GRP2      | write only | output gain control for group 2                            |
| 34h                           | 0  | 1  | 1  | 0  | 1  | 0  | 0  | RAMP_RATE_GRP3 | write only | ramp enable and rate control for group 3                   |
| 35h                           | 0  | 1  | 1  | 0  | 1  | 0  | 1  | STEP_TIME_GRP3 | write only | step time control for group 3                              |
| 36h                           | 0  | 1  | 1  | 0  | 1  | 1  | 0  | HOLD_CNTL_GRP3 | write only | hold ON/OFF time control for group 3                       |
| 37h                           | 0  | 1  | 1  | 0  | 1  | 1  | 1  | IREF_GRP3      | write only | output gain control for group 3                            |
| 38h                           | 0  | 1  | 1  | 1  | 0  | 0  | 0  | GRAD_MODE_SEL0 | write only | gradation mode select register for channel 7 to channel 0  |
| 39h                           | 0  | 1  | 1  | 1  | 0  | 0  | 1  | GRAD_MODE_SEL1 | write only | gradation mode select register for channel 15 to channel 8 |
| 3Ah                           | 0  | 1  | 1  | 1  | 0  | 1  | 0  | GRAD_GRP_SEL0  | write only | gradation group select for channel 3 to channel 0          |
| 3Bh                           | 0  | 1  | 1  | 1  | 0  | 1  | 1  | GRAD_GRP_SEL1  | write only | gradation group select for channel 7 to channel 4          |
| 3Ch                           | 0  | 1  | 1  | 1  | 1  | 0  | 0  | GRAD_GRP_SEL2  | write only | gradation group select for channel 11 to channel 8         |

Table 7. Register summary ...continued

| Register number (hexadecimal) | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Name          | Type       | Function                                              |
|-------------------------------|----|----|----|----|----|----|----|---------------|------------|-------------------------------------------------------|
| 3Dh                           | 0  | 1  | 1  | 1  | 1  | 0  | 1  | GRAD_GRP_SEL3 | write only | gradation group select for channel 15 to channel 12   |
| 3Eh                           | 0  | 1  | 1  | 1  | 1  | 1  | 0  | GRAD_CNTL     | write only | gradation control register for all four groups        |
| 3Fh                           | 0  | 1  | 1  | 1  | 1  | 1  | 1  | OFFSET        | write only | Offset/delay on LEDn outputs                          |
| 40h                           | 1  | 0  | 0  | 0  | 0  | 0  | 0  | SUBADR1       | write only | I <sup>2</sup> C-bus subaddress 1                     |
| 41h                           | 1  | 0  | 0  | 0  | 0  | 0  | 1  | SUBADR2       | write only | I <sup>2</sup> C-bus subaddress 2                     |
| 42h                           | 1  | 0  | 0  | 0  | 0  | 1  | 0  | SUBADR3       | write only | I <sup>2</sup> C-bus subaddress 3                     |
| 43h                           | 1  | 0  | 0  | 0  | 0  | 1  | 1  | ALLCALLADR    | write only | All Call I <sup>2</sup> C-bus address                 |
| 44h                           | 1  | 0  | 0  | 0  | 1  | 0  | 0  | PWMALL        | write only | brightness control for all LEDn                       |
| 45h                           | 1  | 0  | 0  | 0  | 1  | 0  | 1  | IREFALL       | write only | output gain control for all registers IREF0 to IREF15 |
| 46h to 7Fh                    | -  | -  | -  | -  | -  | -  | -  | reserved      | write only | not used <sup>[1]</sup>                               |

[1] Writing to reserved registers are ignored.

### 7.3.1 MODE1 — Mode register 1

Table 8. MODE1 - Mode register 1 (address 00h) bit description

Legend: \* default value.

| Bit | Symbol  | Access | Value | Description                                                                            |
|-----|---------|--------|-------|----------------------------------------------------------------------------------------|
| 7   | AIF     | W only | -     | Not used.                                                                              |
| 6   | AI1     | W only | 0*    | Auto-Increment bit 1 = 0. Auto-increment range as defined in <a href="#">Table 6</a> . |
|     |         |        | 1     | Auto-Increment bit 1 = 1. Auto-increment range as defined in <a href="#">Table 6</a> . |
| 5   | AI0     | W only | 0*    | Auto-Increment bit 0 = 0. Auto-increment range as defined in <a href="#">Table 6</a> . |
|     |         |        | 1     | Auto-Increment bit 0 = 1. Auto-increment range as defined in <a href="#">Table 6</a> . |
| 4   | SLEEP   | W only | 0*    | Normal mode <sup>[1]</sup> .                                                           |
|     |         |        | 1     | Low-power mode. Oscillator off <sup>[2][3]</sup> .                                     |
| 3   | SUB1    | W only | 0     | PCU9955A does not respond to I <sup>2</sup> C-bus subaddress 1.                        |
|     |         |        | 1*    | PCU9955A responds to I <sup>2</sup> C-bus subaddress 1.                                |
| 2   | SUB2    | W only | 0*    | PCU9955A does not respond to I <sup>2</sup> C-bus subaddress 2.                        |
|     |         |        | 1     | PCU9955A responds to I <sup>2</sup> C-bus subaddress 2.                                |
| 1   | SUB3    | W only | 0*    | PCU9955A does not respond to I <sup>2</sup> C-bus subaddress 3.                        |
|     |         |        | 1     | PCU9955A responds to I <sup>2</sup> C-bus subaddress 3.                                |
| 0   | ALLCALL | W only | 0     | PCU9955A does not respond to LED All Call I <sup>2</sup> C-bus address.                |
|     |         |        | 1*    | PCU9955A responds to LED All Call I <sup>2</sup> C-bus address.                        |

[1] It takes 500  $\mu$ s max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500  $\mu$ s window.

[2] No blinking, dimming or gradation control is possible when the oscillator is off.

[3] The device must be reset if the LED driver output state is set to LDRx=11 after the device is set back to Normal mode.

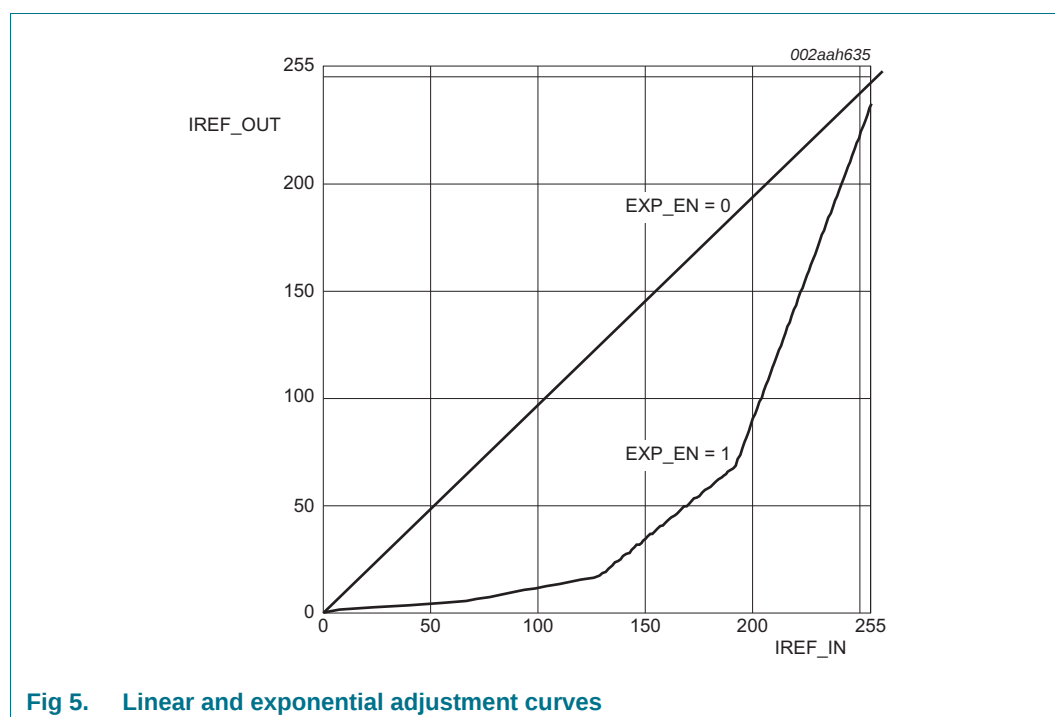
### 7.3.2 MODE2 — Mode register 2

**Table 9. MODE2 - Mode register 2 (address 01h) bit description**

Legend: \* default value.

| Bit | Symbol | Access | Value | Description                                                                                               |
|-----|--------|--------|-------|-----------------------------------------------------------------------------------------------------------|
| 7   | -      | -      | -     | not used (must write a logic 0)                                                                           |
| 6   | -      | -      | -     | not used (must write a logic 0)                                                                           |
| 5   | DMBLNK | W only | 0*    | group control = dimming                                                                                   |
|     |        |        | 1     | group control = blinking                                                                                  |
| 4   | -      | -      | -     | not used (must write a logic 0)                                                                           |
| 3   | OCH    | W only | 0*    | outputs change on STOP condition                                                                          |
|     |        |        | 1     | outputs change on ACK, this ninth bit is always set to 1 by U <sup>F</sup> m I <sup>2</sup> C-bus master. |
| 2   | EXP_EN | W only | 0*    | linear adjustment for gradation control                                                                   |
|     |        |        | 1     | exponential adjustment for gradation control                                                              |
| 1   | -      | -      | 0*    | reserved (must write a logic 0)                                                                           |
| 0   | -      | -      | 1*    | reserved (must write a logic 1)                                                                           |

Brightness adjustment for gradation control is either linear or exponential by setting the EXP\_EN bit as shown in [Figure 5](#). When EXP\_EN = 0, linear adjustment scale is used. When EXP\_EN = 1, exponential scale is used.



**Fig 5. Linear and exponential adjustment curves**

### 7.3.3 LEDOUT0 to LEDOUT3, LED driver output state

**Table 10. LEDOUT0 to LEDOUT3 - LED driver output state registers (address 02h to 05h) bit description**

Legend: \* default value.

| Address | Register | Bit | Symbol | Access | Value | Description                |
|---------|----------|-----|--------|--------|-------|----------------------------|
| 02h     | LEDOUT0  | 7:6 | LDR3   | W only | 10*   | LED3 output state control  |
|         |          | 5:4 | LDR2   | W only | 10*   | LED2 output state control  |
|         |          | 3:2 | LDR1   | W only | 10*   | LED1 output state control  |
|         |          | 1:0 | LDR0   | W only | 10*   | LED0 output state control  |
| 03h     | LEDOUT1  | 7:6 | LDR7   | W only | 10*   | LED7 output state control  |
|         |          | 5:4 | LDR6   | W only | 10*   | LED6 output state control  |
|         |          | 3:2 | LDR5   | W only | 10*   | LED5 output state control  |
|         |          | 1:0 | LDR4   | W only | 10*   | LED4 output state control  |
| 04h     | LEDOUT2  | 7:6 | LDR11  | W only | 10*   | LED11 output state control |
|         |          | 5:4 | LDR10  | W only | 10*   | LED10 output state control |
|         |          | 3:2 | LDR9   | W only | 10*   | LED9 output state control  |
|         |          | 1:0 | LDR8   | W only | 10*   | LED8 output state control  |
| 05h     | LEDOUT3  | 7:6 | LDR15  | W only | 10*   | LED15 output state control |
|         |          | 5:4 | LDR14  | W only | 10*   | LED14 output state control |
|         |          | 3:2 | LDR13  | W only | 10*   | LED13 output state control |
|         |          | 1:0 | LDR12  | W only | 10*   | LED12 output state control |

**LDRx = 00** — LED driver x is off (x = 0 to 15).

**LDRx = 01** — LED driver x is fully on (individual brightness and group dimming/blinking not controlled). The  $\overline{\text{OE}}$  pin can be used as external dimming/blinking control in this state.

**LDRx = 10** — LED driver x individual brightness can be controlled through its PWMx register (default power-up state) or PWMALL register for all LEDn outputs.

**LDRx = 11** — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

**Remark:** Setting the device in low power mode while being on group dimming/blinking mode may cause the LED output state to be in an unknown state after the device is set back to normal mode. The device must be reset and all register values reprogrammed.

### 7.3.4 GRPPWM, group duty cycle control

**Table 11. GRPPWM - Group brightness control register (address 06h) bit description**

Legend: \* default value

| Address | Register | Bit | Symbol   | Access | Value      | Description     |
|---------|----------|-----|----------|--------|------------|-----------------|
| 06h     | GRPPWM   | 7:0 | GDC[7:0] | W only | 1111 1111* | GRPPWM register |

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 122 Hz fixed frequency signal is superimposed with the 31.25 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a 'Don't care'.

General brightness for the 16 outputs is controlled through 255 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 67 ms to 16.8 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256} \quad (1)$$

### 7.3.5 GRPFREQ, group frequency

**Table 12. GRPFREQ - Group frequency register (address 07h) bit description**

Legend: \* default value.

| Address | Register | Bit | Symbol    | Access | Value      | Description      |
|---------|----------|-----|-----------|--------|------------|------------------|
| 07h     | GRPFREQ  | 7:0 | GFRQ[7:0] | W only | 0000 0000* | GRPFREQ register |

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

Blinking period is controlled through 256 linear steps from 00h (67 ms, frequency 15 Hz) to FFh (16.8 s).

$$global\ blinking\ period = \frac{GFRQ[7:0] + 1}{15.26} (s) \quad (2)$$

### 7.3.6 PWM0 to PWM15, individual brightness control

**Table 13. PWM0 to PWM15 - PWM registers 0 to 15 (address 08h to 17h) bit description**

Legend: \* default value.

| Address | Register | Bit | Symbol     | Access | Value      | Description                 |
|---------|----------|-----|------------|--------|------------|-----------------------------|
| 08h     | PWM0     | 7:0 | IDC0[7:0]  | W only | 0000 0000* | PWM0 Individual Duty Cycle  |
| 09h     | PWM1     | 7:0 | IDC1[7:0]  | W only | 0000 0000* | PWM1 Individual Duty Cycle  |
| 0Ah     | PWM2     | 7:0 | IDC2[7:0]  | W only | 0000 0000* | PWM2 Individual Duty Cycle  |
| 0Bh     | PWM3     | 7:0 | IDC3[7:0]  | W only | 0000 0000* | PWM3 Individual Duty Cycle  |
| 0Ch     | PWM4     | 7:0 | IDC4[7:0]  | W only | 0000 0000* | PWM4 Individual Duty Cycle  |
| 0Dh     | PWM5     | 7:0 | IDC5[7:0]  | W only | 0000 0000* | PWM5 Individual Duty Cycle  |
| 0Eh     | PWM6     | 7:0 | IDC6[7:0]  | W only | 0000 0000* | PWM6 Individual Duty Cycle  |
| 0Fh     | PWM7     | 7:0 | IDC7[7:0]  | W only | 0000 0000* | PWM7 Individual Duty Cycle  |
| 10h     | PWM8     | 7:0 | IDC8[7:0]  | W only | 0000 0000* | PWM8 Individual Duty Cycle  |
| 11h     | PWM9     | 7:0 | IDC9[7:0]  | W only | 0000 0000* | PWM9 Individual Duty Cycle  |
| 12h     | PWM10    | 7:0 | IDC10[7:0] | W only | 0000 0000* | PWM10 Individual Duty Cycle |
| 13h     | PWM11    | 7:0 | IDC11[7:0] | W only | 0000 0000* | PWM11 Individual Duty Cycle |
| 14h     | PWM12    | 7:0 | IDC12[7:0] | W only | 0000 0000* | PWM12 Individual Duty Cycle |

**Table 13. PWM0 to PWM15 - PWM registers 0 to 15 (address 08h to 17h) bit description**  
...continued

| Address | Register | Bit | Symbol     | Access | Value      | Description                 |
|---------|----------|-----|------------|--------|------------|-----------------------------|
| 15h     | PWM13    | 7:0 | IDC13[7:0] | W only | 0000 0000* | PWM13 Individual Duty Cycle |
| 16h     | PWM14    | 7:0 | IDC14[7:0] | W only | 0000 0000* | PWM14 Individual Duty Cycle |
| 17h     | PWM15    | 7:0 | IDC15[7:0] | W only | 0000 0000* | PWM15 Individual Duty Cycle |

A 31.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 255 linear steps from 00h (0 % duty cycle = LED output off) to FEh (99.2 % duty cycle = LED output at maximum brightness) and FFh (100 % duty cycle = LED output completed ON). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$duty\ cycle = \frac{IDC_x[7:0]}{256} \quad (3)$$

**Remark:** The first lower end 8 steps of PWM and the last (higher end) steps of PWM do not have effective brightness control of LEDs due to edge rate control of LED output pins.

### 7.3.7 IREF0 to IREF15, LED output current value registers

These registers reflect the gain settings for output current for LED0 to LED15.

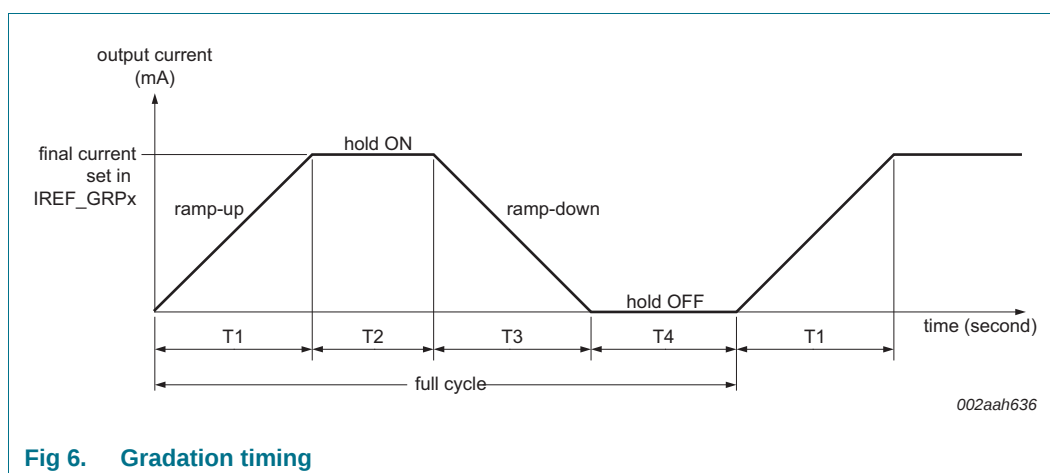
**Table 14. IREF0 to IREF15 - LED output gain control registers (address 18h to 27h) bit description**

Legend: \* default value.

| Address | Register | Bit | Access | Value | Description                  |
|---------|----------|-----|--------|-------|------------------------------|
| 18h     | IREF0    | 7:0 | W only | 00h*  | LED0 output current setting  |
| 19h     | IREF1    | 7:0 | W only | 00h*  | LED1 output current setting  |
| 1Ah     | IREF2    | 7:0 | W only | 00h*  | LED2 output current setting  |
| 1Bh     | IREF3    | 7:0 | W only | 00h*  | LED3 output current setting  |
| 1Ch     | IREF4    | 7:0 | W only | 00h*  | LED4 output current setting  |
| 1Dh     | IREF5    | 7:0 | W only | 00h*  | LED5 output current setting  |
| 1Eh     | IREF6    | 7:0 | W only | 00h*  | LED6 output current setting  |
| 1Fh     | IREF7    | 7:0 | W only | 00h*  | LED7 output current setting  |
| 20h     | IREF8    | 7:0 | W only | 00h*  | LED8 output current setting  |
| 21h     | IREF9    | 7:0 | W only | 00h*  | LED9 output current setting  |
| 22h     | IREF10   | 7:0 | W only | 00h*  | LED10 output current setting |
| 23h     | IREF11   | 7:0 | W only | 00h*  | LED11 output current setting |
| 24h     | IREF12   | 7:0 | W only | 00h*  | LED12 output current setting |
| 25h     | IREF13   | 7:0 | W only | 00h*  | LED13 output current setting |
| 26h     | IREF14   | 7:0 | W only | 00h*  | LED14 output current setting |
| 27h     | IREF15   | 7:0 | W only | 00h*  | LED15 output current setting |

### 7.3.8 Gradation control

Gradation control is designed to use four independent groups of registers to program the full cycle of the gradation timing to implement on each selected channel. Each group has four registers to define the ramp rate, step time, hold ON/OFF time, and final hold ON current, as shown in [Figure 6](#).



**Fig 6. Gradation timing**

- The 'final' and 'hold ON' current is defined in IREF\_GRPx register value  $\times$  (225  $\mu$ A if REXT = 1 k $\Omega$ , or 112.5  $\mu$ A if REXT = 2 k $\Omega$ ).
- Ramp rate value and enable/disable ramp operation is defined in RAMP\_RATE\_GRPx register.
- Total number of ramp steps (or level changes) is calculated as 'IREF\_GRPx value'  $\div$  'ramp rate value in RAMP\_RATE\_GRPx'. If the total number is not an integer, the number is rounded up to the next integer.
- Time for each step is calculated as 'cycle time'  $\times$  'multiple factor' bits in STEP\_TIME\_GRPx register. Minimum time for one step is 0.5 ms (0.5 ms  $\times$  1) and maximum time is 512 ms (8 ms  $\times$  64).
- The ramp-up or ramp-down time (T1 or T3) is calculated as '(total steps + 1)  $\times$  'step time'.
- Hold ON or OFF time (T2 or T4) is defined in HOLD\_CNTL\_GRPx register in the range of 0/0.25/0.5/0.75/1/2/4/6 seconds.
- Gradation start or stop with single shot mode (one full cycle only) or continuous mode (repeat full cycle) is defined in the GRAD\_CNTL register for all groups.
- Each channel can be assigned to one of these four groups in the GRAD\_GRP\_SELx register.
- Each channel can set either normal mode or gradation mode operation in the GRAD\_MODE\_SELx register.

To enable the gradation operation, the following steps are required:

1. Program all gradation control registers except the gradation start bit in GRAD\_CNTL register.
2. Program either LDRx = 01 (LED fully ON mode) only, or LDRx = 10 or 11 (PWM control mode) with individual brightness control PWMx register for duty cycle.
3. Program output current value IREFx register to non-zero, which enables LED output.

4. Set the gradation start bit in GRAD\_CNTL register for enabling gradation operation.

### 7.3.8.1 RAMP\_RATE\_GRP0 to RAMP\_RATE\_GRP3, ramp rate control registers

**Table 15. RAMP\_RATE\_GRP[0:3] - Ramp enable and rate control registers (address 28h, 2Ch, 30h, 34h) for each group bit description**

Legend: \* default value.

| Address | Register       | Bit | Access | Value | Description                                                                                          |
|---------|----------------|-----|--------|-------|------------------------------------------------------------------------------------------------------|
| 28h     | RAMP_RATE_GRP0 | 7   | W only | 0*    | Ramp-up disable                                                                                      |
| 2Ch     | RAMP_RATE_GRP1 |     |        | 1     | Ramp-up enable                                                                                       |
| 30h     | RAMP_RATE_GRP2 | 6   | W only | 0*    | Ramp-down disable                                                                                    |
| 34h     | RAMP_RATE_GRP3 |     |        | 1     | Ramp-down enable                                                                                     |
|         |                | 5:0 | W only | 0x00* | Ramp rate value per step is defined from 1 (00h) to 64 (3Fh) <a href="#">[1]</a> <a href="#">[2]</a> |

[1] Total number of ramp steps is defined as 'IREF\_GRP[7:0] ÷ 'ramp\_rate[5:0]'. (Round up to next integer if it is not an integer number.)

[2] Per step current increment or decrement is calculated by the  $(\text{ramp\_rate} \times I_{\text{ref}})$ , where the  $I_{\text{ref}}$  reference current is 112.5  $\mu\text{A}$  (REXT = 2 k $\Omega$ ) or 225  $\mu\text{A}$  (REXT = 1 k $\Omega$ ).

### 7.3.8.2 STEP\_TIME\_GRP0 to STEP\_TIME\_GRP3, step time control registers

**Table 16. STEP\_TIME\_GRP[0:3] - Step time control registers (address 29h, 2Dh, 31h, 35h) for each group bit description**

Legend: \* default value.

| Address | Register       | Bit | Access | Value | Description                                                                                           |
|---------|----------------|-----|--------|-------|-------------------------------------------------------------------------------------------------------|
| 29h     | STEP_TIME_GRP0 | 7   | W only | 0*    | reserved (must write a logic 0)                                                                       |
| 2Dh     | STEP_TIME_GRP1 | 6   | W only | 0*    | Cycle time is set to 0.5 ms                                                                           |
| 31h     | STEP_TIME_GRP2 |     |        | 1     | Cycle time is set to 8 ms                                                                             |
| 35h     | STEP_TIME_GRP3 | 5:0 | W only | 0x00* | Multiple factor per step, the multiple factor is defined from 1 (00h) to 64 (3Fh) <a href="#">[1]</a> |

[1] Step time = cycle time (0.5 ms or 8 ms) × multiple factor (1 ~ 64); minimum step time is 0.5 ms and maximum step time is 512 ms.

## 7.3.8.3 HOLD\_CNTL\_GRP0 to HOLD\_CNTL\_GRP3, hold ON and OFF control registers

Table 17. HOLD\_CNTL\_GRP[0:3] - Hold ON and OFF enable and time control registers (address 2Ah, 2Eh, 32h, 36h) for each group bit description

Legend: \* default value.

| Address | Register       | Bit | Access | Value | Description                                                                                                                                       |
|---------|----------------|-----|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 2Ah     | HOLD_CNTL_GRP0 | 7   | W only | 0*    | Hold ON disable                                                                                                                                   |
| 2Eh     | HOLD_CNTL_GRP1 |     |        | 1     | Hold ON enable                                                                                                                                    |
| 32h     | HOLD_CNTL_GRP2 | 6   | W only | 0*    | Hold OFF disable                                                                                                                                  |
| 36h     | HOLD_CNTL_GRP3 |     |        | 1     | Hold OFF enable                                                                                                                                   |
|         |                | 5:3 | W only | 000*  | Hold ON time select: <a href="#">[1]</a><br>000: 0 s<br>001: 0.25 s<br>010: 0.5 s<br>011: 0.75 s<br>100: 1 s<br>101: 2 s<br>110: 4 s<br>111: 6 s  |
|         |                | 2:0 | W only | 000*  | Hold OFF time select: <a href="#">[1]</a><br>000: 0 s<br>001: 0.25 s<br>010: 0.5 s<br>011: 0.75 s<br>100: 1 s<br>101: 2 s<br>110: 4 s<br>111: 6 s |

[1] Hold ON or OFF minimum time is 0 s and maximum time is 6 s.

## 7.3.8.4 IREF\_GRP0 to IREF\_GRP3, output gain control

Table 18. IREF\_GRP[0:3] - Final and hold ON output gain setting registers (address 2Bh, 2Fh, 33h, 37h) for each group bit description

Legend: \* default value.

| Address | Register  | Bit | Access | Value | Description                                                               |
|---------|-----------|-----|--------|-------|---------------------------------------------------------------------------|
| 2Bh     | IREF_GRP0 | 7:0 | W only | 00h*  | Final ramp-up and hold ON output current gain setting <a href="#">[1]</a> |
| 2Fh     | IREF_GRP1 |     |        |       |                                                                           |
| 33h     | IREF_GRP2 |     |        |       |                                                                           |
| 37h     | IREF_GRP3 |     |        |       |                                                                           |

[1] Output current =  $I_{ref} \times IREF\_GRP[7:0]$ , where  $I_{ref}$  is reference current. If  $REXT = 2\text{ k}\Omega$ , then  $I_{ref} = 112.5\text{ }\mu\text{A}$ , or if  $REXT = 1\text{ k}\Omega$ , then  $I_{ref} = 225\text{ }\mu\text{A}$ .

### 7.3.8.5 GRAD\_MODE\_SEL0 to GRAD\_MODE\_SEL1, gradation mode select registers

**Table 19. GRAD\_MODE\_SEL[0:1] - Gradation mode select register for channel 15 to channel 0 (address 38h, 39h) bit description**

Legend: \* default value.

| Address | Register       | Bit | Access | Value | Description <sup>[1][2]</sup>                        |
|---------|----------------|-----|--------|-------|------------------------------------------------------|
| 38h     | GRAD_MODE_SEL0 | 7:0 | W only | 00*   | Normal operation mode for channel 7 to channel 0     |
|         |                |     |        | FFh   | Gradation operation mode for channel 7 to channel 0  |
| 39h     | GRAD_MODE_SEL1 | 7:0 | W only | 00*   | Normal operation mode for channel 15 to channel 8    |
|         |                |     |        | FFh   | Gradation operation mode for channel 15 to channel 8 |

[1] Each bit represents one channel that can set either 0 for normal mode (use IREFx to set individual LED output current), or 1 for gradation mode (use IREF\_GRPx to set group LEDs output current.).

[2] In gradation mode, it only affects the source of the IREF current level and does not affect the PWMx operation or LEDOUTx register function. It is possible to use the gradation feature, individual PWMx and group PWM simultaneously.

### 7.3.8.6 GRAD\_GRP\_SEL0 to GRAD\_GRP\_SEL3, gradation group select registers

**Table 20. GRAD\_GRP\_SEL[0:3] - Gradation group select register for channel 15 to channel 0 (address 3Ah, 3Bh, 3Ch, 3Dh) bit description**

Legend: \* default value.

| Address | Register      | Bit | Access | Value | Description <sup>[1]</sup>              |
|---------|---------------|-----|--------|-------|-----------------------------------------|
| 3Ah     | GRAD_GRP_SEL0 | 7:6 | W only | 00*   | Gradation group select for LED3 output  |
|         |               | 5:4 | W only | 00*   | Gradation group select for LED2 output  |
|         |               | 3:2 | W only | 00*   | Gradation group select for LED1 output  |
|         |               | 1:0 | W only | 00*   | Gradation group select for LED0 output  |
| 3Bh     | GRAD_GRP_SEL1 | 7:6 | W only | 01*   | Gradation group select for LED7 output  |
|         |               | 5:4 | W only | 01*   | Gradation group select for LED6 output  |
|         |               | 3:2 | W only | 01*   | Gradation group select for LED5 output  |
|         |               | 1:0 | W only | 01*   | Gradation group select for LED4 output  |
| 3Ch     | GRAD_GRP_SEL2 | 7:6 | W only | 10*   | Gradation group select for LED11 output |
|         |               | 5:4 | W only | 10*   | Gradation group select for LED10 output |
|         |               | 3:2 | W only | 10*   | Gradation group select for LED9 output  |
|         |               | 1:0 | W only | 10*   | Gradation group select for LED8 output  |
| 3Dh     | GRAD_GRP_SEL3 | 7:6 | W only | 11*   | Gradation group select for LED15 output |
|         |               | 5:4 | W only | 11*   | Gradation group select for LED14 output |
|         |               | 3:2 | W only | 11*   | Gradation group select for LED13 output |
|         |               | 1:0 | W only | 11*   | Gradation group select for LED12 output |

[1] LED[3:0] outputs default assigned to group 0; LED[7:4] outputs default assigned to group 1; LED[11:8] outputs default assigned to group 2; LED[15:12] outputs default assigned to group 3.

## 7.3.8.7 GRAD\_CNTL, Gradation control register

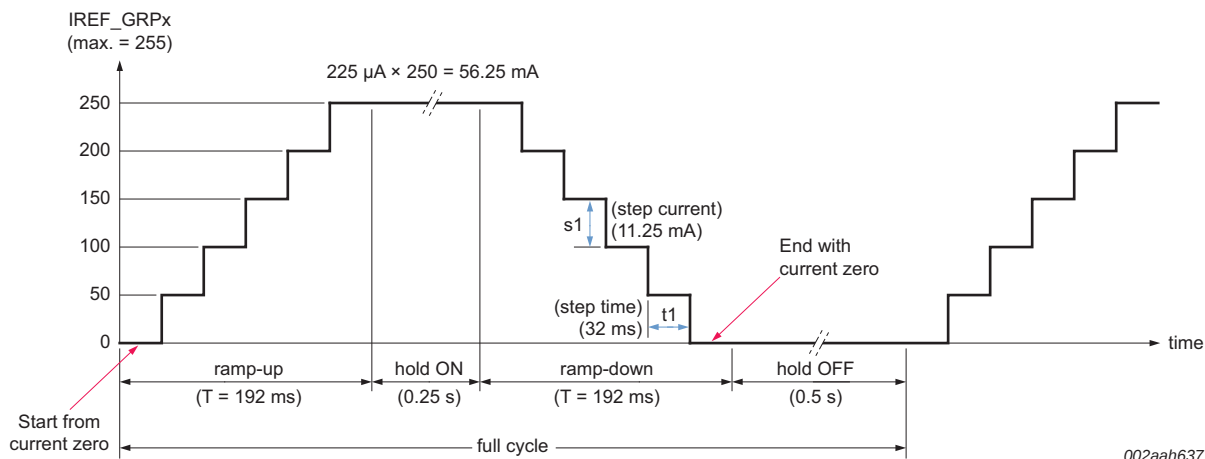
Table 21. GRAD\_CNTL - Gradation control register for group 3 to group 0 (address 3Eh)  
bit description

Legend: \* default value.

| Address | Register  | Bit | Access | Value | Description                                |
|---------|-----------|-----|--------|-------|--------------------------------------------|
| 3Eh     | GRAD_CNTL | 7   | W only | 0*    | Gradation stop for group 3 <sup>[1]</sup>  |
|         |           |     |        | 1     | Gradation start for group 3 <sup>[2]</sup> |
|         |           | 6   | W only | 0*    | Single shot operation for group 3          |
|         |           |     |        | 1     | Continuous operation for group 3           |
|         |           | 5   | W only | 0*    | Gradation stop for group 2 <sup>[1]</sup>  |
|         |           |     |        | 1     | Gradation start for group 2 <sup>[2]</sup> |
|         |           | 4   | W only | 0*    | Single shot operation for group 2          |
|         |           |     |        | 1     | Continuous operation for group 2           |
|         |           | 3   | W only | 0*    | Gradation stop for group 1 <sup>[1]</sup>  |
|         |           |     |        | 1     | Gradation start for group 1 <sup>[2]</sup> |
|         |           | 2   | W only | 0*    | Single shot operation for group 1          |
|         |           |     |        | 1     | Continuous operation for group 1           |
|         |           | 1   | W only | 0*    | Gradation stop for group 0 <sup>[1]</sup>  |
|         |           |     |        | 1     | Gradation start for group 0 <sup>[2]</sup> |
|         |           | 0   | W only | 0*    | Single shot operation for group 0          |
|         |           |     |        | 1     | Continuous operation for group 0           |

- [1] When the gradation operation is forced to stop by writing 0, the output current stops immediately and is frozen at the last output level.
- [2] Writing 1 to this bit starts the gradation operation, and writing 0 to this bit forces the gradation operation to stop when single mode is not completed or continuous mode is running.

#### 7.3.8.8 Ramp control — equation and calculation example



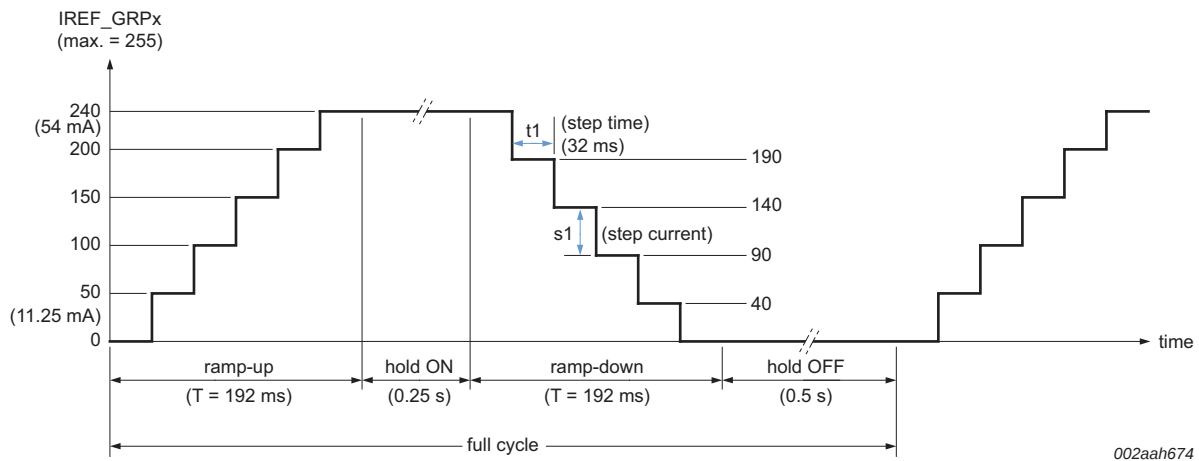
**Fig 7. Ramp calculation example 1**

- $t_1$  (step time) = cycle time  $\times$  multiple factor, where:
  - Cycle time = 0.5 ms (fast ramp) or 8 ms (slow ramp) in STEP\_TIME\_GRPx[6]
  - Multiple factor = 6-bit, from 1 (00h) to 64 (3Fh) counts in STEP\_TIME\_GRPx[5:0]
- $s_1$  (step current) = ramp\_rate  $\times I_{ref}$ , where:
  - ramp\_rate = 6-bit, from 1 (00h) to 64 (3Fh) counts in RAMP\_RATE\_GRPx[5:0]
  - $I_{ref}$  = reference current either 112.5  $\mu$ A if REXT = 2 k $\Omega$ , or 225  $\mu$ A if REXT = 1 k $\Omega$
- $S$  (total steps) = (IREF\_GRPx / ramp\_rate), where:
  - IREF\_GRPx = output current gain setting, 8-bit, up to 255 counts
  - ramp\_rate = 6-bit, up to 64 counts in RAMP\_RATE\_GRPx[5:0]
  - If it is not an integer, then round up to next integer number.
- $T$  (ramp time) = ( $S$  (total steps) + 1)  $\times t_1$  (step time)
  - Ramp-up time starts from zero current and ends at the maximum current
  - Ramp-down time starts from the maximum current and ends at the zero current

**Calculation example 1 (Figure 7):**

- Assumption:
  - $I_{ref} = 225 \mu A$  if  $REXT = 1 k\Omega$
  - Output hold ON current =  $225 \mu A \times 250 = 56.25 mA$  ( $IREF\_GRP_x[7:0] = FAh$ )
  - Cycle time = 0.5 ms ( $STEP\_TIME\_GRP_x[6] = 0$ )
  - Multiple factor = 64 ( $STEP\_TIME\_GRP_x[5:0] = 3Fh$ )
  - Ramp rate = 50 ( $RAMP\_RATE\_GRP_x[5:0] = 31h$ )
  - Hold ON = 0.25 s ( $HOLD\_CNTL\_GRP_x[5:3] = 001$ )
  - Hold OFF = 0.5 s ( $HOLD\_CNTL\_GRP_x[2:0] = 010$ )
- $t_1$  (step time) = cycle time (0.5 ms)  $\times$  multiple (64) = 32 ms
- Step current = ramp\_rate  $\times I_{ref} = 50 \times 225 \mu A = 11.25 mA$

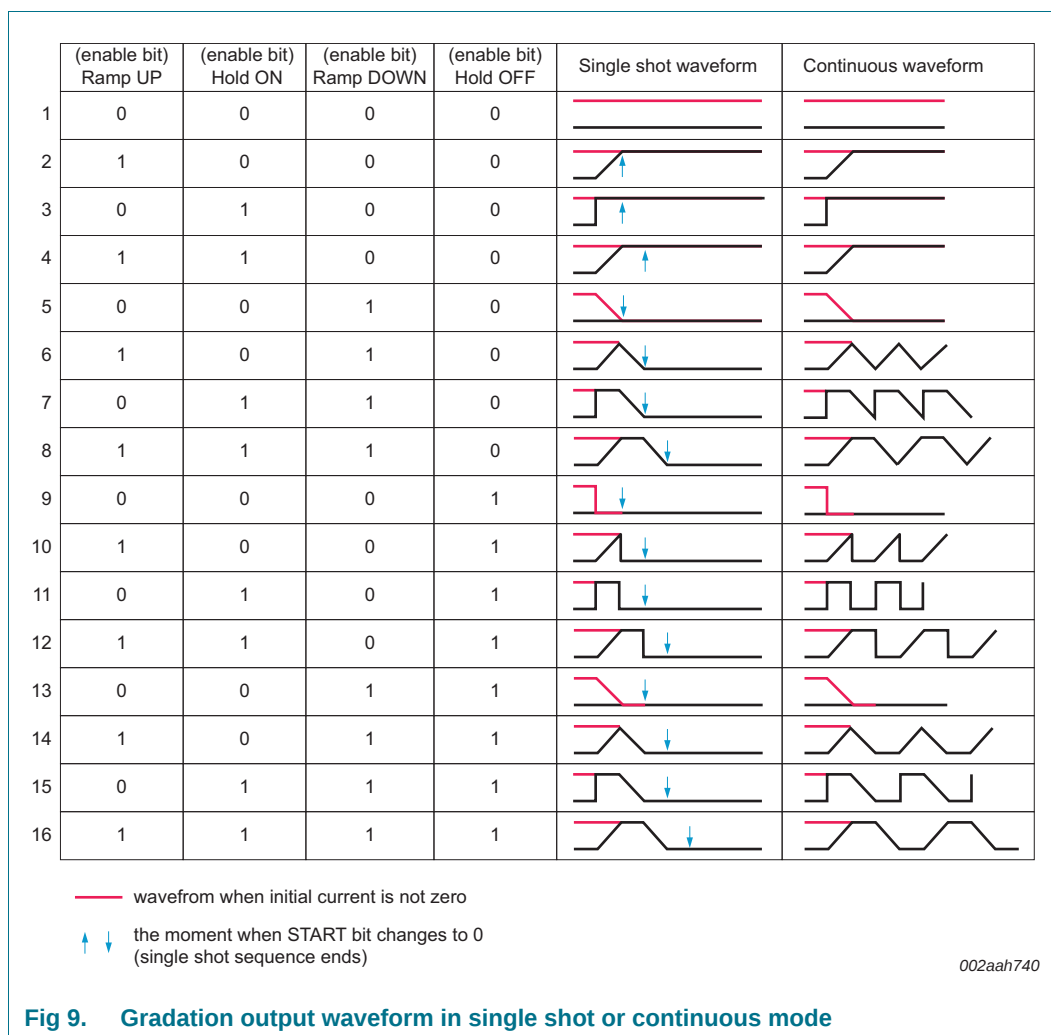
- $S$  (total steps) =  $(I_{REF\_GRP} \div \text{ramp\_rate}) = (250 \div 50) = 5$  steps
- $T$  (ramp time) =  $(S + 1) \times t_1 = 6 \times 32 \text{ ms} = 192 \text{ ms}$



**Fig 8. Ramp calculation example 2**

#### Calculation example 2:

- Assumption:
  - $I_{ref} = 225 \mu\text{A}$  if  $R_{EXT} = 1 \text{ k}\Omega$
  - Output hold ON current =  $225 \mu\text{A} \times 240 = 54 \text{ mA}$  ( $I_{REF\_GRP}[7:0] = F0h$ )
  - Cycle time = 0.5 ms ( $STEP\_TIME\_GRP[6] = 0$ )
  - Multiple factor = 64 ( $STEP\_TIME\_GRP[5:0] = 3Fh$ )
  - Ramp rate = 50 ( $RAMP\_RATE\_GRP[5:0] = 31h$ )
  - Hold ON = 0.25 s ( $HOLD\_CNTL\_GRP[5:3] = 001$ )
  - Hold OFF = 0.5 s ( $HOLD\_CNTL\_GRP[2:0] = 010$ )
- $t_1$  (step time) = cycle time (0.5 ms)  $\times$  multiple (64) = 32 ms
- Step current = ramp\_rate  $\times I_{ref} = 50 \times 225 \mu\text{A} = 11.25 \text{ mA}$  (except the last one)
- $S$  (total steps) =  $I_{REF\_GRP} \div \text{ramp\_rate} = 240 \div 50 = 4.8$  steps (round up to next integer) = 5 steps
- $T$  (ramp time) =  $(S + 1) \times t_1 = 6 \times 32 \text{ ms} = 192 \text{ ms}$



### 7.3.9 OFFSET — LEDn output delay offset register

**Table 22. OFFSET - LEDn output delay offset register (address 3Fh) bit description**

Legend: \* default value.

| Address | Register | Bit | Access | Value | Description                     |
|---------|----------|-----|--------|-------|---------------------------------|
| 3Fh     | OFFSET   | 7:4 | -      | 0000* | not used (must write a logic 0) |
|         |          | 3:0 | W only | 1000* | LEDn output delay offset factor |

The PCU9955A can be programmed to have turn-on delay between LED outputs. This helps to reduce peak current for the V<sub>DD</sub> supply and reduces EMI.

The order in which the LED outputs are enabled is always the same (channel 0 enables first and channel 15 enables last).

OFFSET control register bits [3:0] determine the delay used between the turn-on times as follows:

- 0000 = no delay between outputs (all on, all off at the same time)
- 0001 = delay of 1 clock cycle (125 ns) between successive outputs
- 0010 = delay of 2 clock cycles (250 ns) between successive outputs
- 0011 = delay of 3 clock cycles (375 ns) between successive outputs
- :
- 1111 = delay of 15 clock cycles (1.875 μs) between successive outputs

**Example:** If the value in the OFFSET register is 1000, the corresponding delay =  $8 \times 125 \text{ ns} = 1 \text{ μs}$  delay between successive outputs.

- channel 0 turns on at time 0 μs
- channel 1 turns on at time 1 μs
- channel 2 turns on at time 2 μs
- channel 3 turns on at time 3 μs
- channel 4 turns on at time 4 μs
- channel 5 turns on at time 5 μs
- channel 6 turns on at time 6 μs
- channel 7 turns on at time 7 μs
- channel 8 turns on at time 8 μs
- channel 9 turns on at time 9 μs
- channel 10 turns on at time 10 μs
- channel 11 turns on at time 11 μs
- channel 12 turns on at time 12 μs
- channel 13 turns on at time 13 μs
- channel 14 turns on at time 14 μs
- channel 15 turns on at time 15 μs

### 7.3.10 LED Sub Call I<sup>2</sup>C-bus addresses for PCU9955A

**Table 23. SUBADR1 to SUBADR3 - I<sup>2</sup>C-bus subaddress registers 1 to 3 (address 40h to 42h) bit description**

Legend: \* default value.

| Address | Register | Bit | Symbol  | Access | Value     | Description                       |
|---------|----------|-----|---------|--------|-----------|-----------------------------------|
| 40h     | SUBADR1  | 7:1 | A1[7:1] | W only | 1110 110* | I <sup>2</sup> C-bus subaddress 1 |
|         |          | 0   | A1[0]   | -      | 0*        | reserved (must write a logic 0)   |
| 41h     | SUBADR2  | 7:1 | A2[7:1] | W only | 1110 110* | I <sup>2</sup> C-bus subaddress 2 |
|         |          | 0   | A2[0]   | -      | 0*        | reserved (must write a logic 0)   |
| 42h     | SUBADR3  | 7:1 | A3[7:1] | W only | 1110 110* | I <sup>2</sup> C-bus subaddress 3 |
|         |          | 0   | A3[0]   | -      | 0*        | reserved (must write a logic 0)   |

Default power-up values are ECh, ECh, ECh. At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 are disabled. The power-up default bit subaddress of ECh indicates that this device is a 16-channel LED driver.

All three subaddresses are programmable. Once subaddresses have been programmed to their right values, SUBx bits must be set to logic 1 in order to have the device respond to these addresses (bit[3:1], MODE1 register). When SUBx is set to logic 1, the corresponding I<sup>2</sup>C-bus subaddress can be used during an I<sup>2</sup>C-bus write sequence.

### 7.3.11 ALLCALLADR, LED All Call I<sup>2</sup>C-bus address

**Table 24. ALLCALLADR - LED All Call I<sup>2</sup>C-bus address register (address 43h) bit description**

Legend: \* default value.

| Address | Register   | Bit | Symbol  | Access | Value     | Description                                   |
|---------|------------|-----|---------|--------|-----------|-----------------------------------------------|
| 43h     | ALLCALLADR | 7:1 | AC[7:1] | W only | 1110 000* | ALLCALL I <sup>2</sup> C-bus address register |
|         |            | 0   | AC[0]   | -      | 0*        | reserved (must write a logic 0)               |

The LED All Call I<sup>2</sup>C-bus address allows all the PCU9955As on the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to logic 1 [power-up default state]). This address is programmable through the I<sup>2</sup>C-bus and can be used during an I<sup>2</sup>C-bus write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I<sup>2</sup>C-bus address are valid. The LSB in ALLCALLADR register is set to 0.

If ALLCALL bit = 0 in MODE1 register, the device does not recognize the address programmed in register ALLCALLADR.

### 7.3.12 PWMALL — brightness control for all LEDn outputs

When programmed, the value in this register is used for PWM duty cycle for all the LEDn outputs and is reflected in PWM0 through PWM15 registers.

**Table 25. PWMALL - brightness control for all LEDn outputs register (address 44h) bit description**

Legend: \* default value.

| Address | Register | Bit | Access     | Value      | Description                     |
|---------|----------|-----|------------|------------|---------------------------------|
| 44h     | PWMALL   | 7:0 | write only | 0000 0000* | duty cycle for all LEDn outputs |

**Remark:** Write to any of the PWM0 to PWM15 registers overwrites the value in corresponding PWMn register programmed by PWMALL.

### 7.3.13 IREFALL register: output current value for all LED outputs

The output current setting for all outputs is held in this register. When this register is written to or updated, all LED outputs are set to a current corresponding to this register value.

Writes to IREF0 to IREF15 overwrite the output current settings.

**Table 26. IREFALL - Output gain control for all LED outputs (address 45h) bit description**

Legend: \* default value.

| Address | Register | Bit | Access     | Value | Description                               |
|---------|----------|-----|------------|-------|-------------------------------------------|
| 45h     | IREFALL  | 7:0 | write only | 00h*  | Current gain setting for all LED outputs. |

### 7.3.14 LED driver constant current outputs

In LED display applications, PCU9955A provides nearly no current variations from channel to channel and from device to device. The maximum current skew between channels is less than ±4 % and less than ±6 % between devices.

#### 7.3.14.1 Adjusting output current

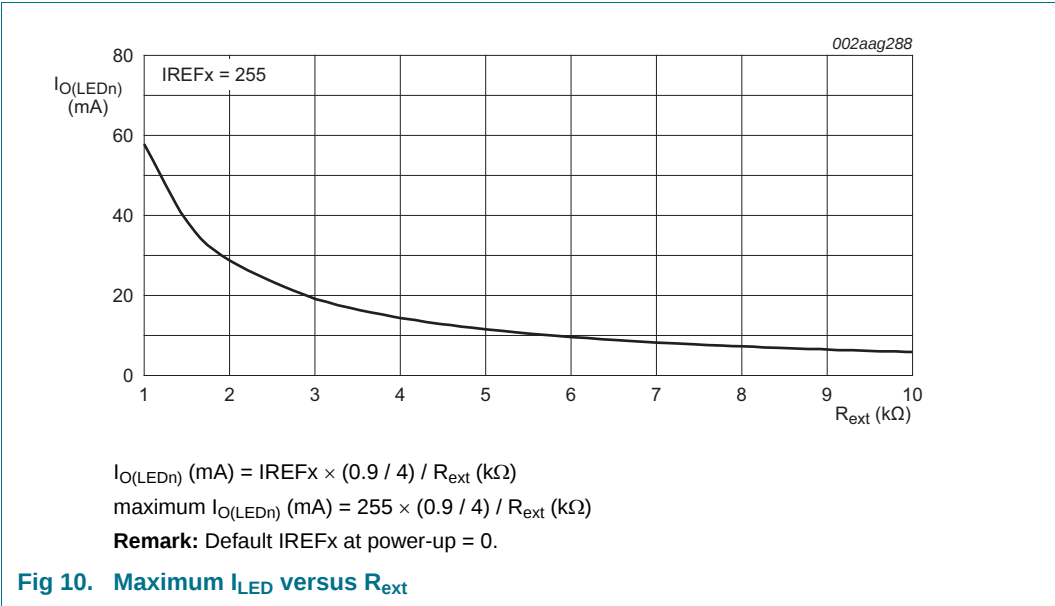
The PCU9955A scales up the reference current ( $I_{ref}$ ) set by the external resistor ( $R_{ext}$ ) to sink the output current ( $I_O$ ) at each output port. The maximum output current for the outputs can be set using  $R_{ext}$ . In addition, the constant value for current drive at each of the outputs is independently programmable using command registers IREF0 to IREF15. Alternatively, programming the IREFALL register allows all outputs to be set at one current value determined by the value in IREFALL register.

[Equation 4](#) and [Equation 5](#) can be used to calculate the minimum and maximum constant current values that can be programmed for the outputs for a chosen  $R_{ext}$ .

$$I_{O\_LED\_MIN} = \frac{900 \text{ mV}}{R_{ext}} \times \frac{1}{4} \text{ (minimum constant current)} \quad (4)$$

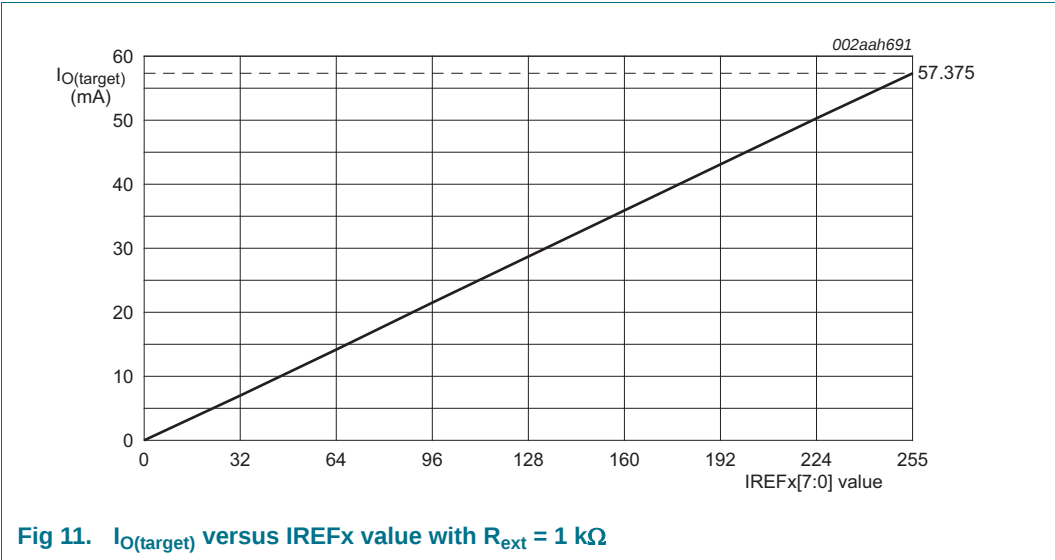
$$I_{O\_LED\_MAX} = (255 \times I_{O\_LED\_MIN}) = \left( \frac{900 \text{ mV}}{R_{ext}} \times \frac{255}{4} \right) \quad (5)$$

$$\text{For a given IREFx setting, } I_{O\_LED} = IREFx \times \frac{900 \text{ mV}}{R_{ext}} \times \frac{1}{4}.$$



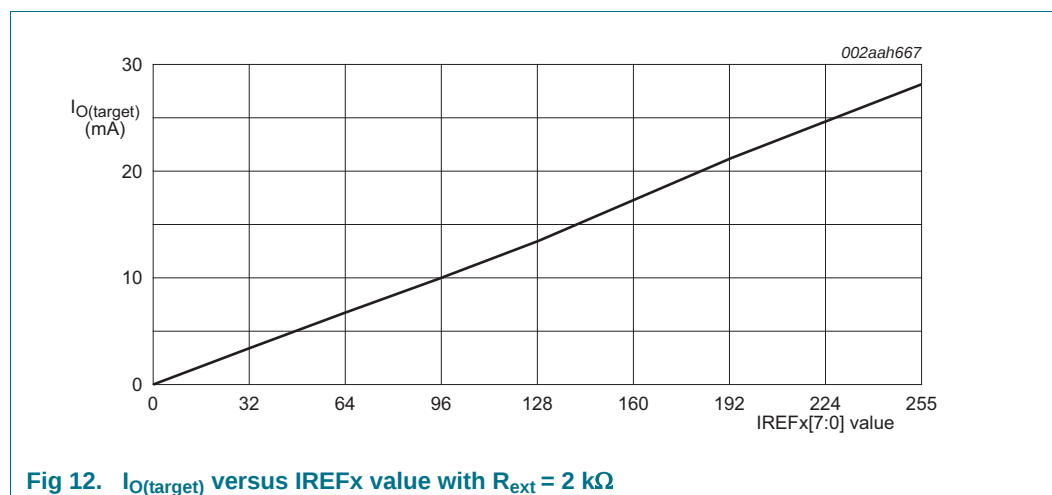
**Example 1:** If  $R_{ext} = 1 \text{ k}\Omega$ ,  $I_{O\_LED\_MIN} = 225 \text{ }\mu\text{A}$ ,  $I_{O\_LED\_MAX} = 57.375 \text{ mA}$  (as shown in [Figure 11](#)).

So each channel can be programmed with its individual IREFx in 256 steps and in  $225 \text{ }\mu\text{A}$  increments to a maximum output current of  $57.375 \text{ mA}$  independently.



**Example 2:** If  $R_{\text{ext}} = 2 \text{ k}\Omega$ ,  $I_{\text{O\_LED\_MIN}} = 112.5 \text{ }\mu\text{A}$ ,  $I_{\text{O\_LED\_MAX}} = 28.687 \text{ mA}$  (as shown in [Figure 12](#)).

So each channel can be programmed with its individual IREFx in 256 steps and in  $112.5 \text{ }\mu\text{A}$  increments to a maximum output channel of  $28.687 \text{ mA}$  independently.



### 7.3.15 Overtemperature protection

If the PCU9955A chip temperature exceeds its limit ( $T_{\text{th(otp)}}$  rising, see [Table 29](#)), all output channels are disabled until the temperature drops below its limit minus a small hysteresis ( $T_{\text{th(otp)}}$  hysteresis), see [Table 29](#). Once the die temperature reduces below the  $T_{\text{th(otp)}}$  rising –  $T_{\text{th(otp)}}$  hysteresis, the chip returns to the same condition it was prior to the overtemperature event.

## 7.4 Active LOW output enable input

The active LOW output enable ( $\overline{\text{OE}}$ ) pin on PCU9955A allows it to enable or disable all the LED outputs at the same time.

- When a LOW level is applied to  $\overline{\text{OE}}$  pin, all the LED outputs are enabled.
- When a HIGH level is applied to  $\overline{\text{OE}}$  pin, all the LED outputs are high-impedance.

The  $\overline{\text{OE}}$  pin can be used as a synchronization signal to switch on/off several PCU9955A devices at the same time when LED drive output state is set fully ON ( $\text{LDRx} = 01$  in  $\text{LEDOUTx}$  register) in these devices. This requires an external clock reference that provides blinking period and the duty cycle.

The  $\overline{\text{OE}}$  pin can also be used as an external dimming control signal. The frequency of the external clock must be high enough not to be seen by the human eye, and the duty cycle value determines the brightness of the LEDs.

**Remark:** Do not use  $\overline{\text{OE}}$  as an external blinking control signal when internal global blinking is selected ( $\text{DMBLNK} = 1$ ,  $\text{MODE2}$  register) since it results in an undefined blinking pattern. Do not use  $\overline{\text{OE}}$  as an external dimming control signal when internal global dimming is selected ( $\text{DMBLNK} = 0$ ,  $\text{MODE2}$  register) since it results in an undefined dimming pattern.

## 7.5 Power-on reset

When power is applied to  $V_{DD}$ , an internal power-on reset holds the PCU9955A in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At this point, the reset condition is released and the PCU9955A registers and I<sup>2</sup>C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter,  $V_{DD}$  must be pulled lower than 1 V and stay LOW for longer than 20  $\mu$ s. The device resets itself, and allow 2 ms for the device to wake up fully.

**Remark:** In order to guarantee a proper Power-On Reset operation for device, the rising rate of  $V_{DD}$  must be less than 3 ms per 1 V or less than 10 ms from 0 V to 3.3 V. Also,  $V_{DD}$  must return to 0 V for a minimum of 10 ms before rising again while  $V_{DD}$  power is re-cycling.

## 7.6 Hardware reset recovery

When a reset of PCU9955A is activated using an active LOW input on the  $\overline{\text{RESET}}$  pin, a reset pulse width of 2.5  $\mu$ s minimum is required. The maximum wait time after  $\overline{\text{RESET}}$  pin is released is 1.5 ms.

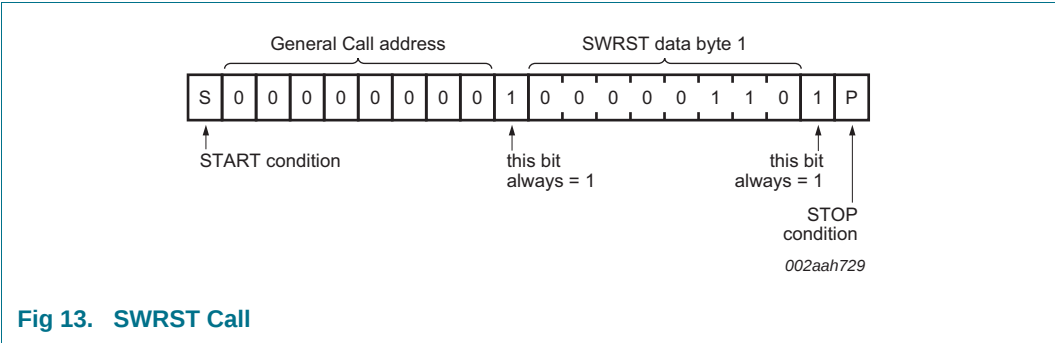
## 7.7 Software reset

The Software Reset Call (SWRST Call) allows all the devices in the I<sup>2</sup>C-bus to be reset to the power-up state value through a specific formatted I<sup>2</sup>C-bus command. To be performed correctly, it implies that the I<sup>2</sup>C-bus is functional and that there is no device hanging the bus.

The maximum wait time after software reset is 1 ms.

The SWRST Call function is defined as the following:

1. A START command is sent by the I<sup>2</sup>C-bus master.
2. The reserved General Call address '0000 000' with the R/W bit set to '0' (write only) is sent by the I<sup>2</sup>C-bus master.
3. The PCU9955A device is a U<sup>2</sup>Fm write-only I<sup>2</sup>C-bus, no acknowledge is returned to the I<sup>2</sup>C-bus master.
4. Once the General Call address has been sent, the master sends 1 byte with 1 specific value (SWRST data byte 1): Byte 1 = 06h.  
If more than 1 byte of data is sent, they are ignored by the PCU9955A.
5. Once the correct byte (SWRST data byte 1) has been sent, the master sends a STOP condition to end the SWRST function: the PCU9955A then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time ( $t_{BUF}$ ).

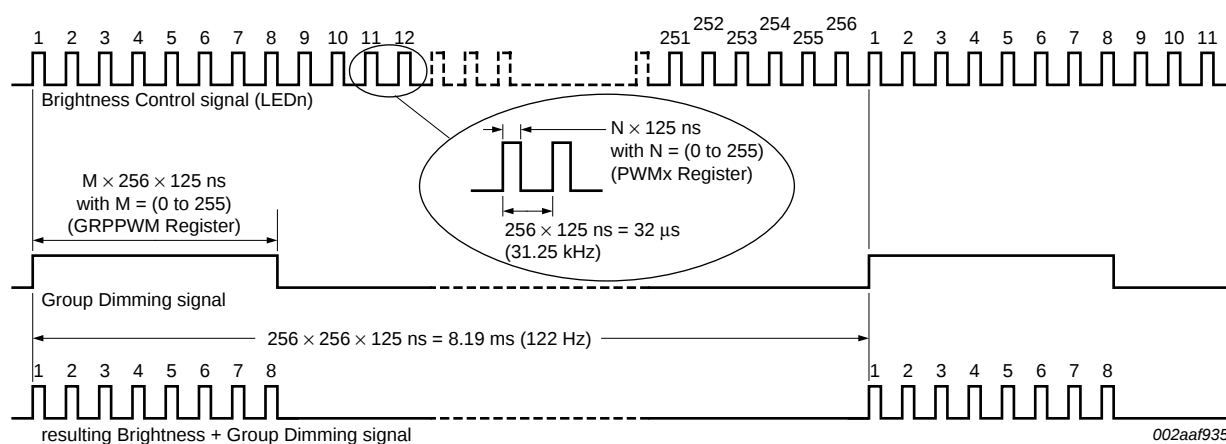


## 7.8 Individual brightness control with group dimming/blinking

A 31.25 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 16 LED outputs LED0 to LED15).

- A lower 122 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 15 Hz to every 16.8 seconds (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.



Minimum pulse width for LEDn Brightness Control is 125 ns.

Minimum pulse width for Group Dimming is 32  $\mu\text{s}$ .

When  $M = 1$  (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal has 1 pulse of the LED Brightness Control signal (pulse width =  $N \times 125 \text{ ns}$ , with 'N' defined in PWMx register).

This resulting Brightness + Group Dimming signal above shows a resulting Control signal with  $M = 8$ .

**Fig 14. Brightness + Group Dimming signals**

## 8. Characteristics of the PCU9955A Ultra Fast-mode I<sup>2</sup>C-bus

The PCU9955A LED controller uses the new Ultra Fast-mode (UFm) I<sup>2</sup>C-bus to communicate with the UFm I<sup>2</sup>C-bus capable host controller. Like the Standard mode and Fast-mode Plus (Fm+) I<sup>2</sup>C-bus, it uses two lines for communication. They are a serial data line (USDA) and a serial clock line (USCL). The UFm is a unidirectional bus, which is capable of higher frequency (up to 5 MHz). The UFm I<sup>2</sup>C-bus slave devices operate in receive-only mode. That is, only I<sup>2</sup>C writes to PCU9955A are supported.

### 8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the USDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 15](#)).

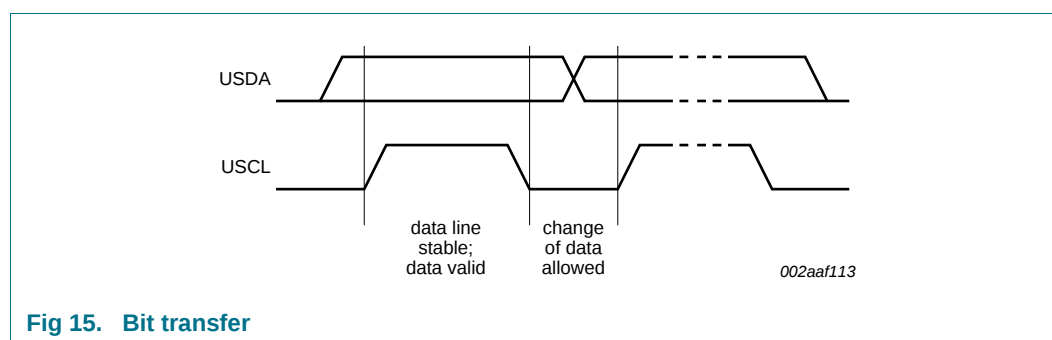


Fig 15. Bit transfer

#### 8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 16](#)).

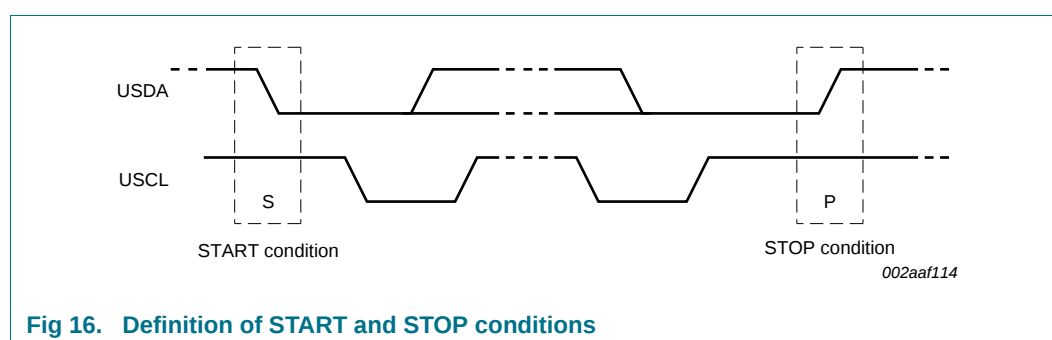


Fig 16. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see [Figure 17](#)).

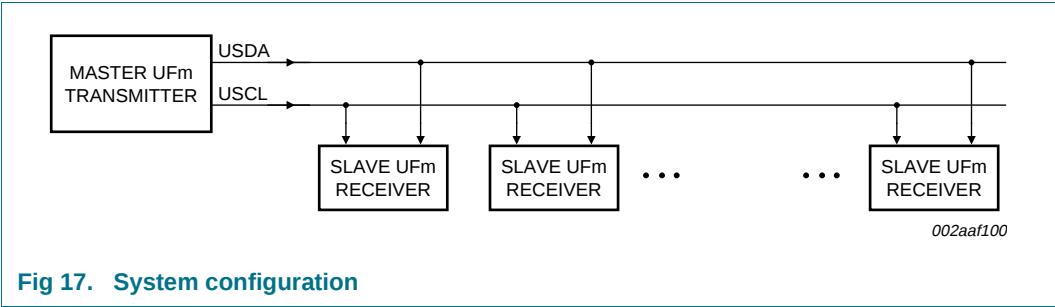


Fig 17. System configuration

8.3 Data transfer

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of 8 bits is followed by 1 bit that is always set to 1. The master generates an extra related clock pulse.

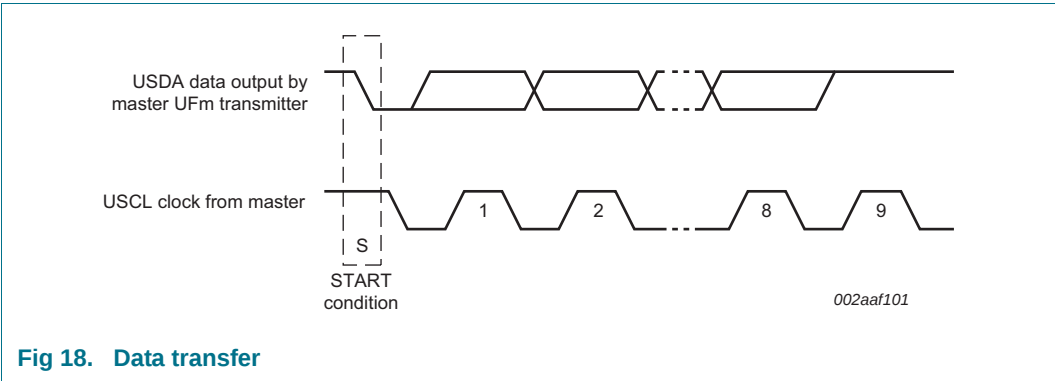
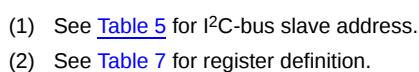


Fig 18. Data transfer

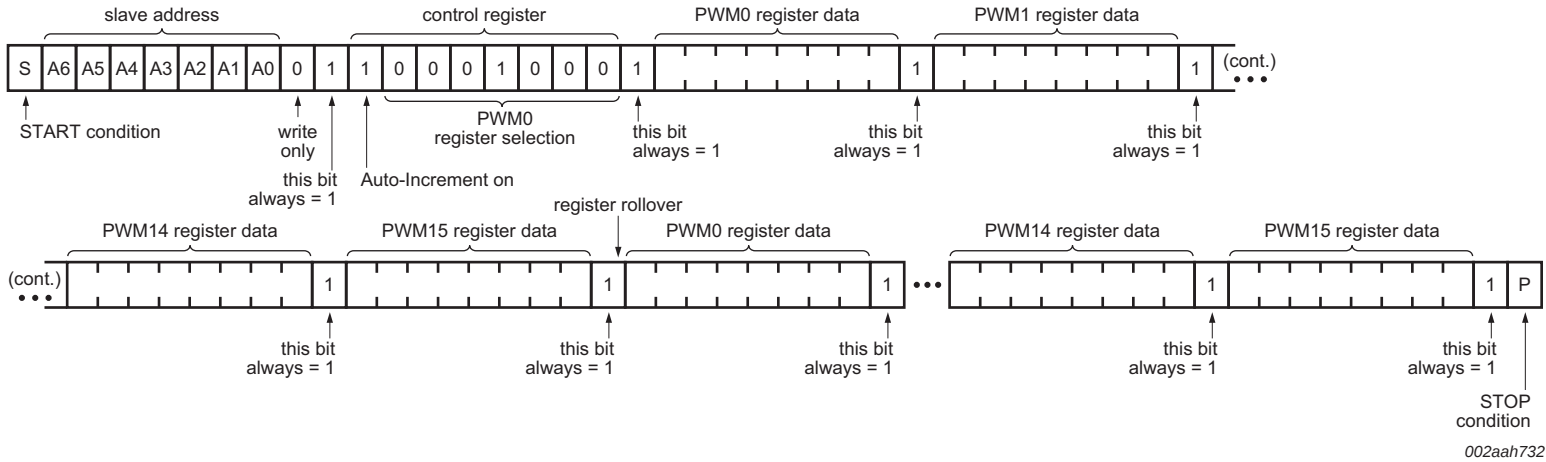


### Fig 19. Write to a specific register



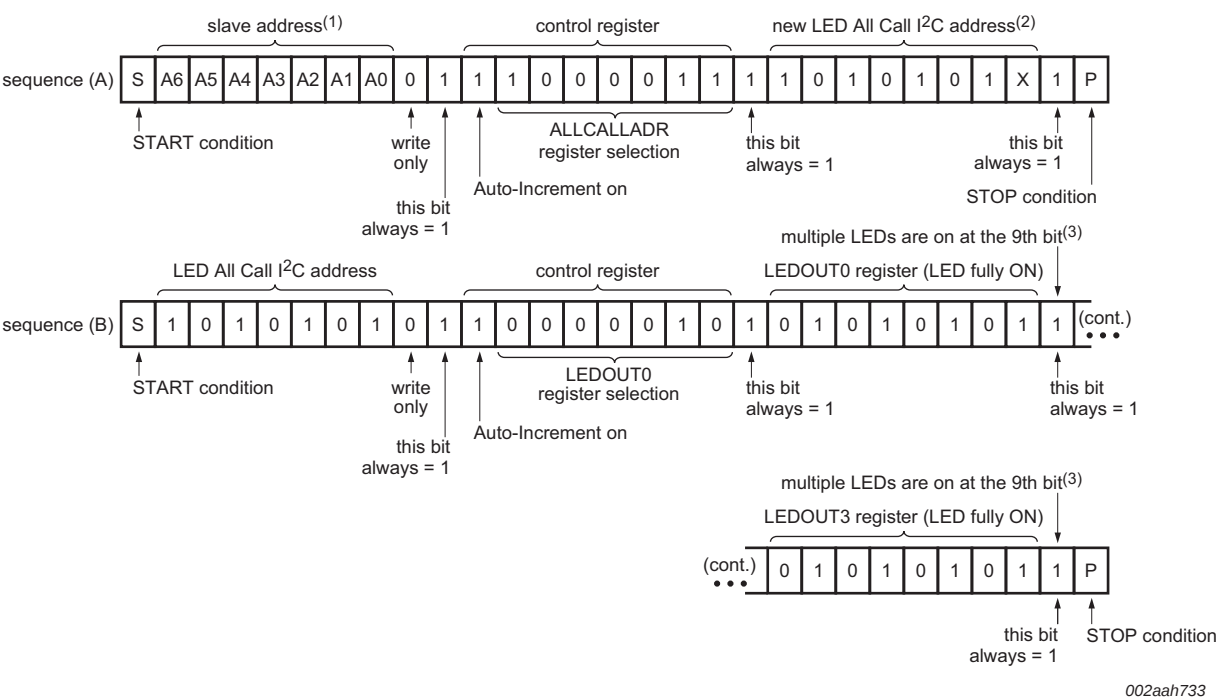
**Remark:** Care should be taken to load the appropriate value here in the AI1 and AI0 bits of the MODE1 register for programming the part with the required Auto-Increment options.

**Fig 20. Write to all registers using the Auto-Increment feature**



This example assumes that AIF + AI[1:0] = 101b.

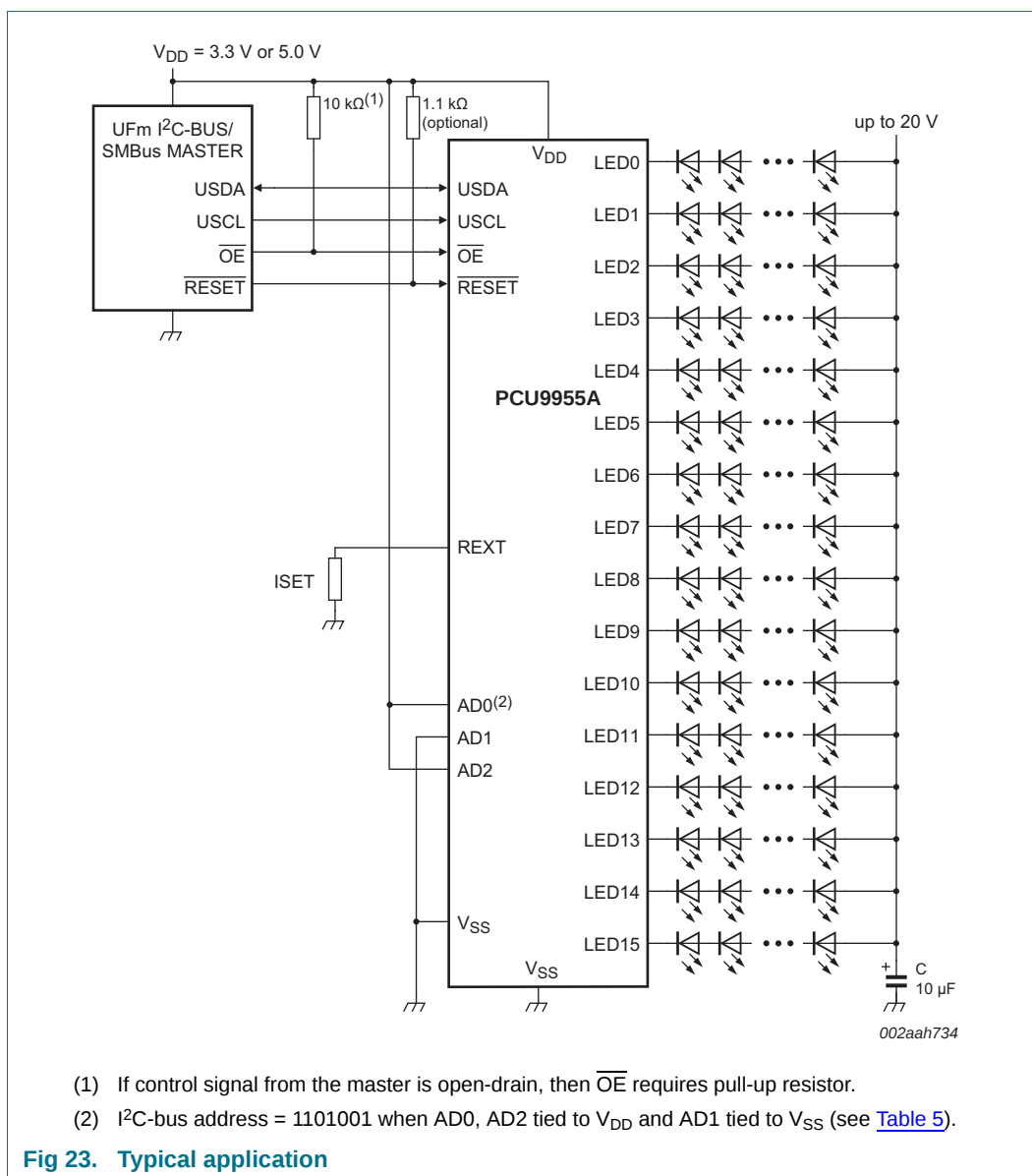
Fig 21. Multiple writes to Individual Brightness registers only using the Auto-Increment feature



- (1) In this example, several PCU9955As are used and the same sequence (A) (above) is sent to each of them.
- (2) ALLCALL bit in MODE1 register is previously set to 1 for this example.
- (3) OCH bit in MODE2 register is previously set to 1 for this example.

Fig 22. LED All Call I<sup>2</sup>C-bus address programming and LED All Call sequence example

## 10. Application design-in information



### 10.1 Thermal considerations

Since the PCU9955A device integrates 16 linear current sources, thermal considerations should be taken into account to prevent overheating, which can cause the device to go into thermal shutdown.

Perhaps the major contributor for device's overheating is the LED forward voltage mismatch. This is because it can cause significant voltage differences between the LED strings of the same type (for example, 2 V to 3 V), which ultimately translates into higher power dissipation in the device. The voltage drop across the LED channels of the device is given by the difference between the supply voltage and the LED forward voltage of each

LED string. Reducing this to a minimum (for example, 0.8 V) helps to keep the power dissipation down. Therefore LEDs binning is recommended to minimize LED voltage forward variation and reduce power dissipation in the device.

In order to ensure that the device does not go into thermal shutdown when operating under certain application conditions, its junction temperature ( $T_j$ ) should be calculated to ensure that is below the overtemperature threshold limit (130 °C). The  $T_j$  of the device depends on the ambient temperature ( $T_{amb}$ ), device total power dissipation ( $P_{tot}$ ), and thermal resistance.

The device junction temperature can be calculated by using the following equation:

$$T_j = T_{amb} + R_{th(j-a)} \times P_{tot} \quad (6)$$

where:

$T_j$  = junction temperature

$T_{amb}$  = ambient temperature

$R_{th(j-a)}$  = junction to ambient thermal resistance

$P_{tot}$  = (device) total power dissipation

An example of this calculation is show below:

**Conditions:**

$T_{amb} = 50\text{ °C}$

$R_{th(j-a)} = 39\text{ °C/W}$  (per JEDEC 51 standard for multilayer PCB)

$I_{LED} = 30\text{ mA / channel}$

$I_{DD(max)} = 20\text{ mA}$

$V_{DD} = 5\text{ V}$

LEDs per channel = 5 LEDs / channel

LED  $V_{F(typ)} = 3\text{ V}$  per LED (15 V total for 5 LEDs in series)

LED  $V_F$  mismatch = 0.2 V per LED (1 V total for 5 LEDs in series)

$V_{reg(drv)} = 0.8\text{ V}$  (This is present only in the LED string with the highest LED forward voltage.)

$V_{sup} = \text{LED } V_{F(typ)} + \text{LED } V_F \text{ mismatch} + V_{reg(drv)} = 15\text{ V} + 1\text{ V} + 0.8\text{ V} = 16.8\text{ V}$

**$P_{tot}$  calculation:**

$P_{tot} = IC\_power + LED\ drivers\_power;$

$IC\_power = (I_{DD} \times V_{DD})$

$IC\_power = (0.02\text{ A} \times 5\text{ V}) = 0.1\text{ W}$

$LED\ drivers\_power = [(16 - 1) \times (I_{LED}) \times (LED\ V_F \text{ mismatch} + V_{reg(drv)})] + (I_{LED} \times V_{reg(drv)})$

$LED\ drivers\_power = [15 \times 0.03\text{ A} \times (1\text{ V} + 0.8\text{ V})] + (0.03\text{ A} \times 0.8\text{ V}) = 0.834\text{ W}$

$P_{tot} = 0.1\text{ W} + 0.834\text{ W} = 0.934\text{ W}$

**T<sub>j</sub> calculation:**

$$T_j = T_{amb} + R_{th(j-a)} \times P_{tot}$$

$$T_j = 50\text{ °C} + (39\text{ °C/W} \times 0.934\text{ W}) = 86.426\text{ °C}$$

This confirms that the junction temperature is below the minimum overtemperature threshold of 130 °C, which ensures the device does not go into thermal shutdown under these conditions.

It is important to mention that the value of the thermal resistance junction-to-ambient ( $R_{th(j-a)}$ ) strongly depends in the PCB design. Therefore, the thermal pad of the device should be attached to a large enough PCB copper area to ensure proper thermal dissipation (similar to JEDEC 51 standard). Several thermal vias in the PCB thermal pad should be used as well to increase the effectiveness of the heat dissipation (for example, 15 thermal vias). The thermal vias should be distributed evenly in the PCB thermal pad.

Finally, it is important to point out that this calculation should be taken as a reference only and therefore evaluations should still be performed under the application environment and conditions to confirm proper system operation.

## 11. Limiting values

**Table 27. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol                | Parameter                      | Conditions               | Min                   | Max  | Unit |
|-----------------------|--------------------------------|--------------------------|-----------------------|------|------|
| V <sub>DD</sub>       | supply voltage                 |                          | −0.5                  | +6.0 | V    |
| V <sub>I/O</sub>      | voltage on an input/output pin |                          | V <sub>SS</sub> − 0.5 | 5.5  | V    |
| V <sub>drv(LED)</sub> | LED driver voltage             |                          | V <sub>SS</sub> − 0.5 | 20   | V    |
| I <sub>O(LEDn)</sub>  | output current on pin LEDn     |                          | -                     | 65   | mA   |
| I <sub>SS</sub>       | ground supply current          |                          | -                     | 1.0  | A    |
| P <sub>tot</sub>      | total power dissipation        | T <sub>amb</sub> = 25 °C | -                     | 2.56 | W    |
|                       |                                | T <sub>amb</sub> = 85 °C | -                     | 1.03 | W    |
| T <sub>stg</sub>      | storage temperature            |                          | −65                   | +150 | °C   |
| T <sub>amb</sub>      | ambient temperature            | operating                | −40                   | +85  | °C   |
| T <sub>j</sub>        | junction temperature           |                          | −40                   | +125 | °C   |

## 12. Thermal characteristics

**Table 28. Thermal characteristics**

| Symbol               | Parameter                                   | Conditions | Typ    | Unit |
|----------------------|---------------------------------------------|------------|--------|------|
| R <sub>th(j-a)</sub> | thermal resistance from junction to ambient | HTSSOP28   | [1] 39 | °C/W |

[1] Per JEDEC 51 standard for multilayer PCB and Wind Speed (m/s) = 0.

## 13. Static characteristics

**Table 29. Static characteristics**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

| Symbol                                        | Parameter                              | Conditions                                                                                                                                                     | Min          | Typ <sup>[1]</sup> | Max           | Unit          |
|-----------------------------------------------|----------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------------|---------------|---------------|
| <b>Supply</b>                                 |                                        |                                                                                                                                                                |              |                    |               |               |
| $V_{DD}$                                      | supply voltage                         |                                                                                                                                                                | 3            | -                  | 5.5           | V             |
| $I_{DD}$                                      | supply current                         | on pin $V_{DD}$ ; operating mode;<br>$f_{SCL} = 1\text{ MHz}$                                                                                                  |              |                    |               |               |
|                                               |                                        | $R_{ext} = 2\text{ k}\Omega$ ; LED[15:0] = off;<br>IREF <sub>x</sub> = 00h                                                                                     | -            | 11                 | 12            | mA            |
|                                               |                                        | $R_{ext} = 1\text{ k}\Omega$ ; LED[15:0] = off;<br>IREF <sub>x</sub> = 00h                                                                                     | -            | 13                 | 14            | mA            |
|                                               |                                        | $R_{ext} = 2\text{ k}\Omega$ ; LED[15:0] = on;<br>IREF <sub>x</sub> = FFh                                                                                      | -            | 15                 | 19            | mA            |
|                                               |                                        | $R_{ext} = 1\text{ k}\Omega$ ; LED[15:0] = on;<br>IREF <sub>x</sub> = FFh                                                                                      | -            | 17                 | 21            | mA            |
| $I_{stb}$                                     | standby current                        | on pin $V_{DD}$ ; no load; $f_{SCL} = 0\text{ Hz}$ ;<br>MODE1[4] = 1; $V_I = V_{DD}$                                                                           |              |                    |               |               |
|                                               |                                        | $V_{DD} = 3.3\text{ V}$                                                                                                                                        | -            | 170                | 600           | $\mu\text{A}$ |
|                                               |                                        | $V_{DD} = 5.5\text{ V}$                                                                                                                                        | -            | 170                | 700           | $\mu\text{A}$ |
| $V_{POR}$                                     | power-on reset voltage                 | no load; $V_I = V_{DD}$ or $V_{SS}$                                                                                                                            | -            | 2                  | -             | V             |
| $V_{PDR}$                                     | power-down reset voltage               | no load; $V_I = V_{DD}$ or $V_{SS}$ <sup>[2]</sup>                                                                                                             | -            | 1                  | -             | V             |
| <b>Inputs USCL, USDA</b>                      |                                        |                                                                                                                                                                |              |                    |               |               |
| $V_{IL}$                                      | LOW-level input voltage                |                                                                                                                                                                | -0.5         | -                  | +0.3 $V_{DD}$ | V             |
| $V_{IH}$                                      | HIGH-level input voltage               |                                                                                                                                                                | 0.7 $V_{DD}$ | -                  | 5.5           | V             |
| $I_L$                                         | leakage current                        | $V_I = V_{DD}$ or $V_{SS}$                                                                                                                                     | -1           | -                  | +1            | $\mu\text{A}$ |
| $C_i$                                         | input capacitance                      | $V_I = V_{SS}$                                                                                                                                                 | -            | 6                  | 10            | pF            |
| <b>Current controlled outputs (LED[15:0])</b> |                                        |                                                                                                                                                                |              |                    |               |               |
| $I_{O(LEDn)}$                                 | output current on pin LED <sub>n</sub> | $V_O = 0.8\text{ V}$ ; IREF <sub>x</sub> = 80h; $R_{ext} = 1\text{ k}\Omega$                                                                                   | 25           | -                  | 30            | mA            |
|                                               |                                        | $V_O = 0.8\text{ V}$ ; IREF <sub>x</sub> = FFh; $R_{ext} = 1\text{ k}\Omega$                                                                                   | 50           | -                  | 60            | mA            |
| $\Delta I_O$                                  | output current variation               | $V_{DD} = 3.0\text{ V}$ ; $T_{amb} = 25\text{ °C}$ ; $V_O = 0.8\text{ V}$ ;<br>IREF <sub>x</sub> = 80h; $R_{ext} = 1\text{ k}\Omega$ ; guaranteed<br>by design |              |                    |               |               |
|                                               |                                        | between bits (different ICs, same channel) <sup>[3]</sup>                                                                                                      | -            | -                  | ±6            | %             |
|                                               |                                        | between bits (2 channels, same IC) <sup>[4]</sup>                                                                                                              | -            | -                  | ±4            | %             |
| $V_{reg(drv)}$                                | driver regulation voltage              | minimum regulation voltage;<br>IREF <sub>x</sub> = FFh; $R_{ext} = 1\text{ k}\Omega$                                                                           | 0.8          | 1                  | 20            | V             |
| $I_{L(off)}$                                  | off-state leakage current              | $V_O = 20\text{ V}$                                                                                                                                            | -            | -                  | 1             | $\mu\text{A}$ |
| <b>OE input, RESET input</b>                  |                                        |                                                                                                                                                                |              |                    |               |               |
| $V_{IL}$                                      | LOW-level input voltage                |                                                                                                                                                                | -0.5         | -                  | +0.3 $V_{DD}$ | V             |
| $V_{IH}$                                      | HIGH-level input voltage               |                                                                                                                                                                | 0.7 $V_{DD}$ | -                  | 5.5           | V             |
| $I_{LI}$                                      | input leakage current                  |                                                                                                                                                                | -1           | -                  | +1            | $\mu\text{A}$ |
| $C_i$                                         | input capacitance                      |                                                                                                                                                                | -            | 3.7                | 5             | pF            |

**Table 29. Static characteristics ...continued**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

| Symbol                              | Parameter                                        | Conditions              | Min  | Typ <sup>[1]</sup> | Max | Unit |
|-------------------------------------|--------------------------------------------------|-------------------------|------|--------------------|-----|------|
| <b>Address inputs AD2, AD1, AD0</b> |                                                  |                         |      |                    |     |      |
| $V_I$                               | input voltage                                    | voltage on an input pin | -0.5 | -                  | 5.5 | V    |
| $I_{LI}$                            | input leakage current                            |                         | -1   | -                  | +1  | μA   |
| $C_i$                               | input capacitance                                |                         | -    | 3.7                | 5   | pF   |
| <b>Overtemperature protection</b>   |                                                  |                         |      |                    |     |      |
| $T_{th(otp)}$                       | overtemperature protection threshold temperature | rising                  | 130  | -                  | 150 | °C   |
|                                     |                                                  | hysteresis              | 15   | -                  | 30  | °C   |

[1] Typical limits at  $V_{DD} = 3.3\text{ V}$ ,  $T_{amb} = 25\text{ °C}$ .

[2] In order to reset part,  $V_{DD}$  must be lowered to 1 V.

[3] Part-to-part mismatch is calculated:

$$\Delta\% = \left( \frac{\left( \frac{I_{O(LED0)} + I_{O(LED1)} + \dots + I_{O(LED14)} + I_{O(LED15)}}{16} - \text{ideal output current} \right)}{\text{ideal output current}} \right) \times 100$$

where 'ideal output current' = 28.68 mA ( $R_{ext} = 1\text{ k}\Omega$ ,  $I_{REFx} = 80\text{h}$ ).

[4] Channel-to-channel mismatch is calculated:

$$\Delta\% = \left( \frac{I_{O(LEDn)} \text{ (where } n = 0 \text{ to } 15)}{\left( \frac{I_{O(LED0)} + I_{O(LED1)} + \dots + I_{O(LED14)} + I_{O(LED15)}}{16} \right)} - 1 \right) \times 100$$

## 14. Dynamic characteristics

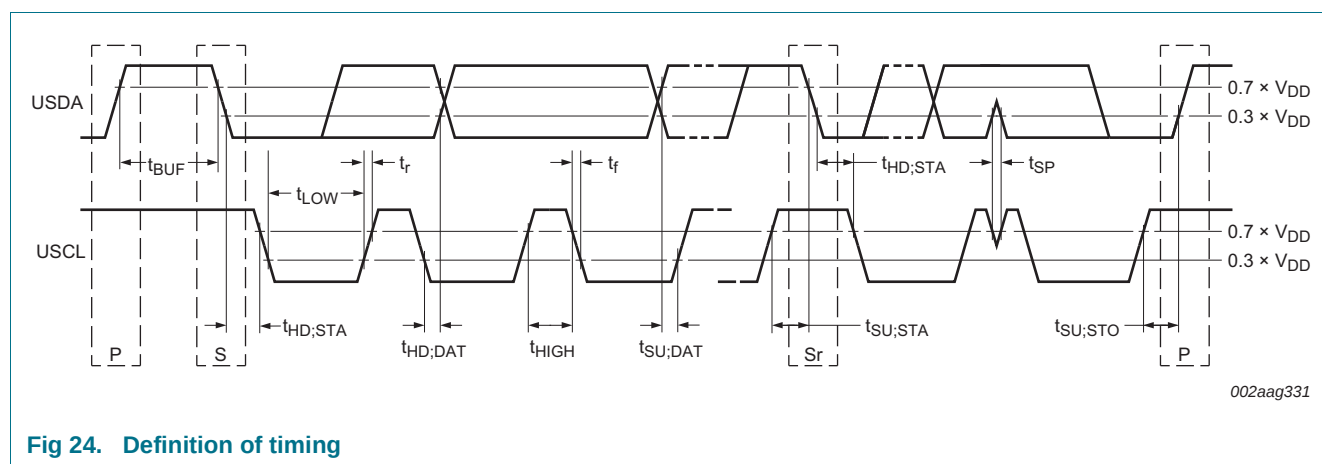
**Table 30. Dynamic characteristics**

All the timing limits are valid within the operating supply voltage and ambient temperature range;  $V_{DD} = 3\text{ V} \pm 0.2\text{ V}$  and  $5.5\text{ V} \pm 0.3\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ; and refer to  $V_{IL}$  and  $V_{IH}$  with an input voltage of  $V_{SS}$  to  $V_{DD}$ .

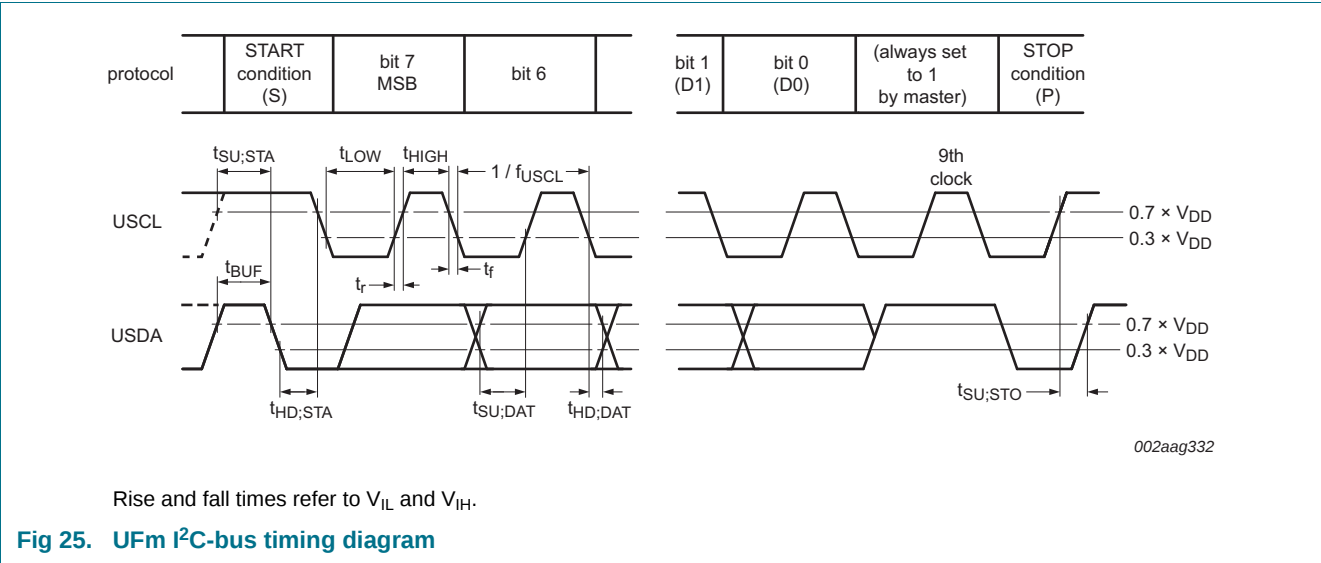
| Symbol       | Parameter                                                         | Conditions | Min  | Typ | Max  | Unit          |
|--------------|-------------------------------------------------------------------|------------|------|-----|------|---------------|
| $f_{USCL}$   | USCL clock frequency                                              | [1]        | 0    | -   | 5000 | kHz           |
| $t_{BUF}$    | bus free time between a STOP and START condition                  |            | 0.08 | -   | -    | $\mu\text{s}$ |
| $t_{HD;STA}$ | hold time (repeated) START condition                              |            | 0.05 | -   | -    | $\mu\text{s}$ |
| $t_{SU;STA}$ | set-up time for a repeated START condition                        |            | 0.05 | -   | -    | $\mu\text{s}$ |
| $t_{SU;STO}$ | set-up time for STOP condition                                    |            | 0.05 | -   | -    | $\mu\text{s}$ |
| $t_{HD;DAT}$ | data hold time                                                    |            | 10   | -   | -    | ns            |
| $t_{VD;DAT}$ | data valid time                                                   | [2]        | -    | -   | -    | ns            |
| $t_{SU;DAT}$ | data set-up time                                                  |            | 30   | -   | -    | ns            |
| $t_{LOW}$    | LOW period of the USCL clock                                      |            | 50   | -   | -    | ns            |
| $t_{HIGH}$   | HIGH period of the USCL clock                                     |            | 50   | -   | -    | ns            |
| $t_f$        | fall time of both USDA and USCL signals                           |            | -    | -   | 50   | ns            |
| $t_r$        | rise time of both USDA and USCL signals                           |            | -    | -   | 50   | ns            |
| $t_{SP}$     | pulse width of spikes that must be suppressed by the input filter |            | -    | -   | 10   | ns            |

[1] Minimum USCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either USDA or USCL is held LOW for a minimum of 25 ms. Disable bus time-out feature for DC operation.

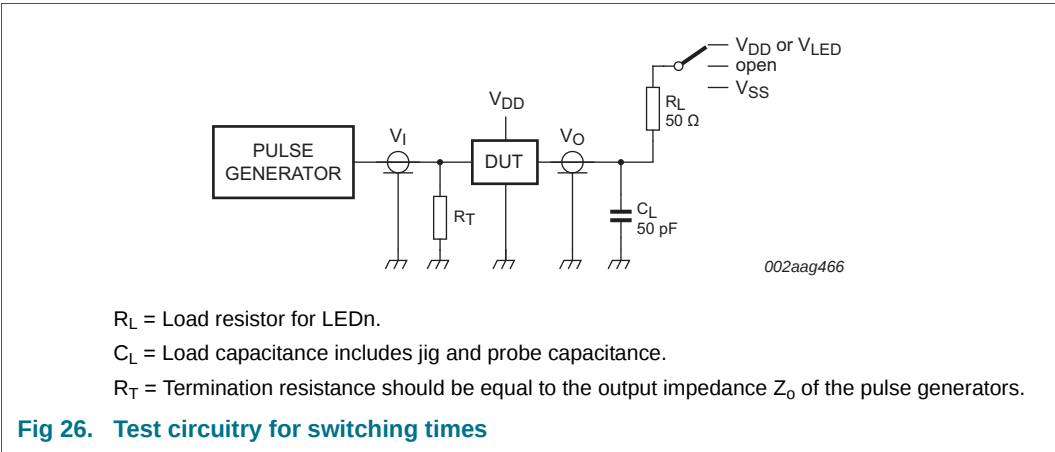
[2]  $t_{VD;DAT}$  is not applicable to the U<sup>2</sup>Fm I<sup>2</sup>C-bus slave device.



**Fig 24. Definition of timing**



15. Test information



16. Package outline

HTSSOP28: plastic thermal enhanced thin shrink small outline package; 28 leads;  
body width 4.4 mm; lead pitch 0.65 mm; exposed die pad

SOT1172-3

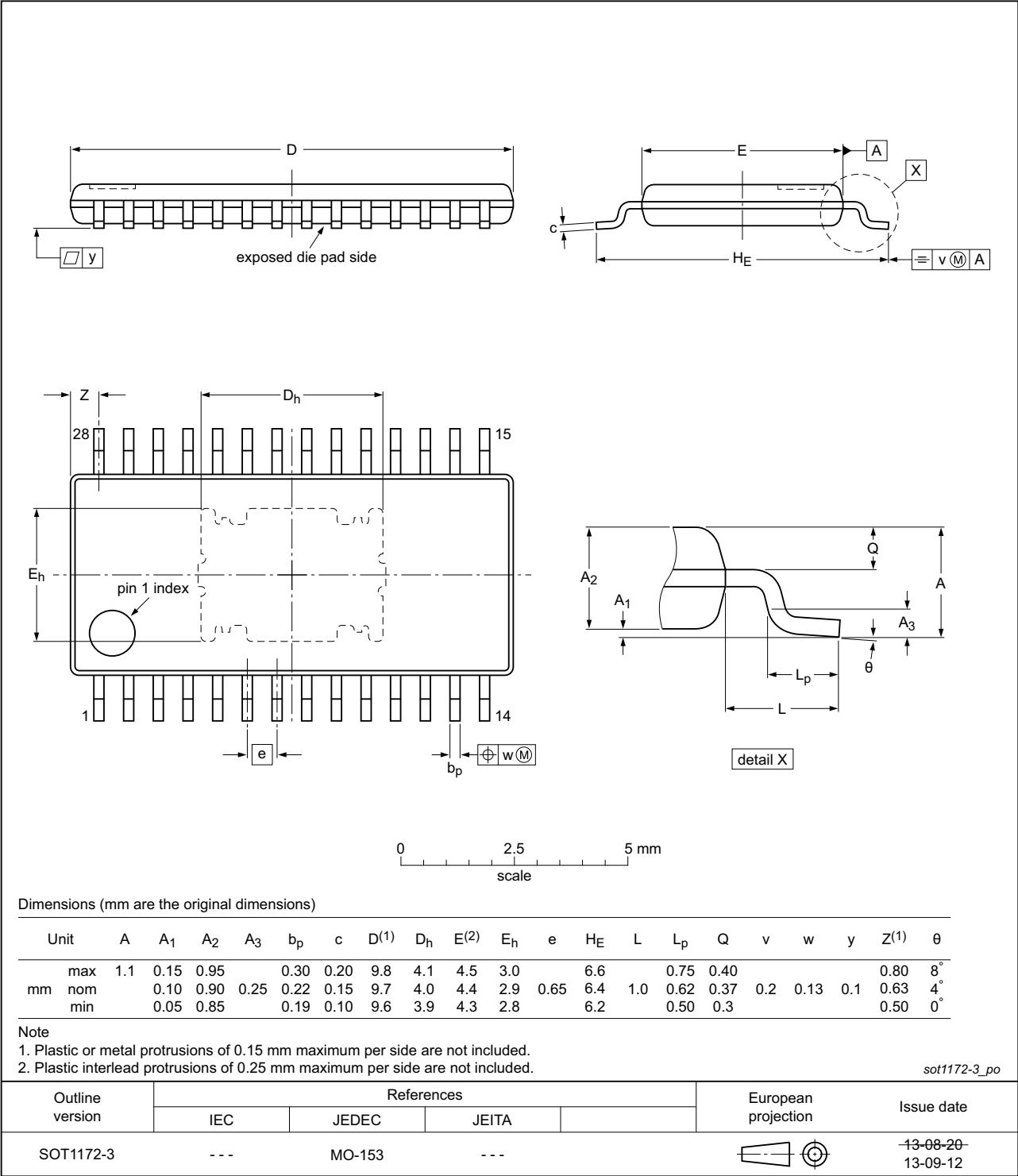


Fig 27. Package outline SOT1172-3 (HTSSOP28)

## 17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in JESD625-A or equivalent standards.

## 18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “*Surface mount reflow soldering description*”.

### 18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 28](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 31](#) and [32](#)

**Table 31. SnPb eutectic process (from J-STD-020D)**

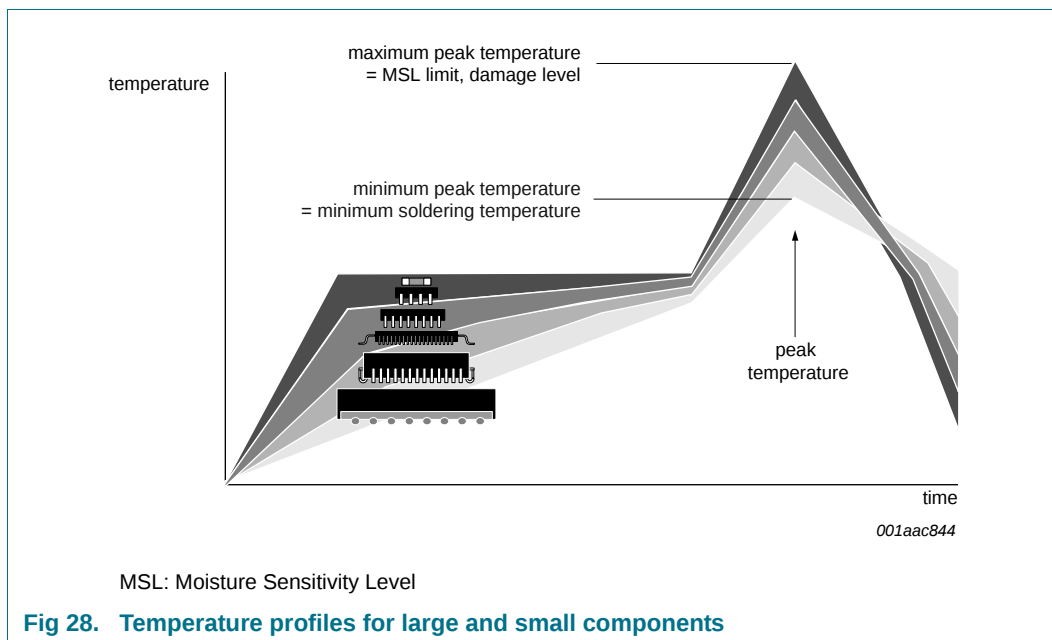
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 32. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

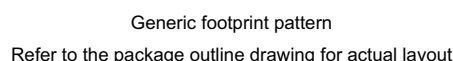
Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 28](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

**SOT1172-3**



— — — — occupied area

DIMENSIONS in mm

|            |                                 |
|------------|---------------------------------|
| Issue date | <del>13-08-20</del><br>13-10-07 |
|------------|---------------------------------|

sot1172-3 fr

**Fig 29. PCB footprint for SOT1172-3 (HTSSOP28); reflow soldering**

## 20. Abbreviations

Table 33. Abbreviations

| Acronym              | Description                                |
|----------------------|--------------------------------------------|
| ACK                  | Acknowledge                                |
| CDM                  | Charged-Device Model                       |
| DAC                  | Digital-to-Analog Converter                |
| DUT                  | Device Under Test                          |
| ESD                  | ElectroStatic Discharge                    |
| FET                  | Field-Effect Transistor                    |
| HBM                  | Human Body Model                           |
| I <sup>2</sup> C-bus | Inter-Integrated Circuit bus               |
| LED                  | Light Emitting Diode                       |
| LSB                  | Least Significant Bit                      |
| MCU                  | MicroController Unit                       |
| MSB                  | Most Significant Bit                       |
| NMOS                 | Negative-channel Metal-Oxide Semiconductor |
| PCB                  | Printed-Circuit Board                      |
| PMOS                 | Positive-channel Metal-Oxide Semiconductor |
| PWM                  | Pulse Width Modulation                     |
| RGB                  | Red/Green/Blue                             |
| RGBA                 | Red/Green/Blue/Amber                       |
| SMBus                | System Management Bus                      |

## 21. Revision history

Table 34. Revision history

| Document ID    | Release date                                                                                                                                                                                                                                                                 | Data sheet status      | Change notice | Supersedes   |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|---------------|--------------|
| PCU9955A v.3.1 | 20150629                                                                                                                                                                                                                                                                     | Product data sheet     | -             | PCU9955A v.3 |
| Modifications: | <ul style="list-style-type: none"> <li><a href="#">Section 7.3.3 "LEDOUT0 to LEDOUT3, LED driver output state"</a>: added remark.</li> <li><a href="#">Table 8 "MODE1 - Mode register 1 (address 00h) bit description"</a>: added <a href="#">Table note [3]</a>.</li> </ul> |                        |               |              |
| PCU9955A v.3   | 20141014                                                                                                                                                                                                                                                                     | Product data sheet     | -             | PCU9955A v.2 |
| Modifications: | <ul style="list-style-type: none"> <li><a href="#">Section 7.5 "Power-on reset"</a>: added remark.</li> </ul>                                                                                                                                                                |                        |               |              |
| PCU9955A v.2   | 20140522                                                                                                                                                                                                                                                                     | Product data sheet     | -             | PCU9955A v.1 |
| PCU9955A v.1   | 20140210                                                                                                                                                                                                                                                                     | Preliminary data sheet | -             | -            |

## 22. Legal information

### 22.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 22.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 22.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's

own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 22.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP Semiconductors N.V.

## 23. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 24. Contents

|          |                                                                               |          |           |                                                                           |           |
|----------|-------------------------------------------------------------------------------|----------|-----------|---------------------------------------------------------------------------|-----------|
| <b>1</b> | <b>General description</b> . . . . .                                          | <b>1</b> | 7.3.9     | OFFSET — LEDn output delay offset register                                | 29        |
| <b>2</b> | <b>Features and benefits</b> . . . . .                                        | <b>2</b> | 7.3.10    | LED Sub Call I <sup>2</sup> C-bus addresses for PCU9955A                  | 30        |
| <b>3</b> | <b>Applications</b> . . . . .                                                 | <b>3</b> | 7.3.11    | ALLCALLADR, LED All Call I <sup>2</sup> C-bus address                     | 30        |
| <b>4</b> | <b>Ordering information</b> . . . . .                                         | <b>4</b> | 7.3.12    | PWMALL — brightness control for all LEDn outputs                          | 31        |
| 4.1      | Ordering options . . . . .                                                    | 4        | 7.3.13    | IREFALL register: output current value for all LED outputs                | 31        |
| <b>5</b> | <b>Block diagram</b> . . . . .                                                | <b>5</b> | 7.3.14    | LED driver constant current outputs                                       | 31        |
| <b>6</b> | <b>Pinning information</b> . . . . .                                          | <b>6</b> | 7.3.14.1  | Adjusting output current                                                  | 31        |
| 6.1      | Pinning . . . . .                                                             | 6        | 7.3.15    | Overtemperature protection                                                | 33        |
| 6.2      | Pin description . . . . .                                                     | 6        | 7.4       | Active LOW output enable input                                            | 33        |
| <b>7</b> | <b>Functional description</b> . . . . .                                       | <b>7</b> | 7.5       | Power-on reset                                                            | 34        |
| 7.1      | Device addresses . . . . .                                                    | 7        | 7.6       | Hardware reset recovery                                                   | 34        |
| 7.1.1    | Regular I <sup>2</sup> C-bus slave address . . . . .                          | 7        | 7.7       | Software reset                                                            | 34        |
| 7.1.2    | LED All Call I <sup>2</sup> C-bus address . . . . .                           | 11       | 7.8       | Individual brightness control with group dimming/blinking                 | 36        |
| 7.1.3    | LED Sub Call I <sup>2</sup> C-bus addresses . . . . .                         | 12       | <b>8</b>  | <b>Characteristics of the PCU9955A Ultra Fast-mode I<sup>2</sup>C-bus</b> | <b>37</b> |
| 7.2      | Control register . . . . .                                                    | 12       | 8.1       | Bit transfer                                                              | 37        |
| 7.3      | Register definitions . . . . .                                                | 14       | 8.1.1     | START and STOP conditions                                                 | 37        |
| 7.3.1    | MODE1 — Mode register 1 . . . . .                                             | 16       | 8.2       | System configuration                                                      | 38        |
| 7.3.2    | MODE2 — Mode register 2 . . . . .                                             | 17       | 8.3       | Data transfer                                                             | 38        |
| 7.3.3    | LEDOUT0 to LEDOUT3, LED driver output state . . . . .                         | 18       | <b>9</b>  | <b>Bus transactions</b>                                                   | <b>39</b> |
| 7.3.4    | GRPPWM, group duty cycle control . . . . .                                    | 18       | <b>10</b> | <b>Application design-in information</b>                                  | <b>42</b> |
| 7.3.5    | GRPFREQ, group frequency . . . . .                                            | 19       | 10.1      | Thermal considerations                                                    | 42        |
| 7.3.6    | PWM0 to PWM15, individual brightness control . . . . .                        | 19       | <b>11</b> | <b>Limiting values</b>                                                    | <b>44</b> |
| 7.3.7    | IREF0 to IREF15, LED output current value registers . . . . .                 | 20       | <b>12</b> | <b>Thermal characteristics</b>                                            | <b>44</b> |
| 7.3.8    | Gradation control . . . . .                                                   | 21       | <b>13</b> | <b>Static characteristics</b>                                             | <b>45</b> |
| 7.3.8.1  | RAMP_RATE_GRP0 to RAMP_RATE_GRP3, ramp rate control registers . . . . .       | 22       | <b>14</b> | <b>Dynamic characteristics</b>                                            | <b>47</b> |
| 7.3.8.2  | STEP_TIME_GRP0 to STEP_TIME_GRP3, step time control registers . . . . .       | 22       | <b>15</b> | <b>Test information</b>                                                   | <b>48</b> |
| 7.3.8.3  | HOLD_CNTL_GRP0 to HOLD_CNTL_GRP3, hold ON and OFF control registers . . . . . | 23       | <b>16</b> | <b>Package outline</b>                                                    | <b>49</b> |
| 7.3.8.4  | IREF_GRP0 to IREF_GRP3, output gain control . . . . .                         | 23       | <b>17</b> | <b>Handling information</b>                                               | <b>50</b> |
| 7.3.8.5  | GRAD_MODE_SEL0 to GRAD_MODE_SEL1, gradation mode select registers . . . . .   | 24       | <b>18</b> | <b>Soldering of SMD packages</b>                                          | <b>50</b> |
| 7.3.8.6  | GRAD_GRP_SEL0 to GRAD_GRP_SEL3, gradation group select registers . . . . .    | 24       | 18.1      | Introduction to soldering                                                 | 50        |
| 7.3.8.7  | GRAD_CNTL, Gradation control register . . . . .                               | 25       | 18.2      | Wave and reflow soldering                                                 | 50        |
| 7.3.8.8  | Ramp control — equation and calculation example . . . . .                     | 26       | 18.3      | Wave soldering                                                            | 50        |
|          |                                                                               |          | 18.4      | Reflow soldering                                                          | 51        |
|          |                                                                               |          | <b>19</b> | <b>Soldering: PCB footprints</b>                                          | <b>53</b> |
|          |                                                                               |          | <b>20</b> | <b>Abbreviations</b>                                                      | <b>54</b> |
|          |                                                                               |          | <b>21</b> | <b>Revision history</b>                                                   | <b>54</b> |

continued &gt;&gt;

|           |                                      |           |
|-----------|--------------------------------------|-----------|
| <b>22</b> | <b>Legal information</b> . . . . .   | <b>55</b> |
| 22.1      | Data sheet status . . . . .          | 55        |
| 22.2      | Definitions . . . . .                | 55        |
| 22.3      | Disclaimers . . . . .                | 55        |
| 22.4      | Trademarks . . . . .                 | 56        |
| <b>23</b> | <b>Contact information</b> . . . . . | <b>56</b> |
| <b>24</b> | <b>Contents</b> . . . . .            | <b>57</b> |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2015.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 29 June 2015

Document identifier: PCU9955A