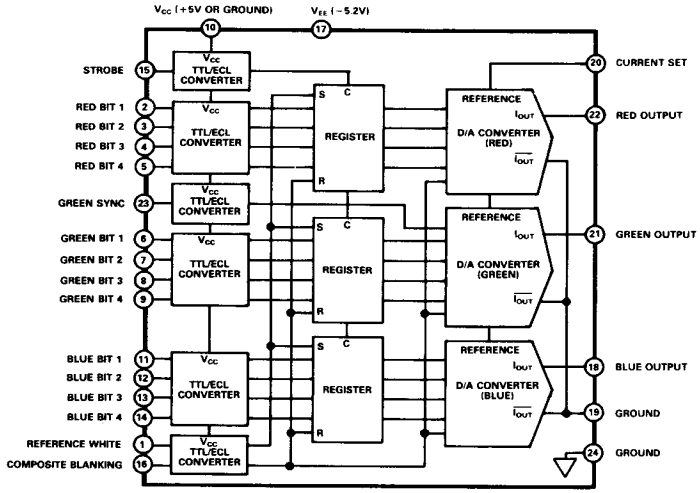
Triple 4-Bit D/A Converter

AD9702

FEATURES
ECL or TTL Compatible
Composite Inputs
125MHz Update Rates Minimum

APPLICATIONS
Raster Scan Displays
Color Graphics Systems
General Video Reconstruction

AD9702 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9702 D/A Converter is a single monolithic IC containing three separate 4-bit digital-to-analog (D/A) converters for red, green, blue (RGB) graphics display applications; 4,096 colors are available to the user. Composite blanking, green sync, and reference white digital control inputs are also included. On-chip data registers and a capability for varying output drive make this a *total* functional solution for graphics displays.

A unique TTL/ECL interface allows the designer a choice of logic compatibility for all inputs; this can be accomplished by applying either +5V or ground to the V_{CC} pin. Internally, the registers and control switching signals operate at ECL logic levels to help assure low glitch impulse at the DAC outputs.

The unit is housed in a 24-pin ceramic package and operates with −5.2V applied for the ECL mode; and −5.2V and +5V for TTL mode. Power dissipation is 1.3 watts for ECL operation and 1.5 watts for TTL.

Monolithic devices are inherently less expensive and more reliable than hybrids. When combined with its small size and outstanding electrical characteristics, these attributes make the AD9702 D/A Converter the first choice for designers of next-generation, medium-resolution displays.

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SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	AD9702BD/BW
RESOLUTION	Bits	4
LEAST SIGNIFICANT BIT (LSB) WEIGHT		
Voltage (Adjustable)	mV	40
Current (Adjustable)	mA	1
ACCURACY (GS = Gray Scale; FS = Full Scale)		
Linearity	±% GS	0.8
Differential Linearity	±% GS, max	0.8
Zero Offset (Initial)	mV, max	0.5
Monotonicity		Guaranteed
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C (max)	20 (30)
Zero Offset	ppm/°C (max)	10 (15)
Gain	ppm/°C (max)	200 (400)
Gain Tracking	ppm/°C	100
DYNAMIC CHARACTERISTICS		
Settling Time – Voltage[1]		
ECL Mode (to ±3.2% GS)	ns, max	5
TTL Mode (to ±3.2% GS)	ns, max	6
Update Rate		
ECL Mode	MHz, min	125
TTL Mode	MHz, min	75
Rise Time	ns	3
Glitch Impulse	pV-s	80
DIGITAL INPUTS		
Logic Compatibility		ECL/TTL
Coding		Binary (BIN)
ECL Logic Levels		
"1"	V (min/max)	−0.9 (−1.1/−0.6)
"0"	V (min/max)	−1.7 (−2.0/−1.5)
TTL Logic Levels		
"1"	V (min/max)	+3.5 (+2.0/+5.0)
"0"	V (min/max)	+0.2 (+0.0/+0.8)
Loading (Each Bit; with Typical Input Logic Levels)		
ECL "1"	µA/pF	50/5
ECL "0"	µA/pF	−100/5
TTL "1"	µA/pF	10/5
TTL "0"	mA/pF	1.5/5
Setup Time (Data)		
ECL	ns, max	2.5
TTL	ns, max	3.5
Hold Time (Data)		
ECL	ns, max	2
TTL	ns, max	3
Propagation Delay		
ECL	ns (max)	4 (5)
TTL	ns (max)	5 (6)
SPEED PERFORMANCE – CONTROL INPUTS		
ECL and TTL Settling Time to 10% of GS for:		
$\overline{\text{Reference White}}$	ns, max	10
$\overline{\text{Composite Blanking}}$	ns, max	10
$\overline{\text{Green Sync}}$	ns, max	10
10% Bright	ns	10
RED, GREEN, AND BLUE ANALOG OUTPUTS		
Gray Scale Current	mA	0 to −16
$\overline{\text{Ref White}}$[2] = "0"	mA	0
$\overline{\text{Ref White}}$ = "1"	mA	Normal Operation[3]
$\overline{\text{Composite Blanking}}$[4] = "0"	mA	−1.4
$\overline{\text{Composite Blanking}}$ = "1"	mA	Normal Operation
$\overline{\text{Green Sync}}$[5] = "0"	mA	−7.6
$\overline{\text{Green Sync}}$ = "1"	mA	Normal Operation
Gray Scale Voltage	mV	0 to −600 (±1%)
$\overline{\text{Ref White}}$[2] = "0"	mV	0
$\overline{\text{Ref White}}$ = "1"	mV	Normal Operation[3]
$\overline{\text{Composite Blanking}}$[4] = "0"	mV	−53
$\overline{\text{Composite Blanking}}$ = "1"	mV	Normal Operation
$\overline{\text{Green Sync}}$[5] = "0"	mV	−285
$\overline{\text{Green Sync}}$ = "1"	mV	Normal Operation

ABSOLUTE MAXIMUM RATINGS

	ECL Lower	ECL Upper	TTL Lower	TTL Upper
Supply Voltages				
V_{CC} (Pin 10)	−0.1V	+1.0V	0.0V	+6.0V
V_{EE} (Pin 17)	−6.0V	+0.3	−6.0V	+0.3V
Power Dissipation (Nominal Voltages)	1.5W		1.8W	
D/A Output Current	30mA		30mA	
Temperature				
Operating (Case)	−55°C to +125°C		−55°C to +125°C	
Storage	−55°C to +150°C		−55°C to +150°C	

PIN DESIGNATIONS

(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
24	GROUND	1	$\overline{\text{REFERENCE WHITE}}$
23	$\overline{\text{GREEN SYNC}}$	2	RED BIT 1 (MSB)
22	RED OUTPUT	3	RED BIT 2
21	GREEN OUTPUT	4	RED BIT 3
20	CURRENT SET	5	RED BIT 4 (LSB)
19	GROUND	6	GREEN BIT 1 (MSB)
18	BLUE OUTPUT	7	GREEN BIT 2
17	V_{EE} (−5.2V)	8	GREEN BIT 3
16	$\overline{\text{COMPOSITE BLANKING}}$	9	GREEN BIT 4 (LSB)
15	STROBE	10	V_{CC} (+5V OR GROUND)
14	BLUE BIT 4 (LSB)	11	BLUE BIT 1 (MSB)
13	BLUE BIT 3	12	BLUE BIT 2

NOTE: FOR NORMAL OPERATION, CONNECT PINS 19 AND 24 TOGETHER AND TO LOW-IMPEDANCE GROUND PLANE AS CLOSE TO CASE AS POSSIBLE.

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Parameter	Units	AD9702BD/BW
RED, GREEN, AND BLUE ANALOG OUTPUTS (Cont.)		
Output Impedance	Ω (min/max)	10k (5k/15k)
Compliance	V	+3.0 to −1.2
Matching (Between any Two Gray Scale Outputs)	±% GS	1.0
RGB Outputs Time Skew	ns, max	2
RGB Outputs Crosstalk[6] (100MHz Bandwidth)	mV	20
Clock Noise on Outputs (100MHz Bandwidth)	mV	5
POWER REQUIREMENTS		
−5.2V ±0.25V[7]	mA (max)	250 (288)
+5V ±0.25V (TTL Only)	mA (max)	50 (60)
Power Supply Rejection Ratio	mV/mV	0.115
ECL Power Dissipation	W (max)	1.3 (1.5)
TTL Power Dissipation	W (max)	1.55 (1.8)
TEMPERATURE RANGE		
Operating (Case)	°C	−25 to +85
Storage	°C	−55 to +150
THERMAL RESISTANCE[8]		
Junction to Air, θ_{JA} (Free Air)	°C/W, max	40
Junction to Case, θ_{JC}	°C/W, max	12
PACKAGE OPTION[9]		
D-24A		AD9702BD
		AD9702BW

NOTES
[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50% points) is not included.
[2]Digital "0" at Reference White control input (Pin 1) sets registers; red, green, and blue outputs go to zero.
[3]In "normal operation," GS current or GS voltage outputs for red, green, and/or blue are established by RGB digital inputs.
[4]Digital "0" at Composite Blanking control input (Pin 16) resets registers; value shown is added to full-scale outputs at red, green, and blue outputs. Reference White and Composite Blanking should not be operated simultaneously.
[5]Green Sync control signal (@ Pin 23) affects only Green Output (@ Pin 21); value shown is added to Green Output established by Green digital inputs (and by Composite Blanking if digital "0" is simultaneously applied to Pin 16).
[6]Logic "0" digital inputs applied to D/A under test; full scale step function "toggling" applied to active D/A.
[7]Power supplies should have less than 10mV p-p ripple.
[8]Maximum junction temperature = 150°C.
[9]See Section 14 for package outline information.
Specifications subject to change without notice.

THEORY OF OPERATION

Refer to the Block Diagram of the AD9702 D/A Converter.

The digital inputs are applied through TTL/ECL converters to registers within the AD9702; the purpose of the registers is to eliminate time skew from the inputs and help reduce glitch impulse in the output signals. The switching of the inputs through the registers to the three internal D/A converters is controlled by the Strobe, Green Sync, Reference White, and Composite Blanking signals.

When operating with ECL-compatible logic, V_{EE} (−5.2V) is applied to Pin 17 and Pin 10 is connected to ground. Under these conditions, the TTL/ECL converters at the input are transparent to incoming signals and the signals are applied directly to the registers. Regardless of the logic levels of the digital inputs, the registers and control logic internal to the AD9702 are operated at ECL levels to help assure maximum switching speed and minimum glitch on the analog outputs.

For TTL logic, V_{CC} (+5V) is applied to Pin 10 and −5.2V is applied to Pin 17. The positive voltage is used only on the TTL/ECL converters, and adds to the flexibility of the AD9702 by allowing it to be compatible with both forms of logic generally encountered in graphics displays.

There is an alternate method of operating with TTL logic without a need for −5.2V supplies. In this arrangement, Pins 10, 19, and 24 are connected to +5V; and Pin 17 is grounded. In addition, digital inputs (RGB Bits 1 – 4) are connected to +5V through 2k resistors on each input line.

The disadvantage of this technique is that the output is referenced to the +5V supply instead of ground. When this happens, the dc component of the output may exceed the general requirements of RS-170 and RS-343. In addition, any noise which is on the power supply can be coupled directly onto the video signal.

One method of overcoming these potential problems is illustrated in Figure 1, Using AD9702 in TTL Mode.

In this arrangement, the strobe signal is attenuated and shifted positively by a resistor network to minimize feedthrough of the clock signal. The digital input signals do not require the same kind of attenuation because their larger TTL swings do not present any problems.

The pull-up resistors which are used on the inputs help assure proper digital "1" logic levels regardless of which TTL logic family is used.

The PNP level shifter shown at the analog output in Figure 1 eliminates the possible problems of TTL operation cited above.

Most of the noise which might be present on the +5V supply is cancelled by common mode rejection in this circuit; and level shifting helps insure the dc component of the output meets video standards.

Minor linearity degradation and temperature drift which might be introduced by the level shifter are not discernible on most video displays. The level shifter circuit is repeated three times for the Red, Green, and Blue analog outputs of the AD9702.

As shown in the block diagram and discussed in the Specifications section, a digital "0" level of the Reference White signal (at Pin 1) is used to set the registers within the converter. This action causes the three (RGB) analog outputs to go to zero output.

The Composite Blanking signal is applied to Pin 16; when a digital "0" level is used, it resets the registers and causes the three analog outputs to be −17.4mA or −653mV because of the amount added to the normal full-scale outputs.

The Green Sync signal at Pin 23 has an effect only on the Green Output of the AD9702 (at Pin 21). When this control and Composite Blanking are at a digital "0" level, the value of the Green analog output will be −25mA or −938mV.

When control inputs Reference White, Composite Blanking, and Green Sync are at digital "1" levels, the RGB analog outputs at Pins 22, 21, and 18 will be a function of their corresponding

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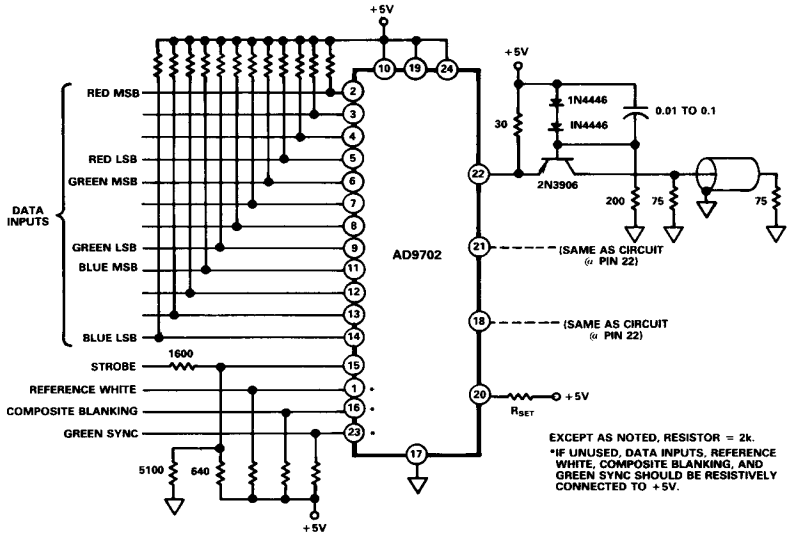

Figure 1. Using AD9702 in TTL Mode (Single Supply)

digital inputs. This is the "normal operation" referred to in the Specifications Table.

Resistor R_{SET} is connected between Pin 20, Current Set, and ground to establish the Gray Scale (GS) value of the RGB outputs. The value to be used is based on the desired full-scale GS output and the following equations:

$$I_{GS} = 5 \times I_{SET}$$

$$R_{SET} = \frac{4.4}{I_{SET}}$$

$$V_{OUT} = \frac{22 \times R_{LOAD}}{R_{SET}}$$

When using these equations, typical values of I_{SET} and V_{OUT} (Gray Scale output) will be within ±5%.

The idealized green analog output is illustrated in Figure 1.

The red and blue analog outputs are similar to the waveform shown in Figure 1, with the exception no sync portion is present on the Red and Blue outputs.

Sync control inputs are not required for Red and Blue outputs because of the RGB signals being synchronized within the AD9702. The majority of applications for the AD9702 in graphics displays use the green sync as the synchronizing signal for the monitor.

ORDERING INFORMATION

The standard AD9702 triple four-bit D/A converter is supplied in hermetic and non-hermetic units. Both versions operate over a case temperature range of −25°C to +85°C. The hermetically-sealed ceramic DIP configuration is model number AD9702BD; the non-hermetic unit is AD9702BW. For special applications or units for military applications, contact the factory for details.

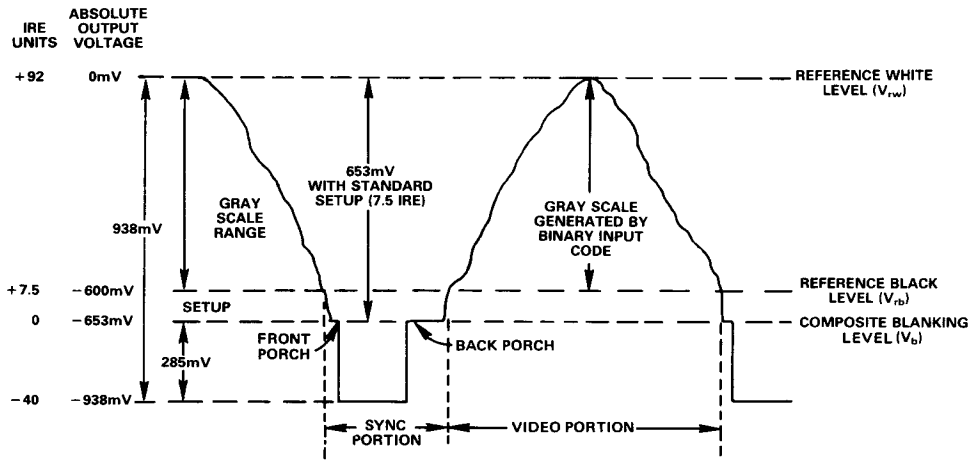

Figure 2. Idealized Green Output Waveform

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