

MOSFET – Power, Single, N-Channel

40 V, 3.3 mΩ, 102 A

NVMYS3D5N04C

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	40	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta,JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	A
		$T_C = 100^\circ\text{C}$	72	
		$T_C = 25^\circ\text{C}$	P_D	W
		$T_C = 100^\circ\text{C}$	34	
Continuous Drain Current $R_{\theta,JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	A
		$T_A = 100^\circ\text{C}$	17	
		$T_A = 25^\circ\text{C}$	P_D	W
		$T_A = 100^\circ\text{C}$	1.8	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10\ \mu\text{s}$	I_{DM}	554	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	°C
Source Current (Body Diode)		I_S	65	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 7.0\ \text{A}$)		E_{AS}	215	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	°C

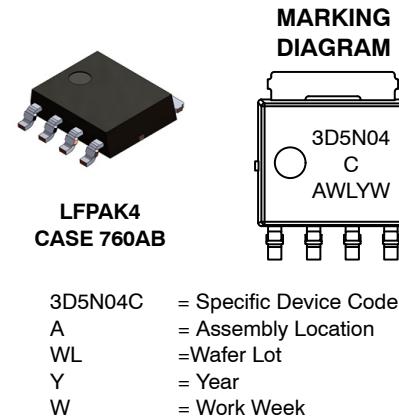
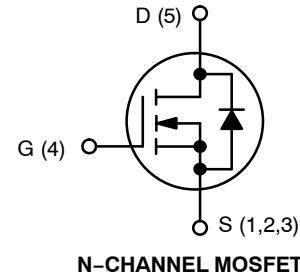
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta,JC}$	2.2	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta,JA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(\text{ON}) \text{ MAX}}$	$I_D \text{ MAX}$
40 V	3.3 mΩ @ 10 V	102 A



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMYS3D5N04C

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				22		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25 °C		10		μA
			T _J = 125 °C			100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 60 μA		2.5		3.5	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-7.8		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 50 A		2.7	3.3	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 50 A			93		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V		1600			pF
Output Capacitance	C _{OSS}			830			
Reverse Transfer Capacitance	C _{rss}			28			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 20 V; I _D = 50 A			23		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 20 V; I _D = 50 A			5.1		
Gate-to-Source Charge	Q _{GS}				9.0		
Gate-to-Drain Charge	Q _{GD}				3.5		
Plateau Voltage	V _{GP}				5.3		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 20 V, I _D = 50 A, R _G = 2.5 Ω		10			ns
Rise Time	t _r			47			
Turn-Off Delay Time	t _{d(OFF)}			19			
Fall Time	t _f			3.0			
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 50 A	T _J = 25 °C		0.9	1.2	V
			T _J = 125 °C		0.78		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A		37			ns
Charge Time	t _a			18			
Discharge Time	t _b			19			
Reverse Recovery Charge	Q _{RR}			23			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

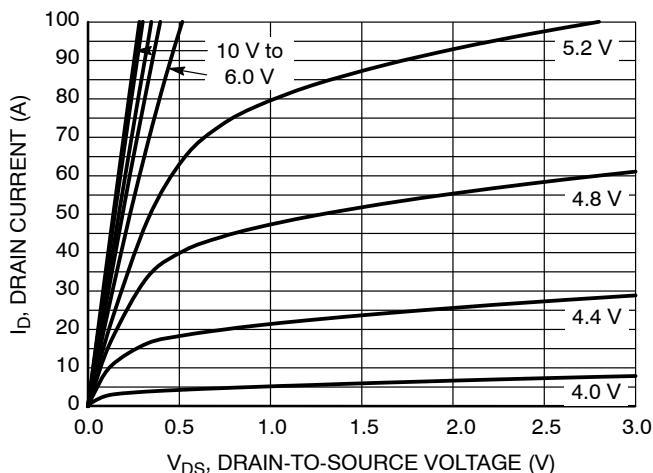


Figure 1. On-Region Characteristics

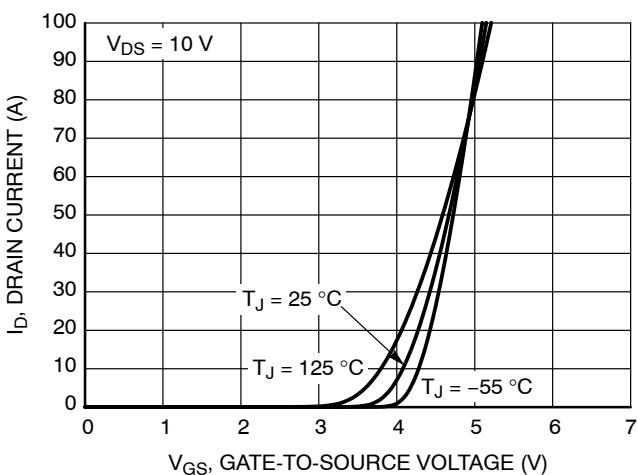


Figure 2. Transfer Characteristics

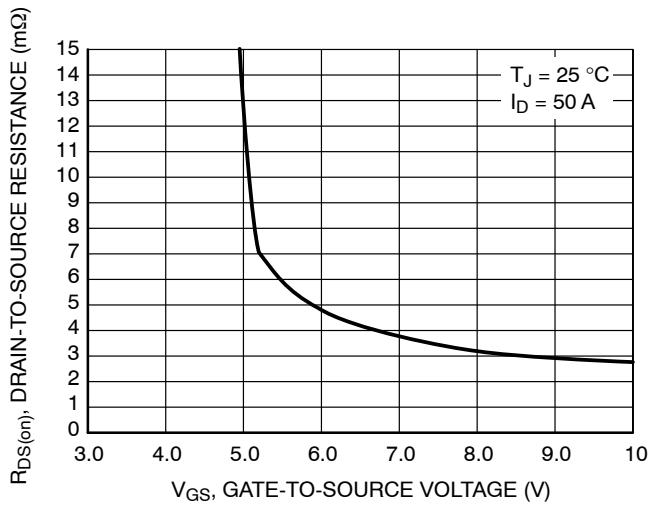


Figure 3. On-Resistance vs. Gate-to-Source Voltage

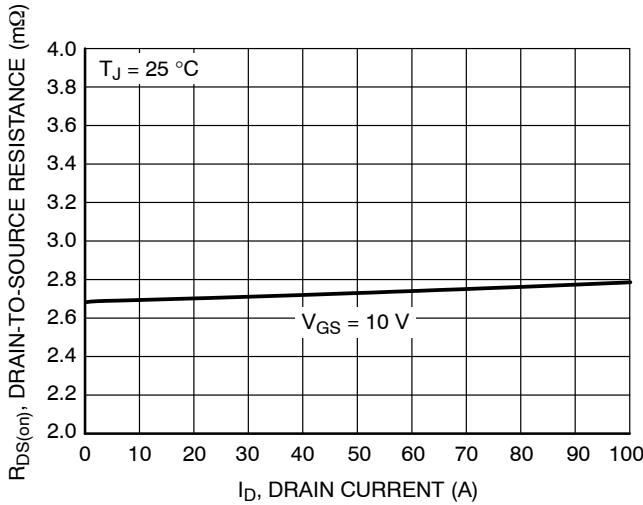


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

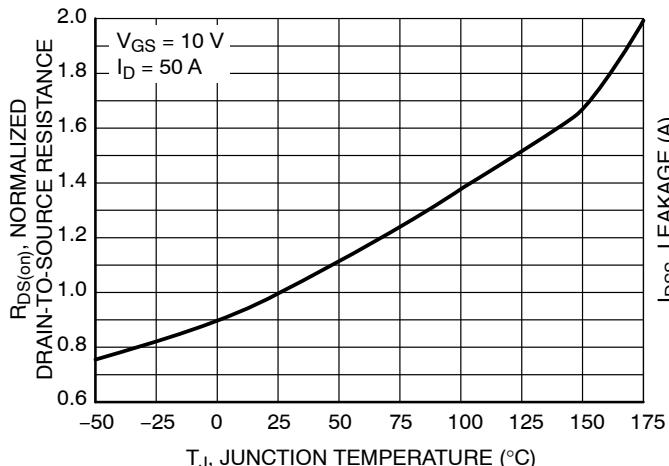


Figure 5. On-Resistance Variation with Temperature

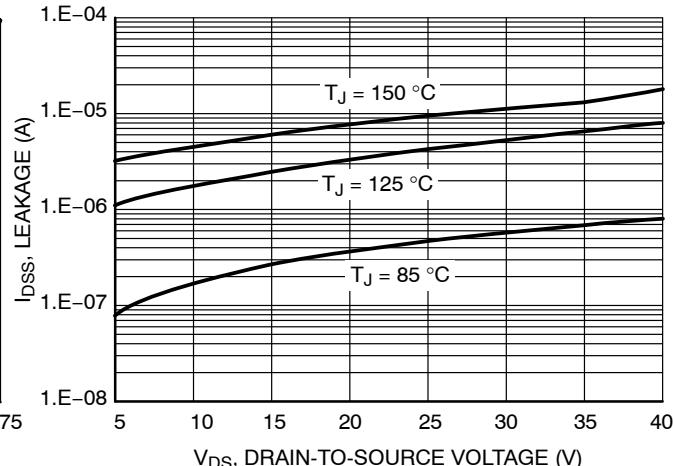


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

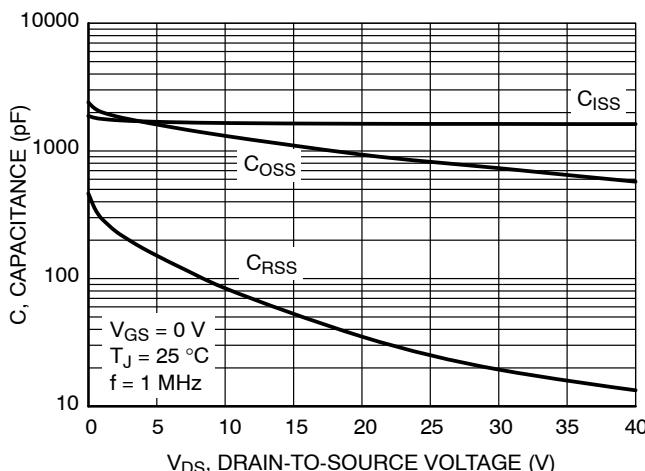


Figure 7. Capacitance Variation

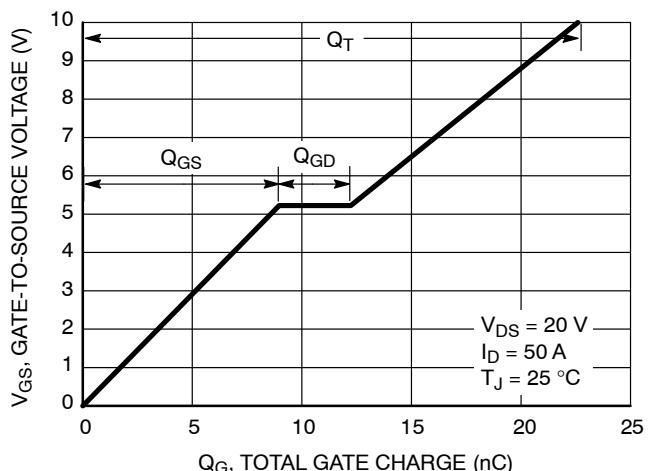


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

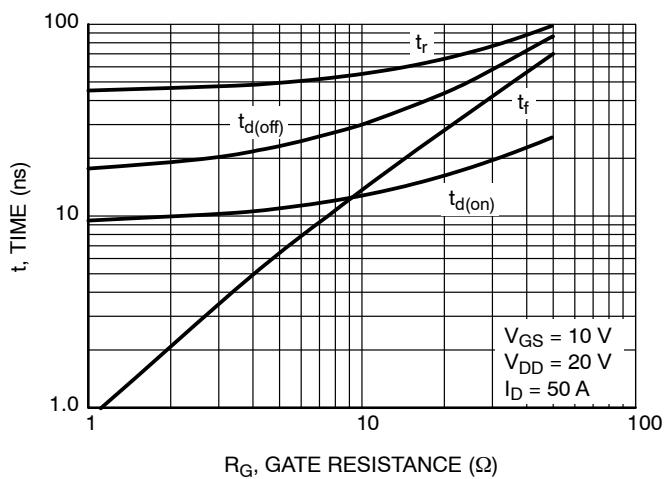


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

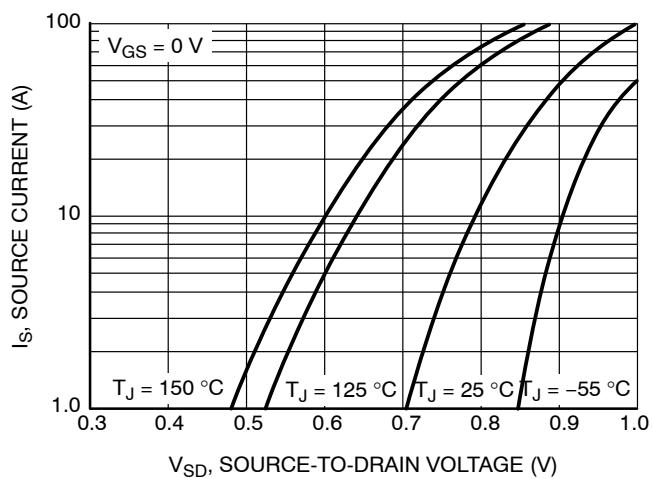


Figure 10. Diode Forward Voltage vs. Current

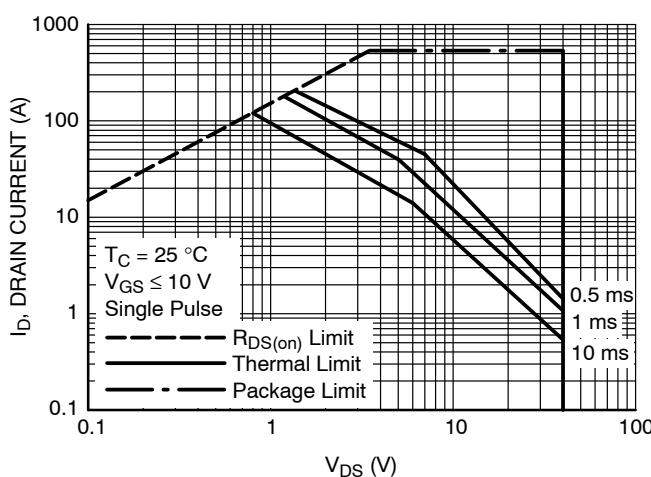


Figure 11. Safe Operating Area

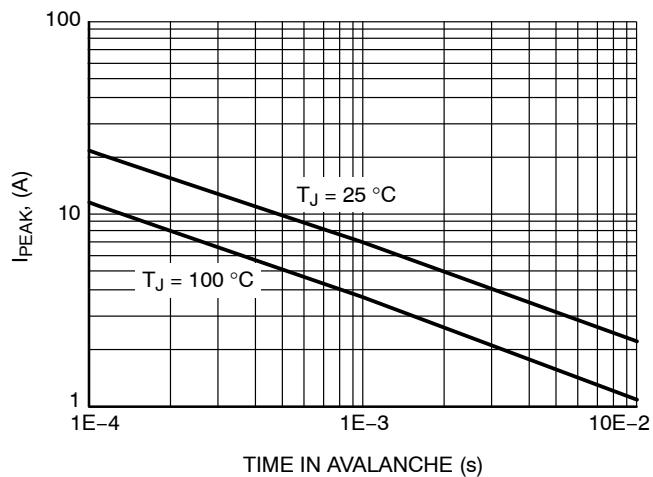


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

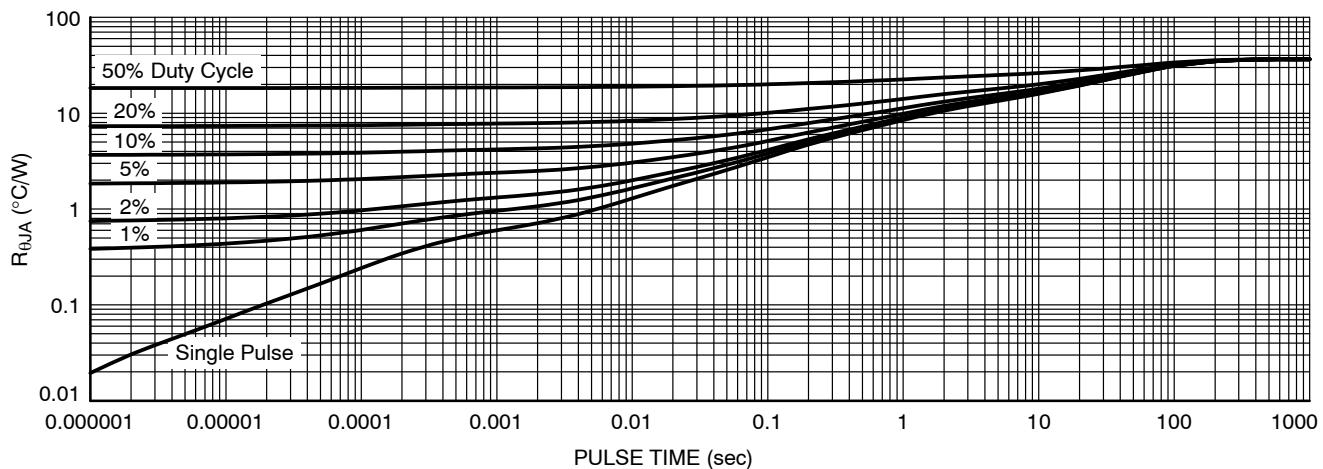


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMYS3D5N04CTWG	3D5N04C	LFPAK4 (Pb-Free)	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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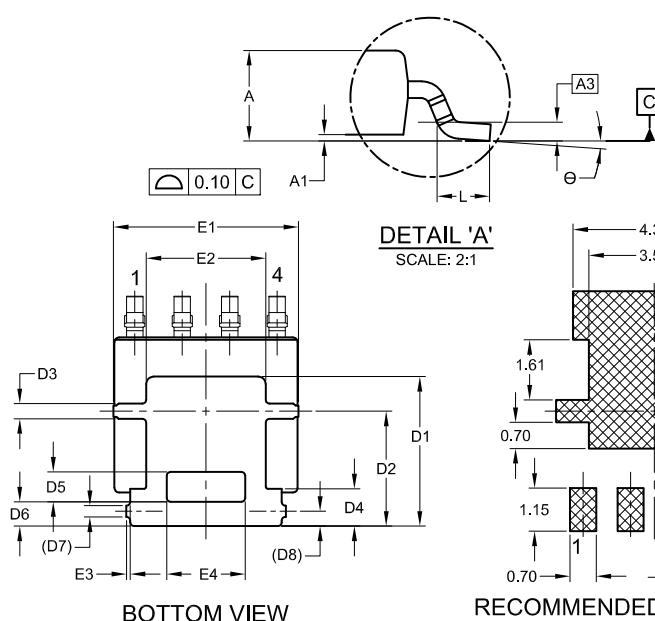
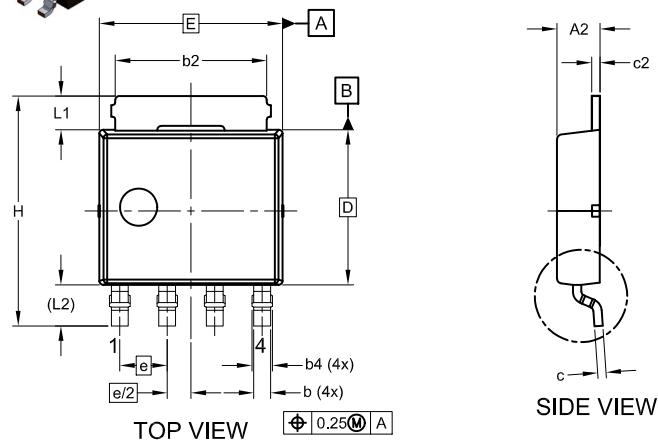
REVISION HISTORY

Revision	Description of Changes	Date
0	Initial production document version release.	12/11/2018
1	Document rebranded to onsemi format.	11/18/2025



LFPAK4 4.90x4.15x1.15MM, 1.27P
CASE 760AB
ISSUE D

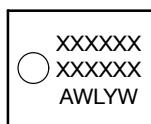
DATE 22 MAY 2024



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SODERRM/D.

**GENERIC
MARKING DIAGRAM***



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.15 BSC		
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
D5	0.70	0.80	0.90
D6	0.55	0.65	0.75
D7	0.31 REF		
D8	0.40 REF		
E	4.90 BSC		
E1	4.85	4.95	5.05
E2	3.10	3.20	3.30
E3	0.00	0.10	0.20
E4	2.00	2.10	2.20
e	1.27 BSC		
e/2	0.635 BSC		
e1	0.40 REF		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.80	0.90	1.00
L2	1.10 REF		
Theta	0°	4°	8°

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DESCRIPTION:	LFPAK4 4.90x4.15x1.15MM, 1.27P	PAGE 1 OF 1

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