Octal D-type flip-flop with reset; positive-edge trigger 74LV273

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.•**
- **Ideal buffer for MOS microprocessor or memory**
- **Common clock and master reset**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV273 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT273.

The 74LV273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n; $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 3.3 V	12 13	ns
f_{max}	maximum clock frequency		110	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV273N	20	DIL	plastic	DIL20/SOT146
74LV273D	20	SO	plastic	SO20/SOT163A
74LV273DB	20	SSOP	plastic	SSOP20/SOT339

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

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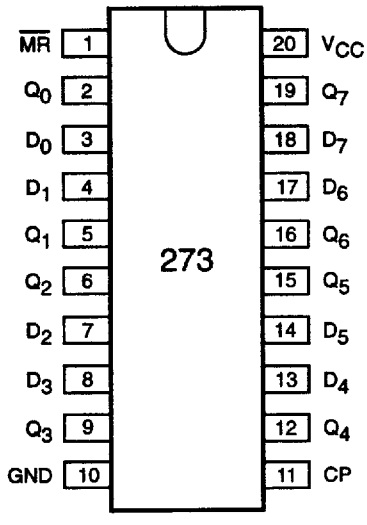

Fig.1 Pin configuration.

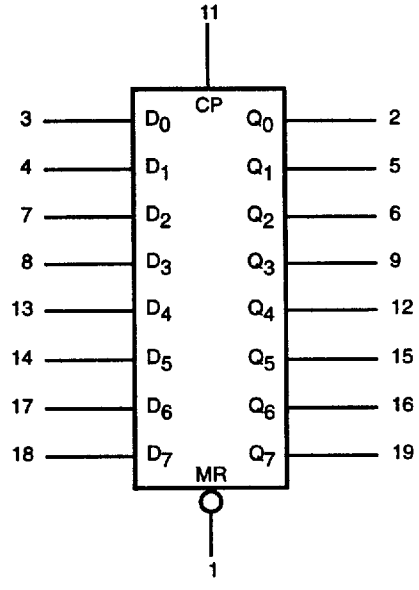

Fig.2 Logic symbol.

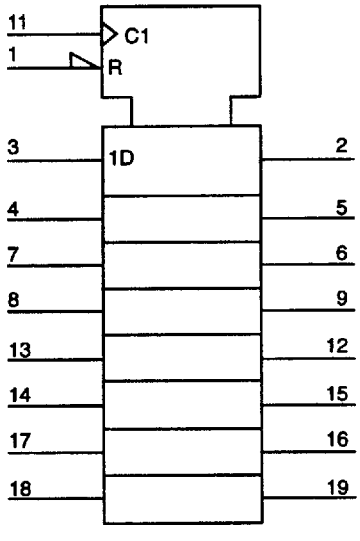

Fig3. IEC logic symbol.

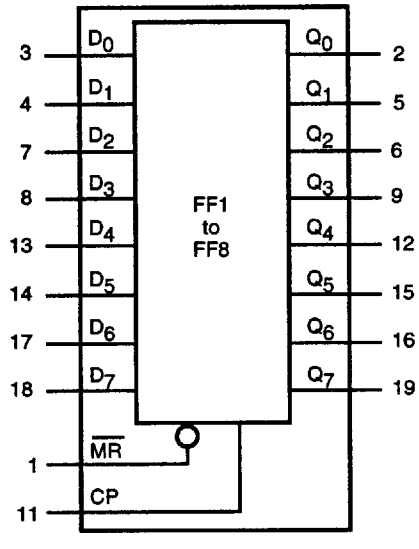

Fig.4 Functional diagram.

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FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_0 to Q_7
reset (clear)	L	X	X	L
load '1'	H	↑	h	H
load '0'	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
↑ = LOW-to-HIGH transition
X = don't care

DC CHARACTERISTICS FOR 74LV273

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV273

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		-40 to +85			-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– – – –	75 26 19 14*	– 49 36 29	– – – –	– 60 44 35	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.5
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	– – – –	80 27 20 15*	– 51 38 30	– – – –	– 61 45 36	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.6
t_W	clock pulse width HIGH or LOW	34 25 20	9 6 5*	– – –	41 30 24	– – –	ns	2.0 2.7 3.0 to 3.6	Fig.5
t_W	master reset pulse width LOW	34 25 20	10 8 6*	– – –	41 30 24	– – –	ns	2.0 2.7 3.0 to 3.6	Fig.6
t_{rem}	removal time $\overline{MR}$ to CP	– 5 5 5	–10 –4 –3 –2*	– – – –	– 5 5 5	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.6
t_{su}	set-up time D_n to CP	– 22 16 13	20 7 5 4*	– – – –	– 26 19 15	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.7
t_h	hold time D_n to CP	– 5 5 5	–10 –4 –3 –2*	– – – –	– 5 5 5	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.7
f_{max}	maximum clock pulse frequency	14 19 24	40 75 100*	– – –	12 16 20	– – –	ns	2.0 2.7 3.0 to 3.6	Fig. 5

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

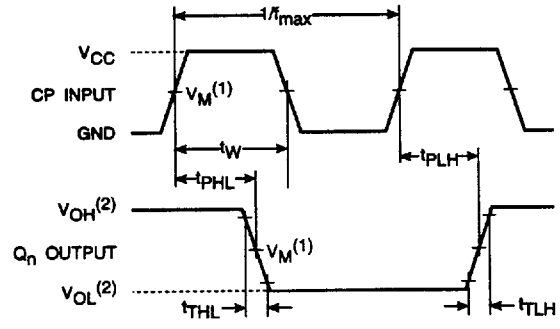

Fig.5 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

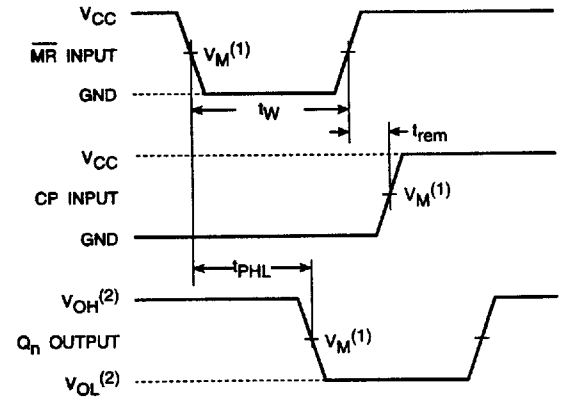

Fig.6 Waveforms showing master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

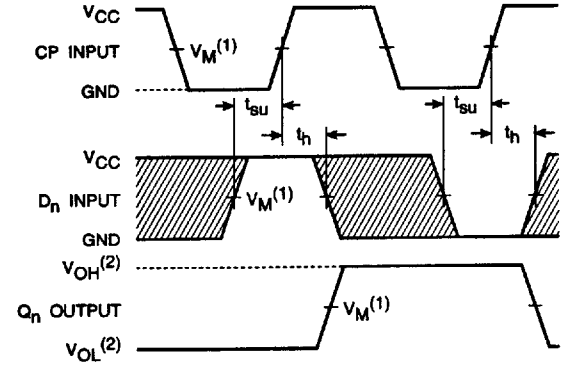

Fig.7 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig.7:
The shaded areas indicate when the input is permitted to change for predictable output performance.