

## 1. Features

- Full Trusted Computing Group (TCG) Trusted Platform Module (TPM) Version 1.2 Compatibility
- Compliant with TCG PC Client Specific TPM Interface Specification Version 1.2
- Single-chip Turnkey Solution
- Hardware Asymmetric Crypto Engine
- 2048-bit RSA® Sign in 200ms
- AVR® RISC Microprocessor
- Internal EEPROM Storage for RSA Keys
- 33MHz LPC (Low Pin Count) Bus for Easy PC Interface
- Secure Hardware and Firmware Design and Chip Layout
- True Random Number Generator (RNG) – FIPS 140-2 Compliant
- NV Storage space for 1280-bytes of user defined data
- 3.3V Supply Voltage
- 28-lead Thin TSSOP, Wide TSSOP or 40-lead QFN Packages
- Offered in both Commercial (0 to 70°C) and Industrial (-40 to +85°C) Temperature Ranges

## 2. Description

The Atmel® AT97SC3204 is a fully integrated security module designed to be integrated into personal computers and other embedded systems. It implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM).

The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

The chip communicates with the PC through the LPC interface. The TPM supports SIRQ (for interrupts) and CLKRUN to permit clock stopping for power savings in mobile computers.



## Trusted Platform Module

### Atmel AT97SC3204 LPC Interface

### Summary

- \* See the full data sheet for detailed design information



Table 1-1. Pin Configurations

| Pin Name        | Function                                     |
|-----------------|----------------------------------------------|
| V <sub>CC</sub> | 3.3V Supply Voltage                          |
| SB3V            | Standby 3.3V Supply Voltage                  |
| GND             | Ground                                       |
| LRESET#         | PCI Reset Input Active Low                   |
| LAD0            | LPC Command, Address, Data Line Input/Output |
| LAD1            | LPC Command, Address, Data Line Input/Output |
| LAD2            | LPC Command, Address, Data Line Input/Output |
| LAD3            | LPC Command, Address, Data Line Input/Output |
| LCLK            | 33MHz PCI Clock Input                        |
| LFRAME#         | LPC FRAME Input                              |
| CLKRUN#         | PCI Clock Run Input/Output                   |
| LPCPD#          | LPC Power Down Input                         |
| SERIQ           | Serialized Interrupt Request Input/Output    |
| GPIO6           | General Purpose Input/Output                 |
| TestI           | Test Input (disabled)                        |
| TestBI          | Test Input (disabled)                        |
| ATest           | Atmel Test Pin                               |
| NC              | No Connect                                   |
| NBO             | Not Bounded out                              |

Figure 2-1. Pinout Diagrams

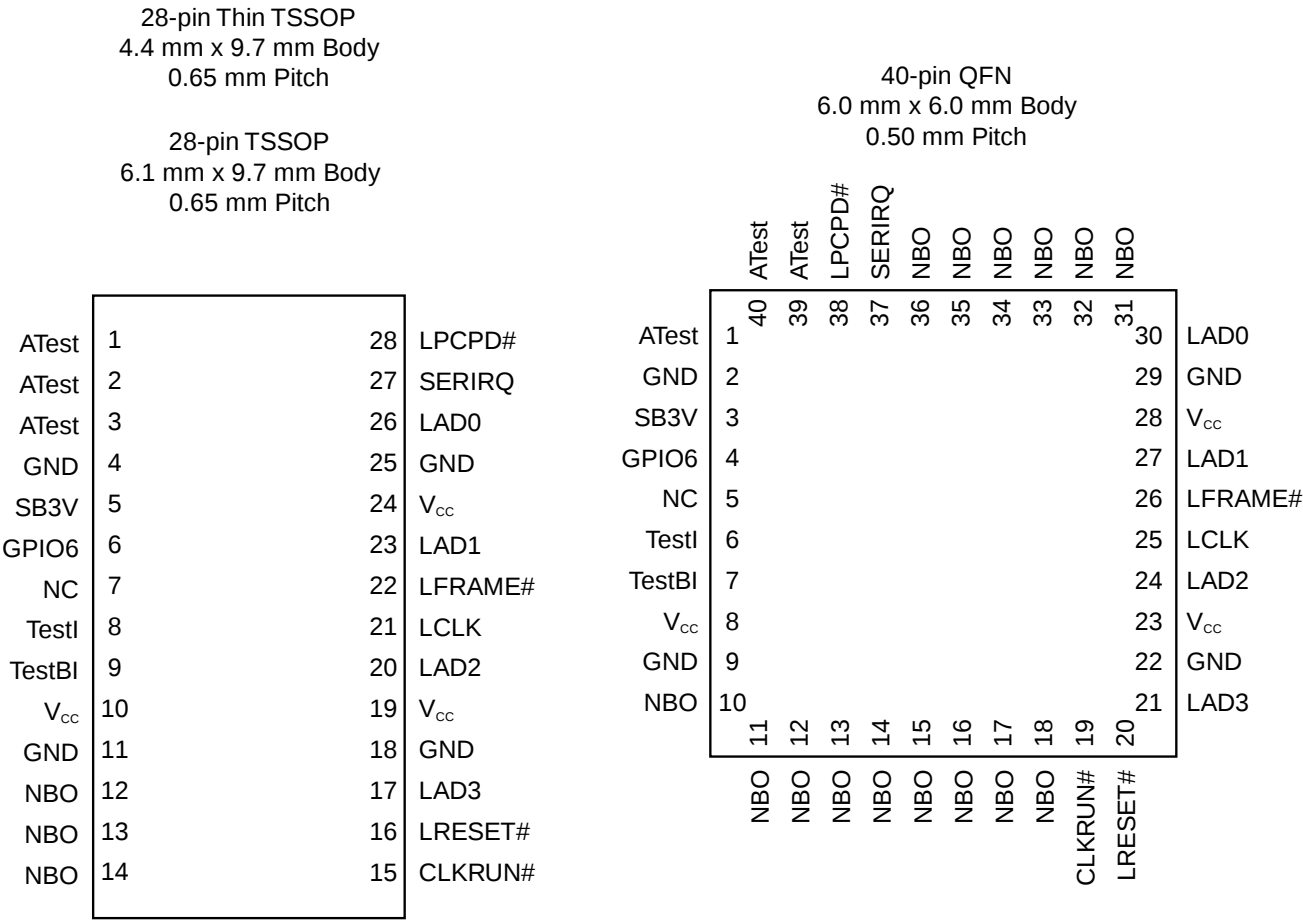
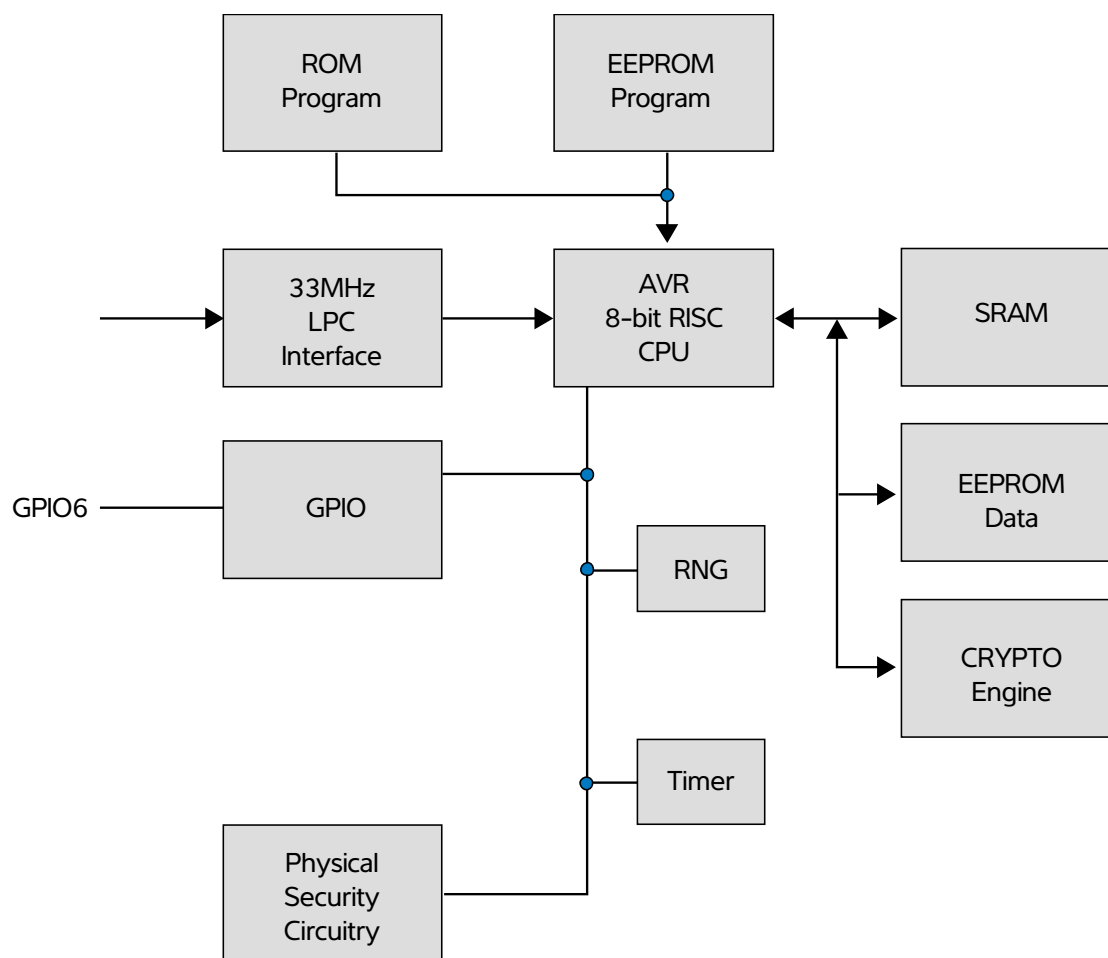


Figure 2-2. Atmel AT97SC3204 Block Diagram



The TPM includes a hardware random number generator, including a FIPS-approved Pseudo Random Number Generator that is used for key generation and TCG protocol functions. The RNG is also available to the system to generate random numbers that may be needed during normal operation.

The chip uses a dynamic internal memory management scheme to store multiple RSA keys. Other than the standard TCG commands (TPM\_FlushSpecific, TPM\_Loadkey2), no system intervention is required to manage this internal key cache.

The TPM is offered to OEM and ODM manufacturers as a turnkey solution, including the firmware integrated on the chip. In addition, Atmel provides the necessary device driver software for integration into certain operating systems, along with BIOS drivers. Atmel will also provide manufacturing support software for use by OEMs and ODMs during initialization and verification of the TPM during board assembly.

Full documentation for TCG primitives can be found in the TCG TPM Main Specification, Parts 1 to 3, on the TCG Web site located at <https://www.trustedcomputinggroup.org>. TPM features specific to PC Client platforms are specified in the "TCG PC Client Specific TPM Interface Specification, Version 1.2", also available on the TCG web site. Implementation guidance for 32-bit PC platforms is outlined in the "TCG PC Client Specific Implementation Specification for Conventional BIOS for TCG Version 1.2", also available on the TCG web site.

### 3. Ordering Information

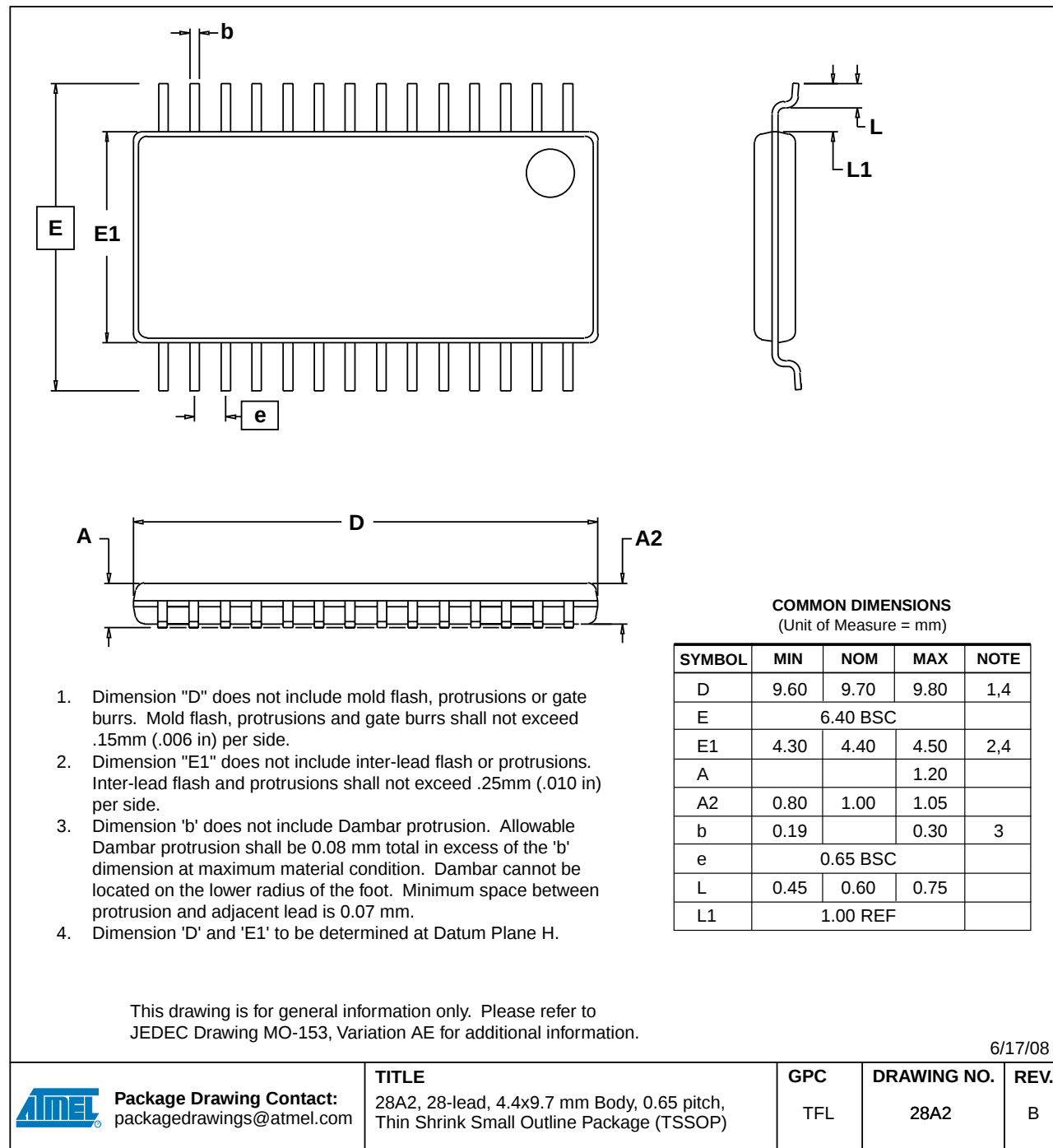
Table 1-2. Atmel AT24C256C Ordering Information

| Atmel Ordering Code       | Package                           |                 | Operating Range                                        |
|---------------------------|-----------------------------------|-----------------|--------------------------------------------------------|
| AT97SC3204 <sup>(1)</sup> | 28A2 (28-pin Thin TSSOP)          | Lead-free, RoHS | Commercial (0°C to 70°C)<br>Industrial (-40°C to 85°C) |
| AT97SC3204 <sup>(1)</sup> | 28A3 (28-pin TSSOP)               | Lead-free, RoHS | Commercial (0°C to 70°C)<br>Industrial (-40°C to 85°C) |
| AT97SC3204 <sup>(1)</sup> | 40ML1 (40-pin QFN) <sup>(2)</sup> | Lead-free, RoHS | Commercial (0°C to 70°C)<br>Industrial (-40°C to 85°C) |

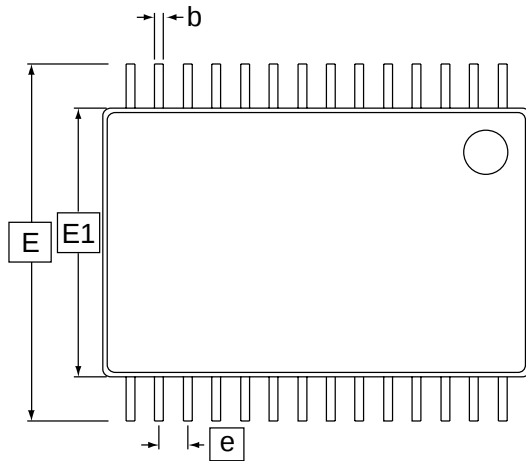
Notes: 1. Please see the Atmel AT97SC3204 datasheet addendum for the complete catalog number ordering code

## 4. Package Drawing

### 28A2 – Thin TSSOP



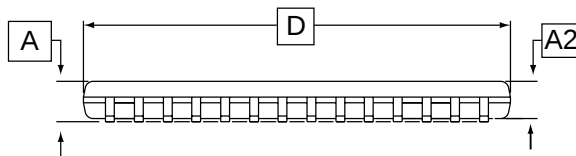
## 28A3 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS  
(Unit of Measure = mm)

| SYMBOL | MIN      | NOM  | MAX  | NOTE |
|--------|----------|------|------|------|
| D      | 9.60     | 9.70 | 9.80 | 2, 5 |
| E      | 8.10 BSC |      |      |      |
| E1     | 6.00     | 6.10 | 6.20 | 3, 5 |
| A      | –        | –    | 1.20 |      |
| A2     | 0.80     | 1.00 | 1.05 |      |
| b      | 0.19     | –    | 0.30 | 4    |
| e      | 0.65 BSC |      |      |      |
| L      | 0.45     | 0.60 | 0.75 |      |
| L1     | 1.00 REF |      |      |      |

- Note: 1. This drawing is for general information only. Please refer to JEDEC Drawing MO-153, Variation DB for additional information.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

1/8/02



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## TITLE

28A3, 28-lead, 6.1 x 9.7 mm Body, 0.65 pitch,  
Thin Shrink Small Outline Package (TSSOP)

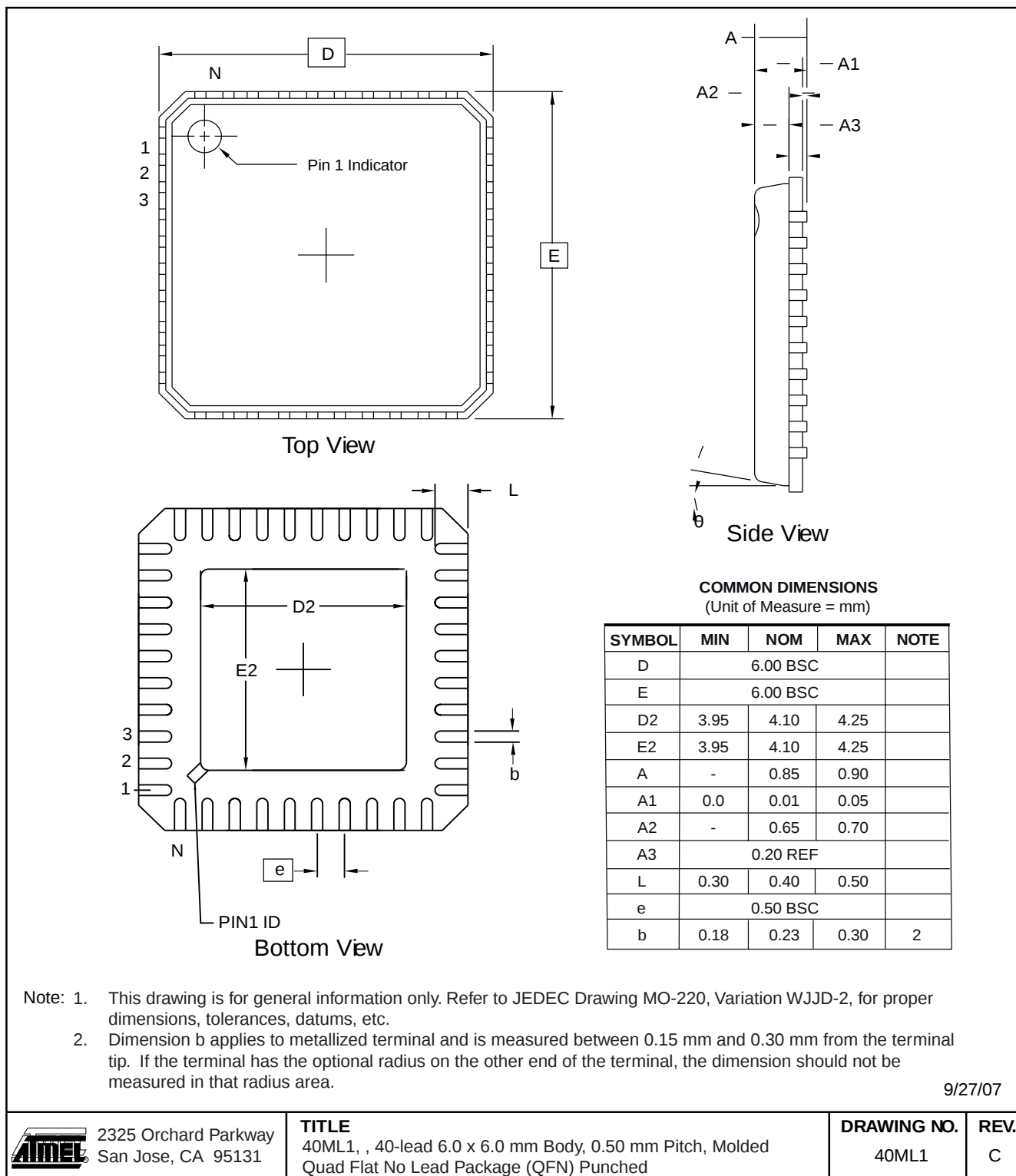
## DRAWING NO.

28A3

## REV.

A

# 40ML1 – QFN



## 5. Revision History

| Doc. Rev. | Date    | Comments                              |
|-----------|---------|---------------------------------------|
| 5294BS    | 10/2010 | Added Industrial Grade support detail |
| 5294AS    | 01/2008 | Initial document release              |



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