

# Regulating Pulse Width Modulators

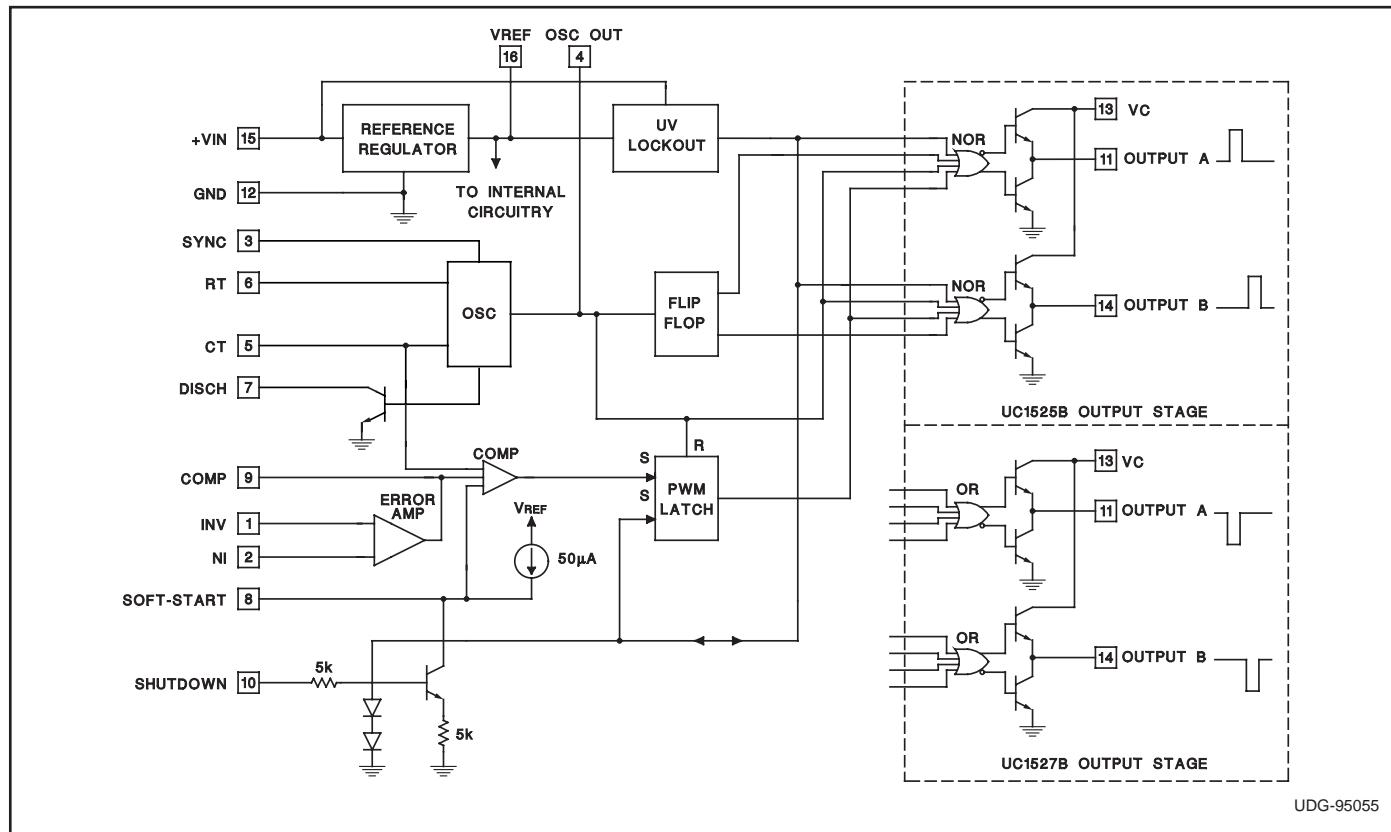
## FEATURES

- 8 to 35V Operation
- 5.1V Buried Zener Reference Trimmed to  $\pm 0.75\%$
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout with Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers
- Low Cross Conduction Output Stage
- Tighter Reference Specifications

## DESCRIPTION

The UC1525B/1527B series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V buried zener reference is trimmed to  $\pm 0.75\%$  and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the CT and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525B output stage features NOR logic, giving a LOW output for an OFF state. The UC1527B utilizes OR logic which results in a HIGH output level when OFF.

## BLOCK DIAGRAM



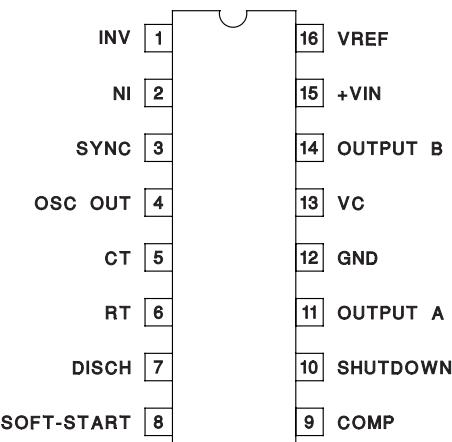
## ABSOLUTE MAXIMUM RATINGS

|  |                 |
|--|-----------------|
| Supply Voltage, (+VIN) .....                         | +40V            |
| Collector Supply Voltage (VC).....                   | +40V            |
| Logic Inputs .....                                   | -0.3V to +5.5V  |
| Analog Inputs.....                                   | -0.3V to VIN    |
| Output Current, Source or Sink .....                 | 500mA           |
| Reference Output Current .....                       | 50mA            |
| Oscillator Charging Current .....                    | 5mA             |
| Power Dissipation at $T_A = +25^\circ\text{C}$ ..... | 1000mW          |
| Power Dissipation at $T_C = +25^\circ\text{C}$ ..... | 2000mW          |
| Operating Junction Temperature .....                 | -55°C to +150°C |
| Storage Temperature Range .....                      | -65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.).....           | +300°C          |

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

## CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)  
J or N, DW Packages



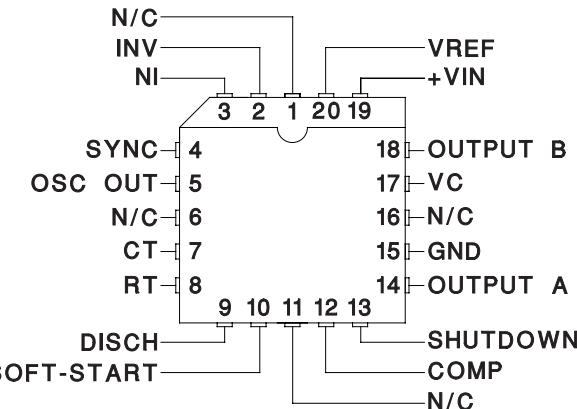
## RECOMMENDED OPERATING CONDITIONS

(Note 1)

|   |                  |
|---|------------------|
| Input Voltage (+VIN) .....                    | +8V to +35V      |
| Collector Supply Voltage (VC) .....           | +4.5V to +35V    |
| Sink/Source Load Current (steady state) ..... | 0 to 100mA       |
| Sink/Source Load Current (peak) .....         | 0 to 400mA       |
| Reference Load Current .....                  | 0 to 20mA        |
| Oscillator Frequency Range.....               | 100Hz to 400kHz  |
| Oscillator Timing Resistor .....              | 2kΩ to 150kΩ     |
| Oscillator Timing Capacitor .....             | 0.001μF to 0.1μF |
| Dead Time Resistor Range.....                 | 0Ω to 500Ω       |

Note 1: Range over which the device is functional and parameter limits are guaranteed.

LCC-20, PLCC-20 (Top View)  
L, Q Packages



**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1525B and UC1527B;  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2525B and UC2527B;  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3525B and UC3527B;  $+VIN = 20V$ ,  $T_A = T_J$ .

| PARAMETER                      | TEST CONDITIONS   | UC1525B/UC2525B<br>UC1527B/UC2527B |      |       | UC3525B<br>UC3527B |      |       | UNITS |
|--------------------------------|---|------------------------------------|------|-------|--------------------|------|-------|-------|
|                                |   | MIN                                | TYP  | MAX   | MIN                | TYP  | MAX   |       |
| <b>Reference Section</b>       |   |                                    |      |       |                    |      |       |       |
| Output Voltage                 | $T_J = 25^\circ\text{C}$  | 5.062                              | 5.10 | 5.138 | 5.036              | 5.10 | 5.164 | V     |
| Line Regulation                | $VIN = 8V$ to $35V$   |                                    | 5    | 10    |                    | 5    | 10    | mV    |
| Load Regulation                | $I_L = 0\text{mA}$ to $20\text{mA}$                               |                                    | 7    | 15    |                    | 7    | 15    | mV    |
| Temperature Stability (Note 2) | Over Operating Range  |                                    | 10   | 50    |                    | 10   | 50    | mV    |
| Total Output Variation         | Line, Load, and Temperature                                       | 5.036                              |      | 5.164 | 5.024              |      | 5.176 | V     |
| Short Circuit Current          | $VREF = 0$ , $T_J = 25^\circ\text{C}$                             |                                    | 80   | 100   |                    | 80   | 100   | mA    |
| Output Noise Voltage (Note 2)  | $10\text{Hz} \leq f \leq 10\text{kHz}$ , $T_J = 25^\circ\text{C}$ |                                    | 40   | 200   |                    | 40   | 200   | μVrms |
| Long Term Stability (Note 2)   | $T_J = 125^\circ\text{C}$ , 1000 Hrs.                             |                                    | 3    | 10    |                    | 3    | 10    | mV    |

UC1525B UC1527B

UC2525B UC2527B

UC3525B UC3527B

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| PARAMETER   | TEST CONDITIONS  | UC1525B/UC2525B<br>UC1527B/UC2527B |           |         | UC3525B<br>UC3527B |         |         | UNITS         |
|---|--|------------------------------------|-----------|---------|--------------------|---------|---------|---------------|
|   |  | MIN                                | TYP       | MAX     | MIN                | TYP     | MAX     |               |
| <b>Oscillator Section (Note 3)</b>                        |  |                                    |           |         |                    |         |         |               |
| Initial Accuracy (Notes 2 & 3)                            | $T_J = 25^\circ\text{C}$   |                                    | $\pm 2$   | $\pm 6$ |                    | $\pm 2$ | $\pm 6$ | %             |
| Voltage Stability (Notes 2 & 3)                           | $\text{VIN} = 8\text{V}$ to $35\text{V}$   |                                    | $\pm 0.3$ | $\pm 1$ |                    | $\pm 1$ | $\pm 2$ | %             |
| Temperature Stability (Note 2)                            | Over Operating Range   |                                    | $\pm 3$   | $\pm 6$ |                    | $\pm 3$ | $\pm 6$ | %             |
| Minimum Frequency   | $\text{RT} = 200\text{k}\Omega$ , $\text{CT} = 0.1\mu\text{F}$                       |                                    |           | 120     |                    |         | 120     | Hz            |
| Maximum Frequency   | $\text{RT} = 2\text{k}\Omega$ , $\text{CT} = 470\text{pF}$                           | 400                                |           |         | 400                |         |         | kHz           |
| Current Mirror  | $I_{\text{RT}} = 2\text{mA}$   | 1.7                                | 2.0       | 2.2     | 1.7                | 2.0     | 2.2     | mA            |
| Clock Amplitude (Notes 2 & 3)                             |  | 3.0                                | 3.5       |         | 3.0                | 3.5     |         | V             |
| Clock Width (Notes 2 & 3)                                 | $T_J = 25^\circ\text{C}$   | 0.3                                | 0.5       | 1.0     | 0.3                | 0.5     | 1.0     | $\mu\text{s}$ |
| Sync Threshold  |  | 1.2                                | 2.0       | 2.8     | 1.2                | 2.0     | 2.8     | V             |
| Sync Input Current  | Sync Voltage = $3.5\text{V}$   |                                    | 1.0       | 2.5     |                    | 1.0     | 2.5     | mA            |
| <b>Error Amplifier Section (V<sub>CM</sub> = 5.1V)</b>    |  |                                    |           |         |                    |         |         |               |
| Input Offset Voltage                                      |  |                                    | 0.5       | 5       |                    | 2       | 10      | mV            |
| Input Bias Current  |  |                                    | 1         | 10      |                    | 1       | 10      | $\mu\text{A}$ |
| Input Offset Current                                      |  |                                    |           | 1       |                    |         | 1       | $\mu\text{A}$ |
| DC Open Loop Gain   | $\text{RL} \geq 10 \text{ Meg}\Omega$  | 60                                 | 75        |         | 60                 | 75      |         | dB            |
| Gain-Bandwidth Product (Note 2)                           | $\text{A}_V = 0\text{dB}$ , $T_J = 25^\circ\text{C}$                                 | 1                                  | 2         |         | 1                  | 2       |         | MHz           |
| Output Low Level  |  |                                    | 0.2       | 0.5     |                    | 0.2     | 0.5     | V             |
| Output High Level   |  | 3.8                                | 5.6       |         | 3.8                | 5.6     |         | V             |
| Common Mode Rejection                                     | $\text{V}_{\text{CM}} = 1.5\text{V}$ to $5.2\text{V}$                                | 60                                 | 75        |         | 60                 | 75      |         | dB            |
| Supply Voltage Rejection                                  | $\text{VIN} = 8\text{V}$ to $35\text{V}$   | 50                                 | 60        |         | 50                 | 60      |         | dB            |
| <b>PWM Comparator</b>                                     |  |                                    |           |         |                    |         |         |               |
| Minimum Duty Cycle  |  |                                    |           | 0       |                    |         | 0       | %             |
| Maximum Duty Cycle (Note 3)                               |  | 45                                 | 49        |         | 45                 | 49      |         | %             |
| Input Threshold (Note 3)                                  | Zero Duty Cycle  | 0.7                                | 0.9       |         | 0.7                | 0.9     |         | V             |
| Input Threshold (Note 3)                                  | Maximum Duty Cycle   |                                    | 3.3       | 3.6     |                    | 3.3     | 3.6     | V             |
| Input Bias Current (Note 2)                               |  |                                    | 0.05      | 1.0     |                    | 0.05    | 1.0     | $\mu\text{A}$ |
| <b>Shutdown Section</b>                                   |  |                                    |           |         |                    |         |         |               |
| Soft Start Current  | $\text{V}_{\text{SHUTDOWN}} = 0\text{V}$ , $\text{V}_{\text{SOFTSTART}} = 0\text{V}$ | 25                                 | 50        | 80      | 25                 | 50      | 80      | $\mu\text{A}$ |
| Soft Start Low Level                                      | $\text{V}_{\text{SHUTDOWN}} = 2.5\text{V}$   |                                    | 0.4       | 0.7     |                    | 0.4     | 0.7     | V             |
| Shutdown Threshold  | To outputs, $\text{V}_{\text{SOFTSTART}} = 5.1\text{V}$ , $T_J = 25^\circ\text{C}$   | 0.6                                | 0.8       | 1.0     | 0.6                | 0.8     | 1.0     | V             |
| Shutdown Input Current                                    | $\text{V}_{\text{SHUTDOWN}} = 2.5\text{V}$   |                                    | 0.4       | 1.0     |                    | 0.4     | 1.0     | mA            |
| Shutdown Delay (Note 2)                                   | $\text{V}_{\text{SHUTDOWN}} = 2.5\text{V}$ , $T_J = 25^\circ\text{C}$                |                                    | 0.2       | 0.5     |                    | 0.2     | 0.5     | $\mu\text{s}$ |
| <b>Output Drivers (Each Output) (V<sub>C</sub> = 20V)</b> |  |                                    |           |         |                    |         |         |               |
| Output Low Level  | $I_{\text{SINK}} = 20\text{mA}$  |                                    | 0.2       | 0.4     |                    | 0.2     | 0.4     | V             |
|   | $I_{\text{SINK}} = 100\text{mA}$   |                                    | 1.0       | 2.0     |                    | 1.0     | 2.0     | V             |
| Output High Level   | $I_{\text{SOURCE}} = 20\text{mA}$  | 18                                 | 19        |         | 18                 | 19      |         | V             |
|   | $I_{\text{SOURCE}} = 100\text{mA}$   | 17                                 | 18        |         | 17                 | 18      |         | V             |
| Undervoltage Lockout                                      | $\text{V}_{\text{COMP}}$ and $\text{V}_{\text{SOFTSTART}} = \text{High}$             | 6                                  | 7         | 8       | 6                  | 7       | 8       | V             |
| Collector Leakage   | $\text{VC} = 35\text{V}$   |                                    |           | 200     |                    |         | 200     | $\mu\text{A}$ |

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| PARAMETER   | TEST CONDITIONS                               | UC1525B/UC2525B<br>UC1527B/UC2527B |     |     | UC3525B<br>UC3527B |     |     | UNITS |
|---|---|------------------------------------|-----|-----|--------------------|-----|-----|-------|
|   |   | MIN                                | TYP | MAX | MIN                | TYP | MAX |       |
| <b>Output Drivers (Each Output) (<math>V_C = 20\text{V}</math>) (cont.)</b> |   |                                    |     |     |                    |     |     |       |
| Rise Time (Note 2)  | $C_L = 1\text{nF}$ , $T_J = 25^\circ\text{C}$ |                                    | 100 | 600 |                    | 100 | 600 | ns    |
| Fall Time (Note 2)  | $C_L = 1\text{nF}$ , $T_J = 25^\circ\text{C}$ |                                    | 50  | 300 |                    | 50  | 300 | ns    |
| Cross conduction charge   | Per cycle, $T_J = 25^\circ\text{C}$           |                                    | 30  |     |                    | 30  |     | nc    |
| <b>Total Standby Current</b>  |   |                                    |     |     |                    |     |     |       |
| Supply Current  | $V_{IN} = 35\text{V}$                         |                                    | 14  | 20  |                    | 14  | 20  | mA    |

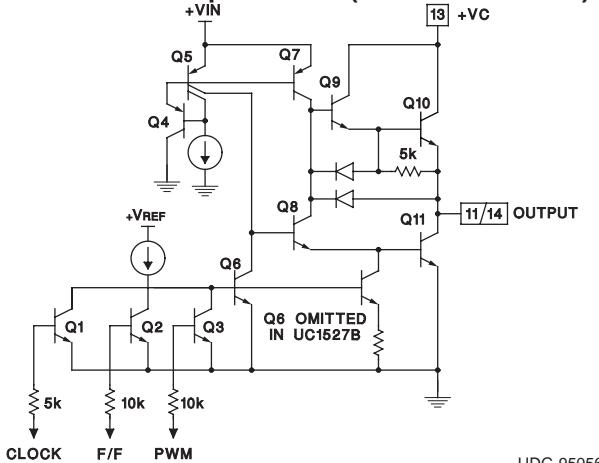
Note 2: Ensured by design. Not 100% tested in production.

Note 3: Tested at  $f_{osc} = 40\text{kHz}$  ( $R_T = 3.6\text{K}\Omega$ ,  $C_T = 0.01\mu\text{F}$ ,  $R_D = 0\Omega$ ). Approximate oscillator frequency is defined by:

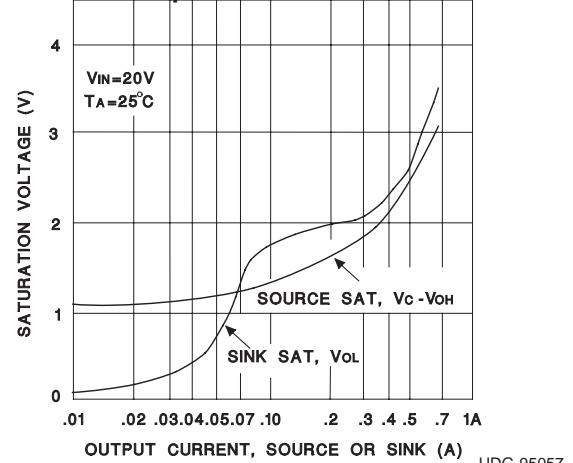
$$f = \frac{1}{C_T \cdot (0.7 \cdot R_T + 3R_D)}$$

## PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

### UC1525B Output Circuit (1/2 Circuit Shown)



### UC1525B Output Saturation Characteristics



+V<sub>SUPPLY</sub> ————— Q1 ————— TO OUTPUT FILTER

R1 R2

13 VC

OUTPUT A 11

UC1525B

OUTPUT B 14

GND 12

RETURN —————

UDG-95058

For single-ended supplies, the driver outputs are grounded. The VC terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

V<sub>SUPPLY</sub> ————— R1

13 VC

OUTPUT A 11

UC1525B

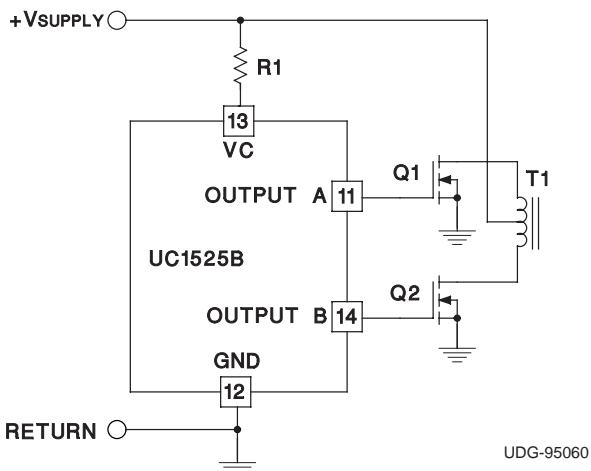
OUTPUT B 14

GND 12

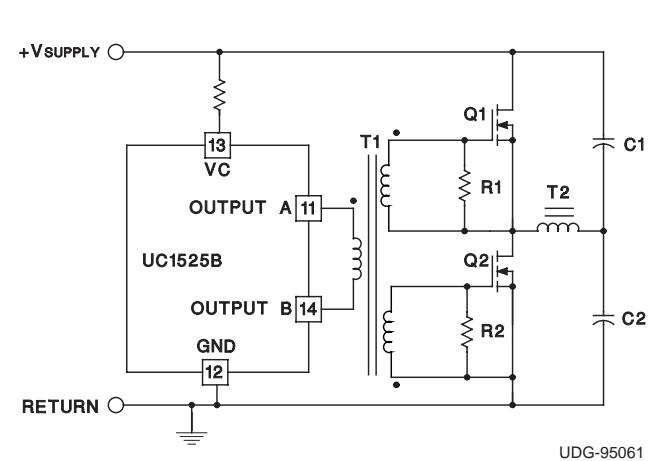
RETURN —————

UDG-95059

In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C<sub>1</sub> and C<sub>2</sub>.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven directly by the UC1525B. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

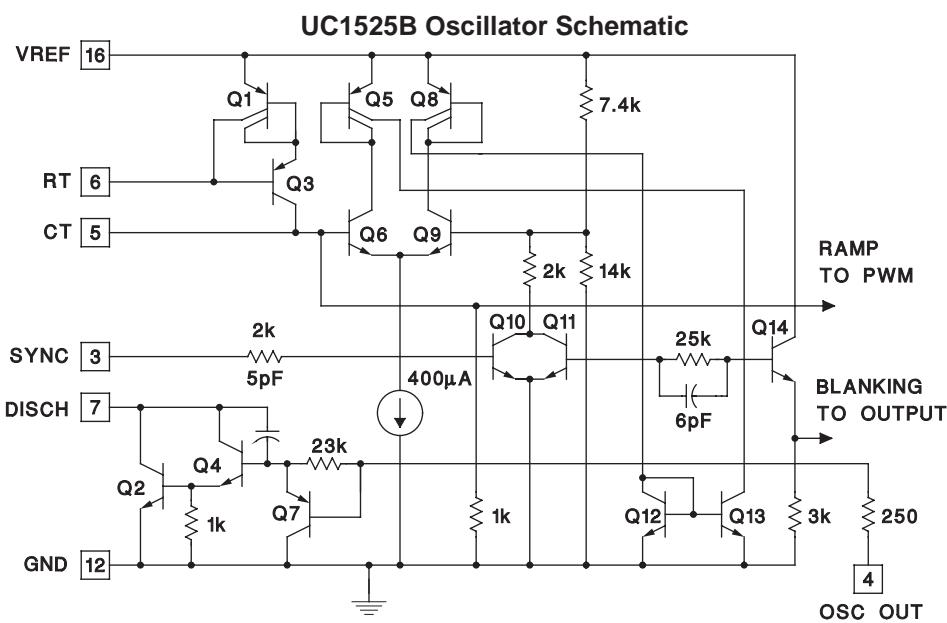
## PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

### Shutdown Options (See Block Diagram)

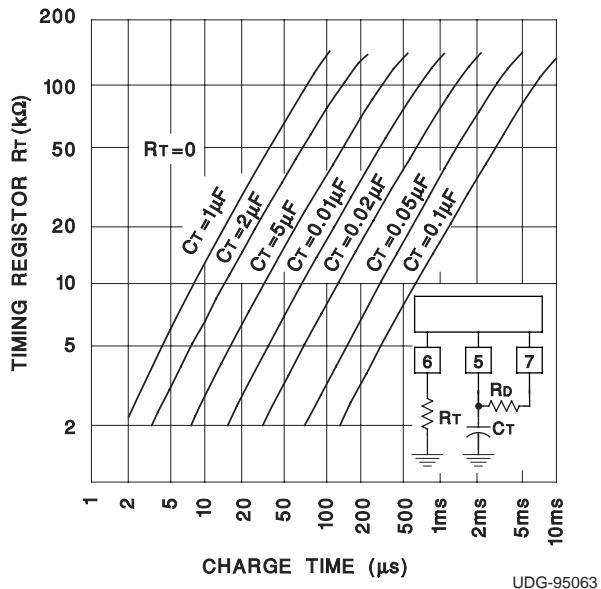
Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of  $100\mu\text{A}$  to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by ap-

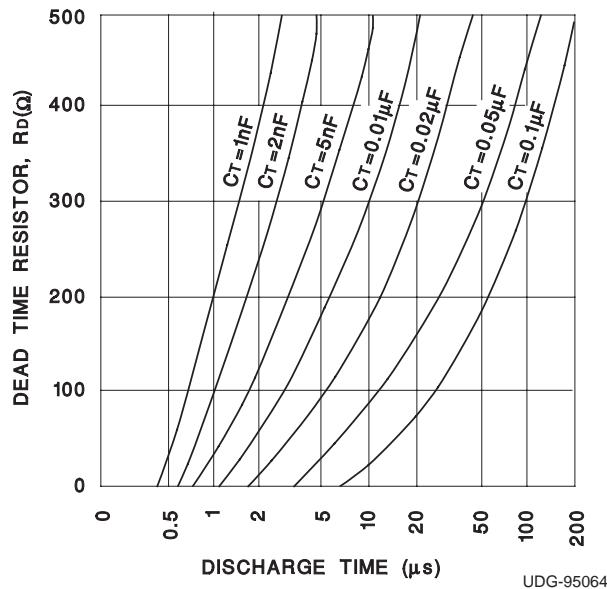
plying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.



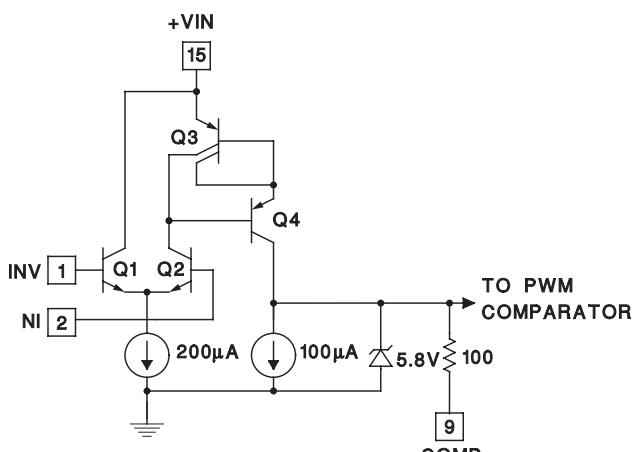
Oscillator Charge Time vs.  $R_T$  and  $C_T$



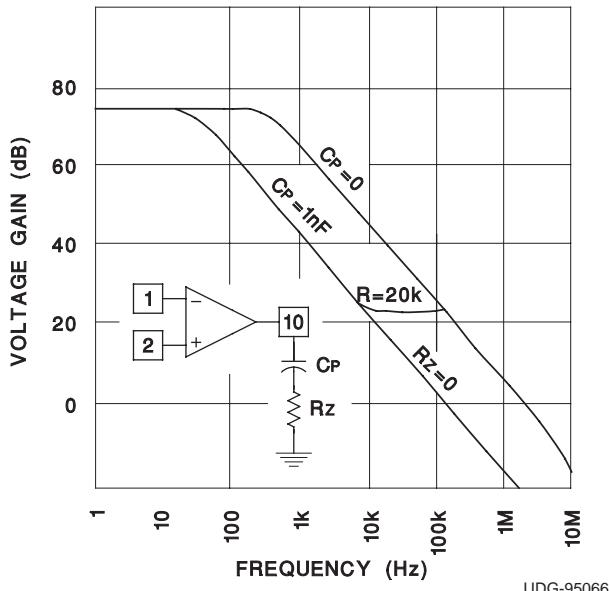
Oscillator Discharge Time vs.  $R_D$  and  $C_T$



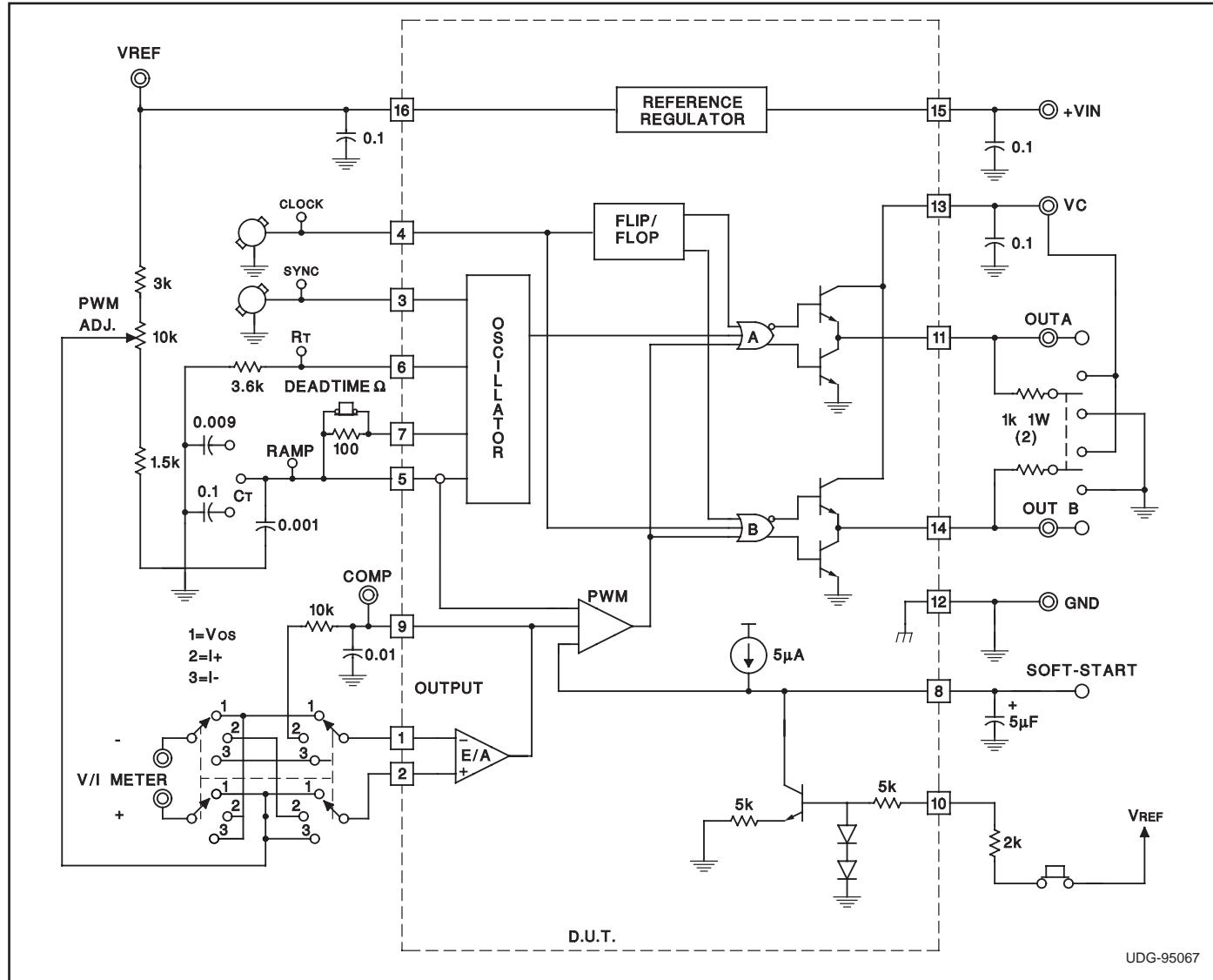
UC1525B Error Amplifier



Error Amplifier Open-Loop Frequency Response



LAB TEST FIXTURE



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