TEXAS INSTRUMENTS

TAS5066-5112F6EVM

PurePath Digital ™ Evaluation Module for the TAS5066PAG Six-Channel Digital Audio PWM Processor and TAS5112ADFD Stereo Digital Amplifier Power Output Stage

User's Guide

April 2004

Digital Audio and Video Products

SLEU051

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Preface

Read This First

About This Manual

This manual describes the operation of the TAS5066-5112F6EVM evaluation module from Texas Instruments.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 — Overview
- ❏ Chapter 2 — System Interfaces
- ❏ Chapter 3 — Protection

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This document may contain cautions and warnings.

This is an example of a caution statement.

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Related Documentation from Texas Instruments

The following table contains a list of data manuals that have detailed descriptions of the integrated circuits used in the design of the TAS5066−5112F6EVM. The data manuals can be obtained at the URL http://www.ti.com.

Part Number	Literature Number
TAS5066PAG	SLES089
TAS5112ADFD	SLES094
TLV272	SLOS351C
SN74LVC2G08	SCES198I
SN74LVC1G126	SCES224J
SN74LVC2G126	SCES205G
LMV331I	SLCS136K
LM317M	SLVS297I
TPS76433	SLVS180B
TPS3801K33	SLVS219B

Additional Documentation

- ❑ EVM Application Report (SLEA031)
- ❑ PC Configuration Tool for TAS50XX (DAS TCT 50xx – version 3.1 or later)
- ❑ General Application Notes

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Contents

1 Overview 1-1
1.1 TAS5066-5112F6EVM Features 1-2
1.2 PCB Key Map 1-3

2 System Interfaces 2-1
2.1 PSU Interface (J901) 2-2
2.2 PSU Control Interface (J902) 2-4
2.3 Loudspeaker Connectors (J220, J240, J320, J340, J420, and J440) 2-5
2.4 Subwoofer Line Out Connector (J500) 2-6
2.5 Control Interface (J130) 2-7
2.6 Digital Audio Interface (J131) 2-8
2.7 PWM Timing, Interchannel Delay Registers 2-9

3 Protection 3-1
3.1 Short-Circuit Protection and Fault-Reporting Circuitry 3-2
3.2 Device Fault Reporting 3-3

Figures

1−1 Complete PurePath Digital™ System 1-2
1−2 Physical Structure for the TAS5066-5112F6EVM 1-3
2−1 Recommended Power-Up Sequence 2-2
2−2 J901 Pin Numbers (PCB Connector Top View) 2-3
2−3 J902 Pin Numbers (PCB Connector Top View) 2-4
2−4 J220, J240, J320, J340, J420, and J440 Pin Numbers (PCB Connector Top View) 2-5
2−5 J500 Pin Numbers (PCB Connector Top View) 2-6

Tables

2−1 Recommended Power Supplies 2-2
2−2 J901 Pin Description 2-3
2−3 J902 Pin Description 2-4
2−4 Recommended Source/Speaker Allocation 2-5
2−5 J220, J240, J320, J340, J420, and J440 Pin Descriptions 2-5
2−6 J500 Pin Description 2-6
2−7 J130 Pin Description 2-7
2−8 J131 Pin Description 2-8
2−9 Clock Rates 2-8
2−10 Recommended Interchannel Delay Register Values (based on EVM designs) 2-9
3−1 Channel Allocation 3-2
3−2 TAS5112A Error Signal Decoding 3-3

Chapter 1

Overview

The TAS5066-5112F6EVM PurePath Digital™ customer evaluation module demonstrates two integrated circuits: TAS5066 and TAS5112ADFD.

The TAS5066 is a high performance 24-bit, 6-channel, digital pulse width modulator (PWM) based on Equibit™ technology. The TAS5066 has a wide variety of serial input (I^2S) options including right-justified, left-justified, and DSP data formats. It accepts I^2S data with sample rates up to 192 kHz.

The TAS5112A is a high-performance, stereo digital amplifier power stage designed to drive a 6-Ω loudspeaker up to 50 W. It contains integrated gate-drivers, 8 matched and electrically isolated, enhancement-mode, N-channel power DMOS transistors, and protection/fault-reporting circuitry.

The TAS5066-5112F6EVM, together with a TI input board, is a complete digital audio amplifier system which includes digital input (S/PDIF), analog input, interface to PC, digital volume control, and failure protection. The system is designed for home theater applications such as DVD minicomponent systems, home theater in a box (HTIB), DVD receiver, A/V receiver, or TV sets.

Topic **Page**

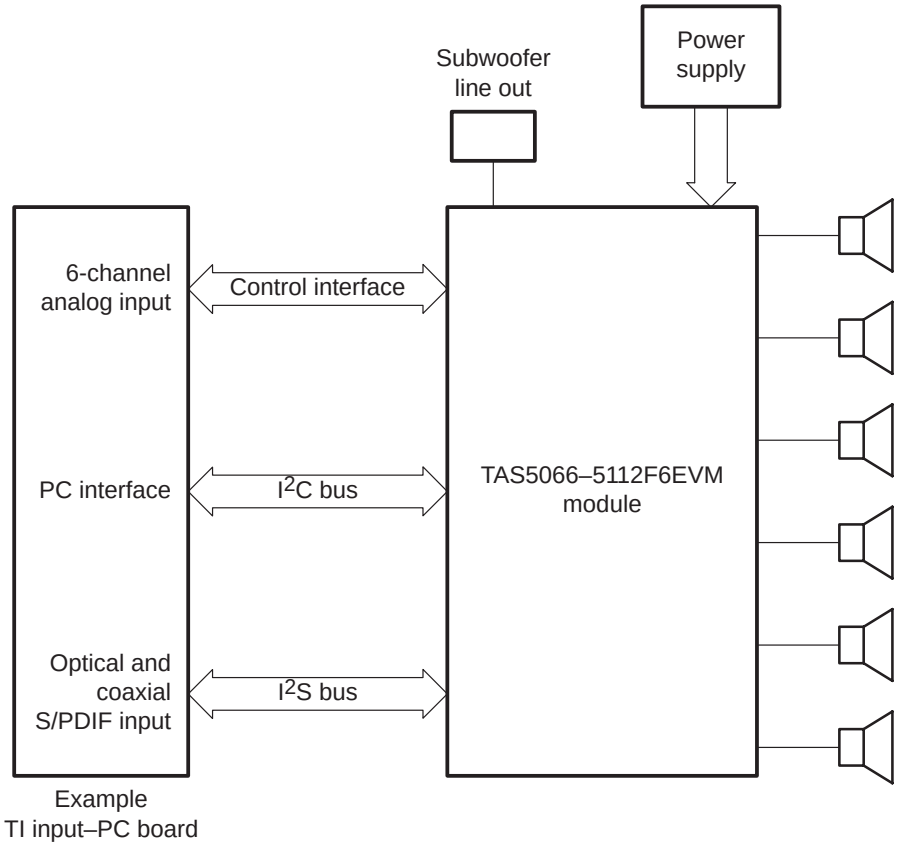
1.1 TAS5066-5112F6EVM Features 1-2

1.2 PCB Key Map 1-3

1.1 TAS5066-5112F6EVM Features

- 6-channel PurePath Digital™ reference design
- Subwoofer line out with low-pass filter
- Self-contained protection system (short circuit and thermal)
- Standard I^2S and I^2C/control connector for TI input board
- Double-sided, plated-through PCB layout

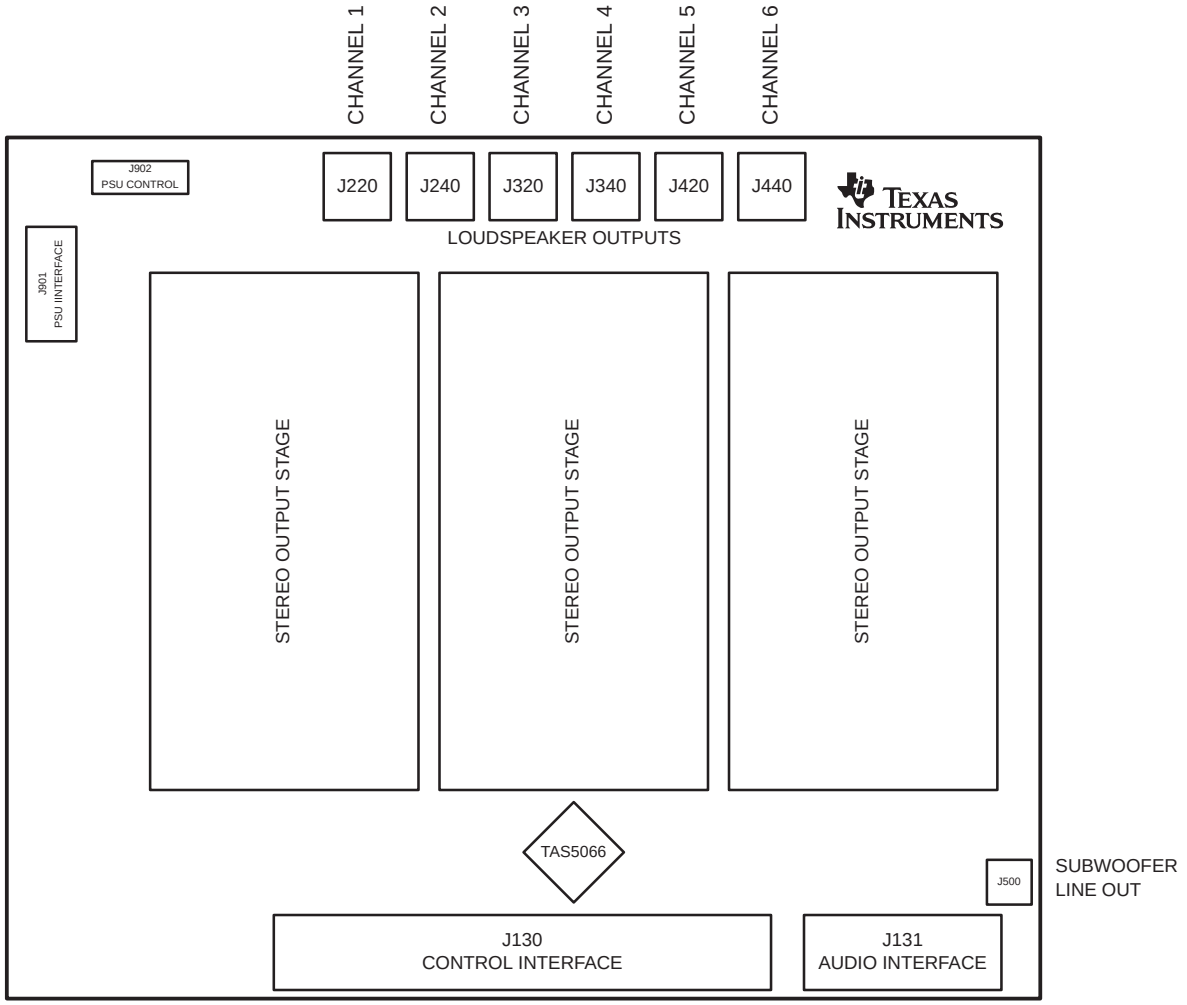
Figure 1−1. Complete PurePath Digital™ System



1.2 PCB Key Map

Figure 1−2 shows the physical structure for the TAS5066-5112F6EVM.

Figure 1−2. Physical Structure for the TAS5066-5112F6EVM



Chapter 2

System Interfaces

This chapter describes the TAS5066-5112F6EVM board in regards to power supply (PSU) and system interfaces.

Topic **Page**

2.1	PSU Interface (J901)	2-2
2.2	PSU Control Interface (J902)	2-4
2.3	Loudspeaker Connectors (J220, J240, J320, J340, J420, and J440)	2-5
2.4	Subwoofer Line Out Connector (J500)	2-6
2.5	Control Interface (J130)	2-7
2.6	Digital Audio Interface (J131)	2-8
2.7	PWM Timing, Interchannel Delay Registers	2-9

2.1 PSU Interface (J901)

The TAS5066-5112F6EVM module must be powered from one or two external regulated power supplies. High audio performance requires a stabilized output stage power supply with low ripple voltage and low output impedance.

Note:

The length of power supply cable must be minimized. Increasing the length of PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

Maximum output stage supply voltage depends on the speaker load resistance. Please check the recommended maximum supply voltage in the TAS5112A data sheet.

Table 2−1. Recommended Power Supplies

Description	Voltage Limitations (6-Ω Load)	Current Recommendations
System power supply	15 to 20 V	0.25 A
Output power stage supply	0 to 29.5 V	4 A†

† The rated current corresponds to 2-channel full scale (50 W each) or 6-channel 1/8 scale (6 W each), which most likely is adequate for a standard 6-channel amplifier design.

Figure 2−1 shows the recommended TAS5112A power-up sequence. For proper TAS5112A operation, the $\overline{\text{RESET}}$ signal must be kept low during power up. $\overline{\text{RESET}}$ is pulled low during power up for 200 ms by the onboard reset generator (U903).

Figure 2−1. Recommended Power-Up Sequence

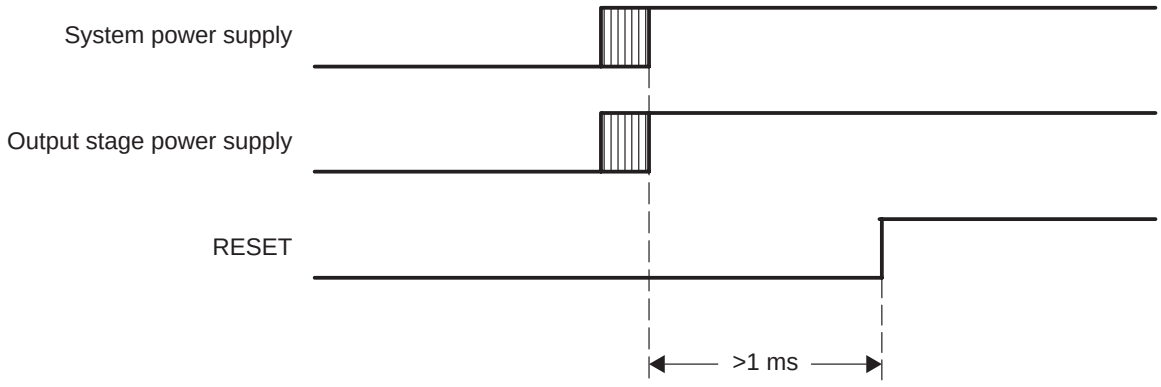


Figure 2−2. J901 Pin Numbers (PCB Connector Top View)

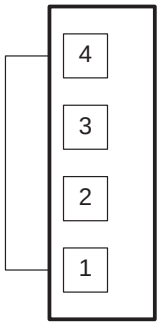


Table 2−2. J901 Pin Description

Pin Number	Net-Name on Schematics	Description
1	V-HBRIDGE	Output stage power supply
2	V+	System power supply
3	GND	Ground
4	GND	Ground

2.2 PSU Control Interface (J902)

This interface is used for onboard sensing of output supply voltage and for power supply volume control (PSCV).

Figure 2−3. J902 Pin Numbers (PCB Connector Top View)

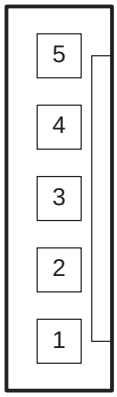


Table 2−3. J902 Pin Description

Pin Number	Net-Name on Schematics	Description
1	NOT USED	–
2	V-HBRIDGE	Sense of output supply voltage
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bidirectional)
5	PSVC	For future use

2.3 Loudspeaker Connectors (J220, J240, J320, J340, J420, and J440)

The output stage for the right and left front channels are separated into two different TAS5112A, in order to improve the stereo performance and thermal capability with continuous 0-dB sine wave during stereo power tests. Hence, the front and rear channels are covered by the same TAS5112A for each side. Also, the subwoofer channel is in a separate TAS5112A (together with the center channel), so 2.1 systems use the three-piece TAS5112A device optimally.

Table 2−4. Recommended Source/Speaker Allocation

Reference Number	I^2S Data Line	Channel Number	Description
J220	SDIN1 (a)	1	Front left channel
J240	SDIN2 (a)	3	Rear left channel
J320	SDIN1 (b)	2	Front right channel
J340	SDIN2 (b)	4	Rear right channel
J420	SDIN3 (a)	5	Center channel
J440	SDIN3 (b)	6	Subwoofer channel

CAUTION

Both positive and negative speaker outputs are floating and may not be connected to ground (e.g., through an oscilloscope).

Figure 2−4. J220, J240, J320, J340, J420, and J440 Pin Numbers (PCB Connector Top View)

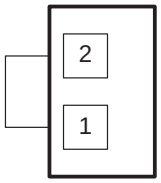


Table 2−5. J220, J240, J320, J340, J420, and J440 Pin Descriptions

Pin Number	Net-Name on Schematics	Description
1	OUT-1	Speaker negative output
2	OUT-2	Speaker positive output

2.4 Subwoofer Line Out Connector (J500)

Figure 2−5. J500 Pin Numbers (PCB Connector Top View)

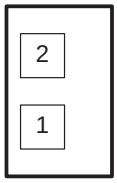


Table 2−6. J500 Pin Description

Pin Number	Net-Name on Schematics	Description
1	OUT	Subwoofer line out
2	GND	Ground

2.5 Control Interface (J130)

This interface connects the TAS5066-5112F6EVM board to a TI input board.

Table 2−7. J130 Pin Description

Pin Number	Net-Name on Schematics	Description
1	GND	Ground
2	PSVC-MCPU	Power supply volume control from (mC) input board (for future use)
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bidirectional). TAS5066 enters a 4-ms initialization sequence before PWM signals are present at the output. Activate $\overline{\text{MUTE}}$ before $\overline{\text{RESET}}$ for quiet reset.
5	$\overline{\text{ERR-RCVY}}$	Error recovery or soft reset provides click and pop free reset, without resetting I^2C volume register settings.
6	$\overline{\text{MUTE}}$	Ramp volume from any setting to noiseless soft mute. Mute can also be activated by I^2C.
7	$\overline{\text{PDN}}$	Power down. TAS5066 enters the power-down state when activated.
8, 9	RESERVED	–
10	SDA	I^2C data clock
11	GND	Ground
12	SCL	I^2C bit clock
13, 14	RESERVED	–
15	DBSPD_MODULATOR	Double speed mode
16	CLIP_MODULATOR	Clipping indicator
17	GND	Ground
18, 19	RESERVED	–
20	$\overline{\text{SHUTDOWN1}}$	Shutdown error reporting for front left, front right, and center channels. Activated if TAS5112 has high current or high temperature. See Chapter 3, Protection.
21	$\overline{\text{SHUTDOWN2}}$	Shutdown error reporting for rear left, rear right, and subwoofer channels. Activated if TAS5112 has high current or high temperature. See Chapter 3, Protection.
22	$\overline{\text{TEMP\_WARNING}}$	Temperature warning. Activated if one or more TAS5112A has reached temperature warning level
23, 24	RESERVED	–
25, 26	GND	Ground
27−30	RESERVED	–
31, 32	GND	Ground
33, 34	+5V	+5-Vdc power supply (output)

2.6 Digital Audio Interface (J131)

The digital audio interface contains digital audio signal data (I^2S), clocks, etc. See the TAS5066 data manual for signal timing and details not explained in this document.

Table 2−8. J131 Pin Description

Pin Number	Net-Name on Schematics	Description
1	GND	Ground
2	MCLK	Master clock input. Low jitter system clock for PWM generation and reclocking. Ground connection from source to TAS5066 must be a low impedance connection.
3	GND	Ground
4	SDIN1	I^2S data 1, channels 1 and 2
5	SDIN2	I^2S data 2, channels 3 and 4
6	SDIN3	I^2S data 3, channels 5 and 6
7−9	−	Reserved
10	GND	Ground
11	SCLK	I^2S bit clock
12	GND	Ground
13	LRCLK	I^2S left-right clock
14	GND	Ground
15	−	Reserved
16	GND	Ground

Table 2−9. Clock Rates

Speed	TAS5066 System Control Register 0 (x02h)	Sample Frequency (F_S)	LRCLK	SCLK (64xF_S)	MCLK
Normal speed MCLK = 256xF_S	D7 = 0 D6 = 0	32 kHz	32.0 kHz	2.0480 MHz	8.1920 MHz
		44.1 kHz	44.1 kHz	2.8224 MHz	11.2896 MHz
		48 kHz	48.0 kHz	3.0720 MHz	12.2880 MHz
Double speed MCLK = 256xF_S	D7 = 0 D6 = 1	64 kHz	64.0 kHz	4.0960 MHz	16.3840 MHz
		88 kHz	88.2 kHz	5.6448 MHz	22.5792 MHz
		96 kHz	96.0 kHz	6.1440 MHz	24.5760 MHz
Quad speed MCLK = 128xF_S	D7 = 1 D6 = 0	176 kHz	176.4 kHz	11.2896 MHz	22.5790 MHz
		192 kHz	192.0 kHz	12.2880 MHz	24.5760 MHz

2.7 PWM Timing, Interchannel Delay Registers

For maximum performance, the PWM timing must be optimized for the specific configuration and PCB layout. The default values in TAS5066 are not optimal in many designs and therefore the interchannel delays must be programmed by I^2C to the TAS5066 at start-up and after every system reset.

Table 2−10. Recommended Interchannel Delay Register Values (based on EVM designs)

Register Description	Register Address	Value (hex)
Interchannel delay channel 1	0x0C	0x01
Interchannel delay channel 2	0x0D	0x49
Interchannel delay channel 3	0x0E	0x91
Interchannel delay channel 4	0x0F	0xD9
Interchannel delay channel 5	0x10	0x21
Interchannel delay channel 6	0x11	0x69

Chapter 3

Protection

This chapter describes the short-circuit protection and fault-reporting circuitry of the TAS5112A device.

Topic **Page**

3.1	Short-Circuit Protection and Fault-Reporting Circuitry	3-2
3.2	Device Fault Reporting	3-3

3.1 Short-Circuit Protection and Fault-Reporting Circuitry

The TAS5112A is a self-protecting device that provides device fault reporting (including high-temperature protection and short-circuit protection). The TAS5112A is configured in back-end, auto-recovery mode and therefore resets automatically after all errors (M1, M2, and M3 are set low). This means that the device re-starts itself after an error occurs and reports the short through the $\overline{\text{SHUTDOWN1}}$ and $\overline{\text{SHUTDOWN2}}$ error signals.

The shutdown report signals are separated into two wires $\overline{\text{SHUTDOWN1}}$ and $\overline{\text{SHUTDOWN2}}$. $\overline{\text{SHUTDOWN1}}$ covers the primary information channels (front channels and center), where the $\overline{\text{SHUTDOWN2}}$ covers the secondary information channels (rear channels and subwoofer). Thereby, the microprocessor can react differently on errors depending on the primary- or secondary-channel faults, e.g., lowering output level or shutting down the secondary channels on continuous error reporting from one of those, where the primary channels continue. See Table 3−1 for channel allocation.

Table 3−1. Channel Allocation

Description	Terminal	Error Signal
Front left	J220	$\overline{\text{SHUTDOWN1}}$
Front right	J320	$\overline{\text{SHUTDOWN1}}$
Rear left	J240	$\overline{\text{SHUTDOWN2}}$
Rear right	J340	$\overline{\text{SHUTDOWN2}}$
Center	J420	$\overline{\text{SHUTDOWN1}}$
Subwoofer	J440	$\overline{\text{SHUTDOWN2}}$

3.2 Device Fault Reporting

The $\overline{\text{OTW}}$, $\overline{\text{SD\_AB}}$, and $\overline{\text{SD\_CD}}$ outputs from TAS5112A indicate fault conditions. See the TAS5112 data manual for a description of these pins.

Table 3−2. TAS5112A Error Signal Decoding

$\overline{\text{OTW}}$	$\overline{\text{SD\_XX}}$	Device Condition
0	0	High-temperature error and/or high-current error
0	1	High-temperature warning
1	0	Undervoltage lockout or high-current error
1	1	Normal operation, no errors/warnings

The temperature warning ($\overline{\text{OTW}}$) signals at the TAS5066-5112F6EVM board are wire-ORed to one temperature warning signal ($\overline{\text{TEMP\_WARNING}}$ – pin 22 in the control interface connector). Shutdown signals ($\overline{\text{SD\_AB}}$ and $\overline{\text{SD\_CD}}$) are wire-ORed to two shutdown signals ($\overline{\text{SHUTDOWN1}}$ and $\overline{\text{SHUTDOWN2}}$ – pin 20 and pin 21 in the control interface connector). The shutdown signals, together with the temperature warning signal, give information on the chip state information as described in Table 3−2 above.
Device fault-reporting outputs are open-drain outputs.