

PSMN017-30EL

N-channel 30 V 17 mΩ logic level MOSFET in I2PAK

Rev. 2 — 3 April 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in I2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

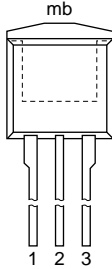
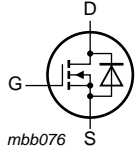
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	30	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	[1]	-	32	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	47	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 10 A; T _j = 25 °C; see Figure 13	-	18.7	23.4	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; see Figure 13	-	13.4	17	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 10 A; V _{DS} = 15 V; see Figure 14 ; see Figure 15	-	1.94	-	nC
Q _{G(tot)}	total gate charge		-	5.1	-	nC
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 32 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped	-	-	13	mJ

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		
			SOT226 (I2PAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN017-30EL	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

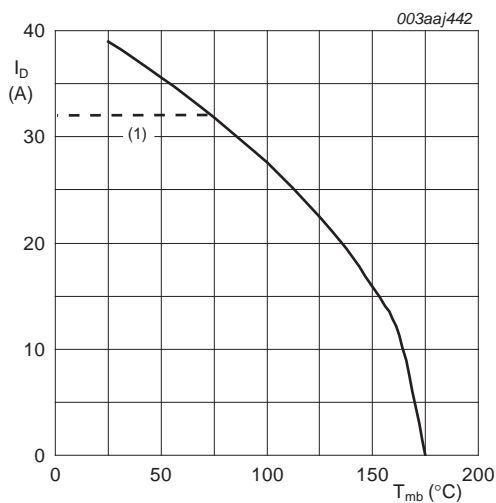
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	[1]	25.5	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	[1]	32	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	154	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	47	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	32	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	154	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 32\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	13	mJ

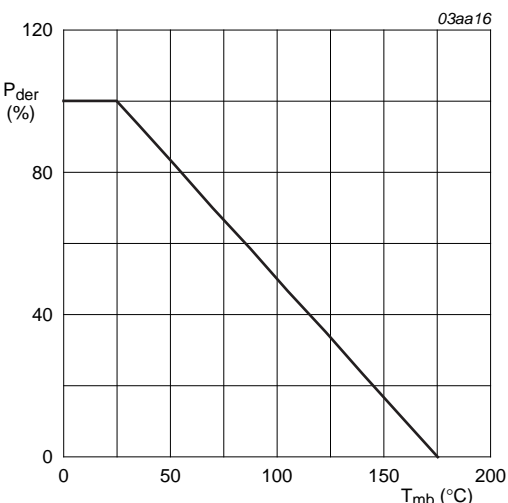
[1] Continuous current is limited by package.



$V_{GS} \geq 10V$

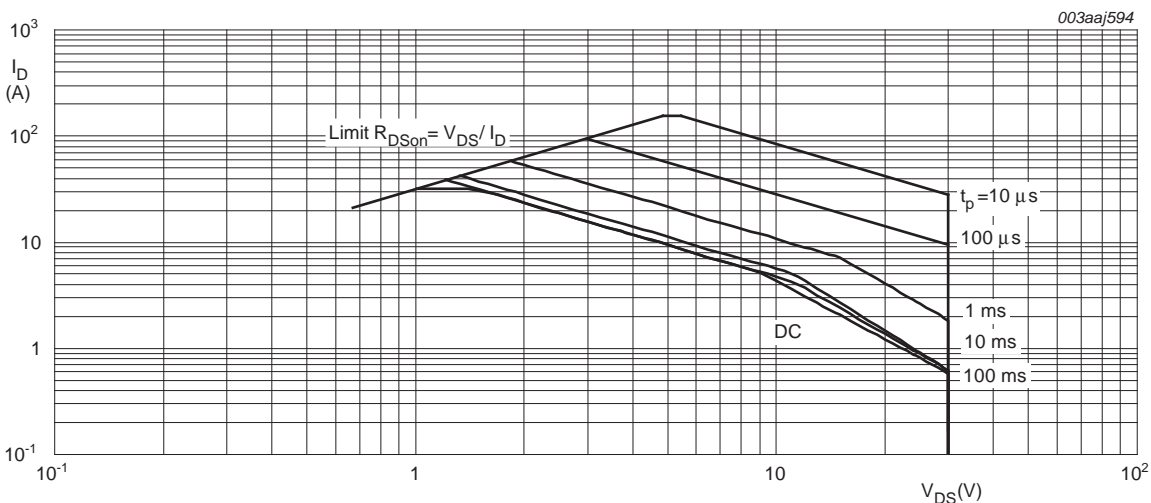
(1) Capped at 32A due to package

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



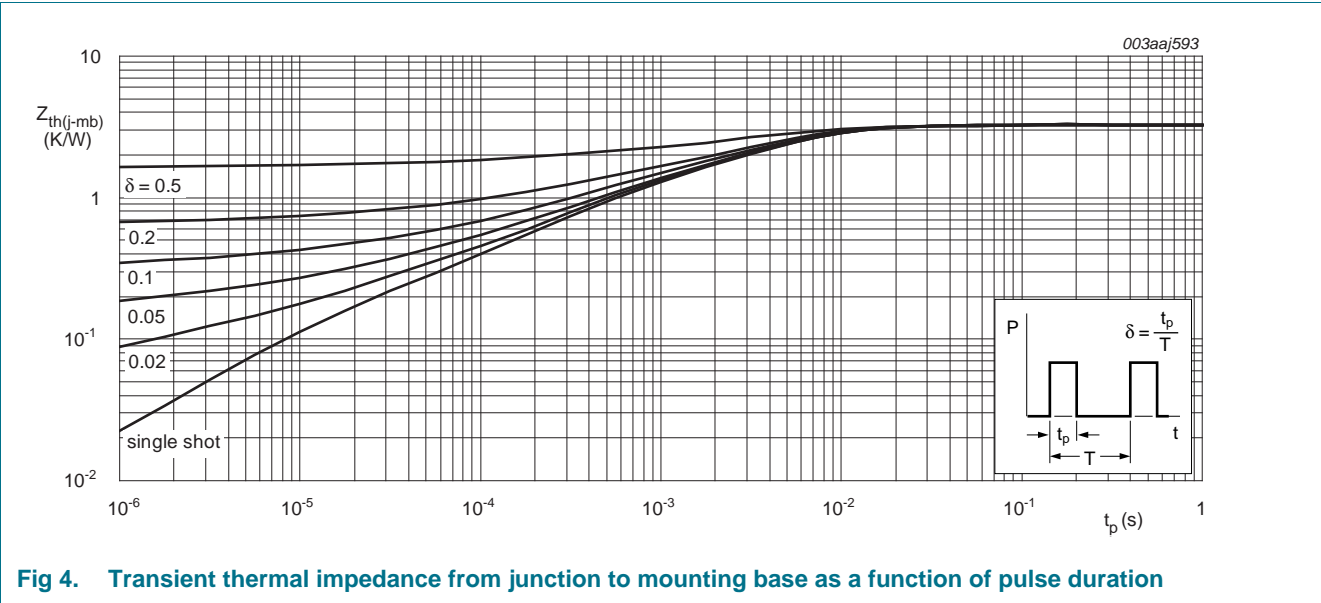
$T_{mb} = 25^{\circ}C; I_{DM}$ is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	3.18	3.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	60	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	30	-	-	V
		$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = -55\ ^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ\text{C}$; see Figure 10 ; see Figure 11	1.3	1.7	2.15	V
		$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 175\ ^\circ\text{C}$; see Figure 11	0.5	-	-	V
		$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ\text{C}$	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	0.3	1	μA
		$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 125\ ^\circ\text{C}$	-	-	50	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -16\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}$; $I_D = 10\ \text{A}$; $T_j = 175\ ^\circ\text{C}$; see Figure 12	-	-	43.2	mΩ
		$V_{GS} = 4.5\ \text{V}$; $I_D = 10\ \text{A}$; $T_j = 25\ ^\circ\text{C}$; see Figure 13	-	18.7	23.4	mΩ
		$V_{GS} = 10\ \text{V}$; $I_D = 10\ \text{A}$; $T_j = 175\ ^\circ\text{C}$; see Figure 12	-	24	31.5	mΩ
		$V_{GS} = 10\ \text{V}$; $I_D = 10\ \text{A}$; $T_j = 100\ ^\circ\text{C}$; see Figure 12	-	-	23.5	mΩ
		$V_{GS} = 10\ \text{V}$; $I_D = 10\ \text{A}$; $T_j = 25\ ^\circ\text{C}$; see Figure 13	-	13.4	17	mΩ
R_G	gate resistance	$f = 1\ \text{MHz}$	-	2.03	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10\ \text{A}$; $V_{DS} = 15\ \text{V}$; $V_{GS} = 10\ \text{V}$; see Figure 14 ; see Figure 15	-	10.7	-	nC
		$I_D = 0\ \text{A}$; $V_{DS} = 0\ \text{V}$; $V_{GS} = 10\ \text{V}$; see Figure 14 ; see Figure 15	-	9.55	-	nC
		$I_D = 10\ \text{A}$; $V_{DS} = 15\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 14 ; see Figure 15	-	5.1	-	nC
Q_{GS}	gate-source charge		-	1.52	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.5	-	nC
Q_{GD}	gate-drain charge		-	1.94	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 10\ \text{A}$; $V_{DS} = 15\ \text{V}$; see Figure 14 ; see Figure 15	-	2.86	-	V
C_{iss}	input capacitance	$V_{DS} = 15\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$;	-	552	-	pF
C_{oss}	output capacitance	$T_j = 25\ ^\circ\text{C}$; see Figure 16	-	127	-	pF
C_{rss}	reverse transfer capacitance		-	64	-	pF

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; R _L = 1.5 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 5 Ω	-	10.7	-	ns
t _r	rise time		-	9.2	-	ns
t _{d(off)}	turn-off delay time		-	11.4	-	ns
t _f	fall time		-	5.1	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 10 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 17	-	0.89	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs;	-	17.3	-	ns
Q _r	recovered charge	V _{GS} = 0 V; V _{DS} = 15 V	-	6.5	-	nC

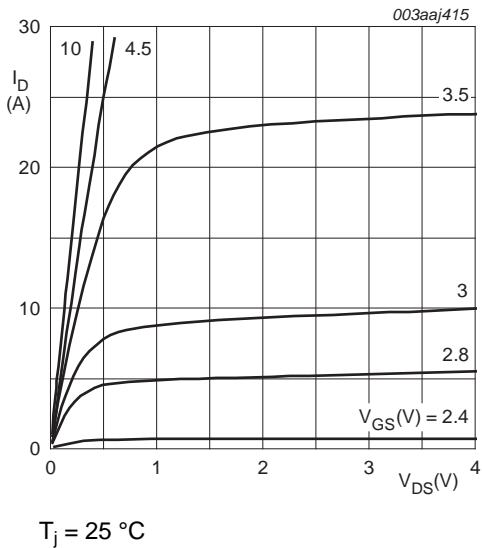


Fig 5. Output characteristics; drain current as a function of drain-source voltage; typical values

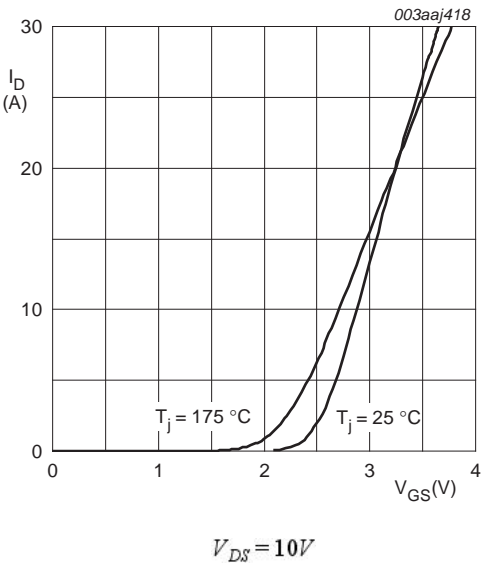
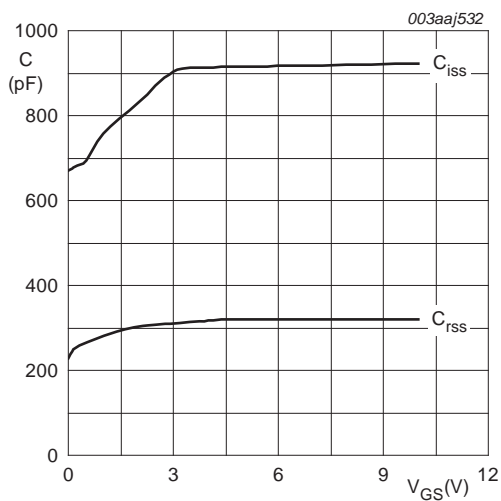
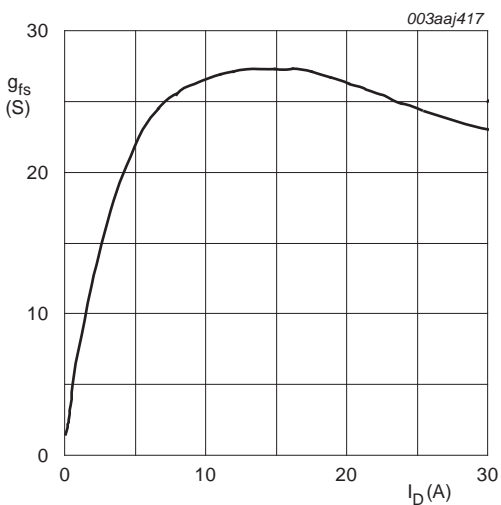


Fig 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values



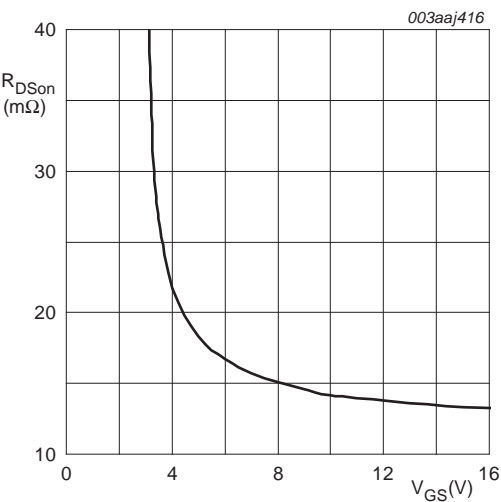
$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



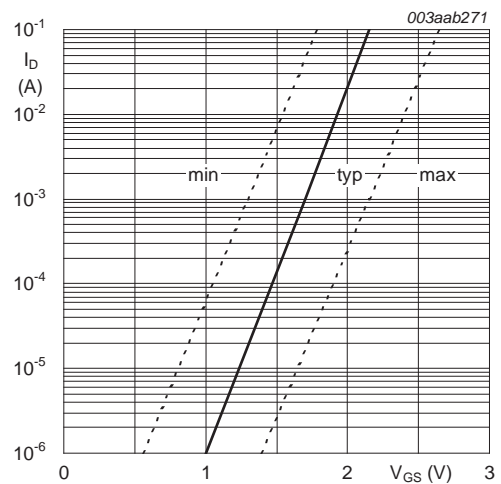
$T_j = 25^\circ\text{C}; V_{DS} = 10\text{ V}$

Fig 8. Forward transconductance as a function of drain current; typical values



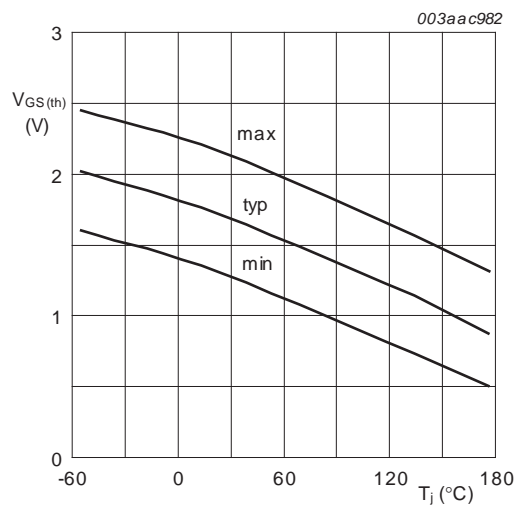
$T_j = 25^\circ\text{C}; I_D = 10\text{ A}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



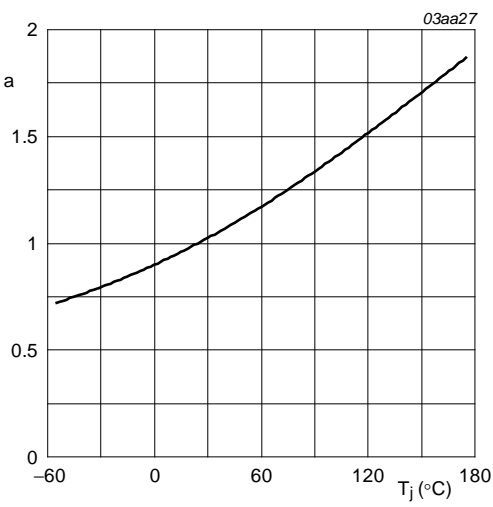
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



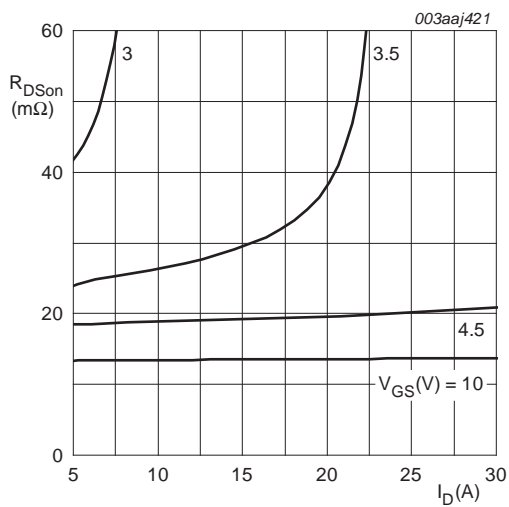
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



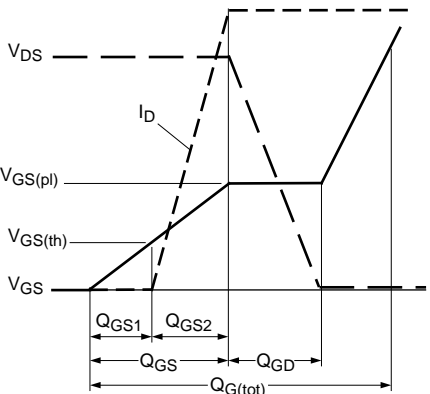
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ\text{C}$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values



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Fig 14. Gate charge waveform definitions

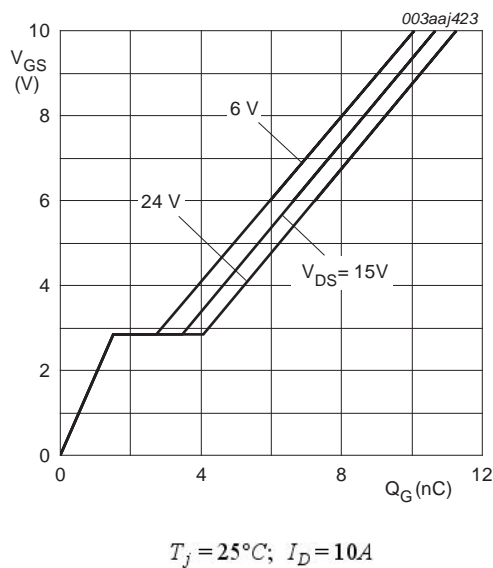


Fig 15. Gate-source voltage as a function of gate charge; typical values

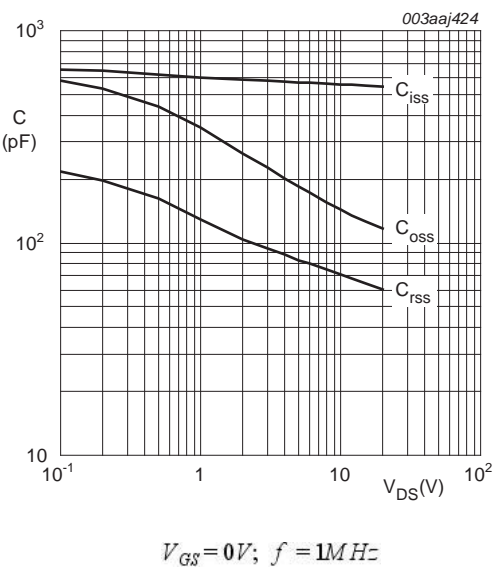


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

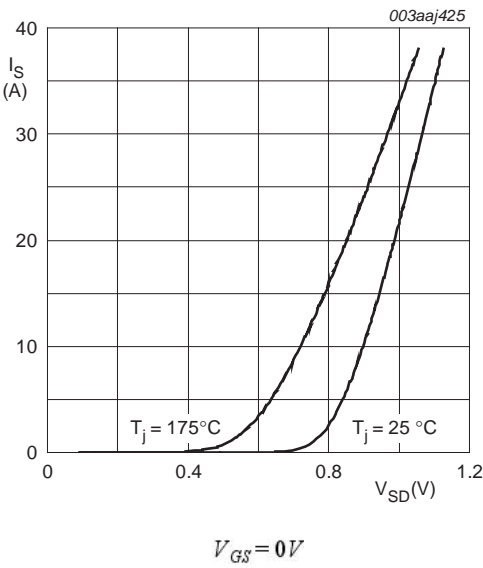


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-262

SOT226

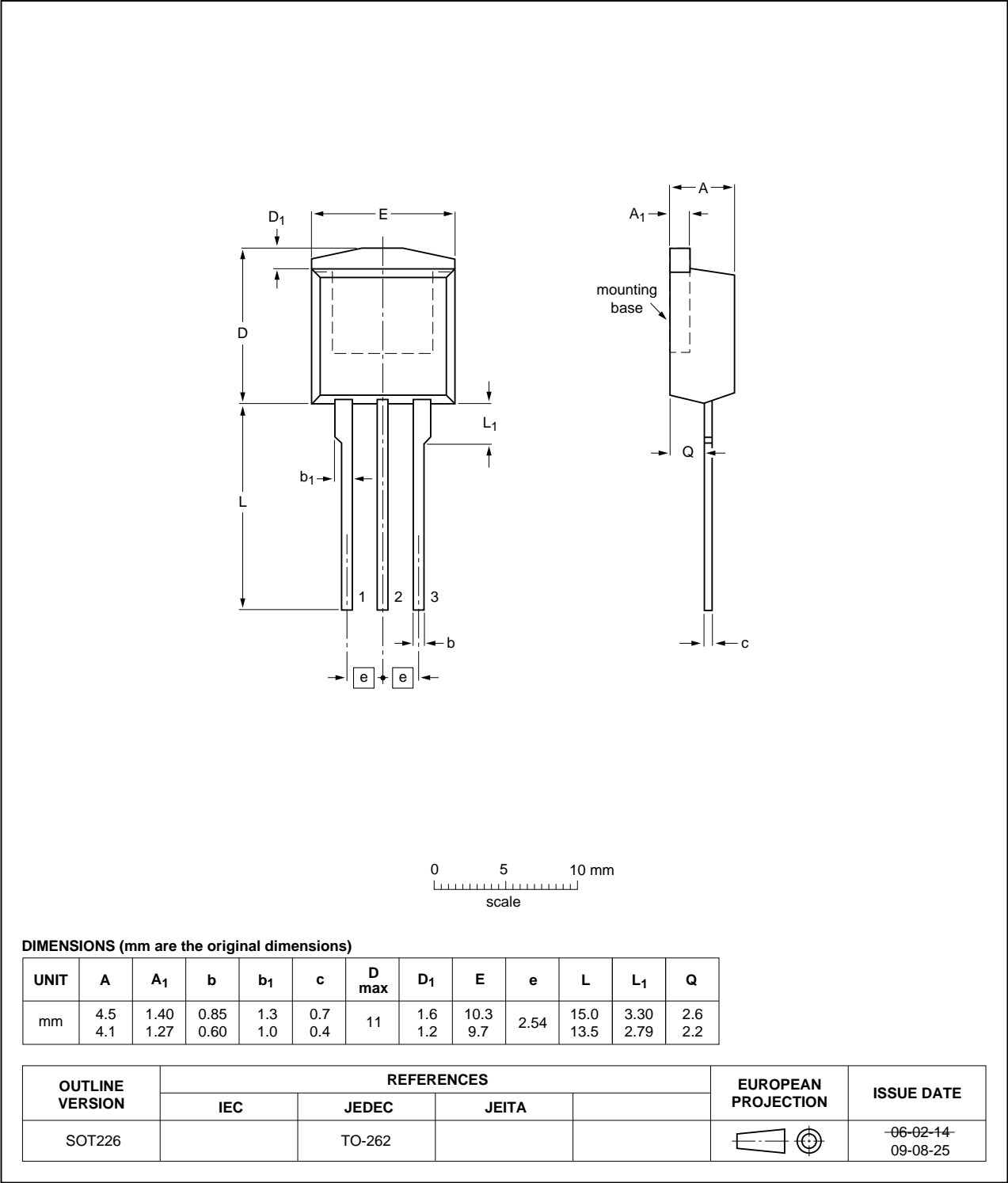


Fig 18. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN017-30EL v.2	20120403	Product data sheet	-	PSMN017-30EL v.1
Modifications:	<ul style="list-style-type: none">• Status changed from objective to product.• Various changes to content.			
PSMN017-30EL v.1	20120228	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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