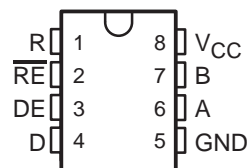


- Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27
- Recommended for PROFIBUS Applications
- Operates at Data Rates up to 35 Mbaud
- Operating Temperature Range
... -25°C to 85°C
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirement
... 30 mA Max
- Wide Positive and Negative Input/Output Bus-Voltage Ranges
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fail-Safe Design
- Package Options Include Plastic Small-Outline (D) Package and (P) DIPs

D[†] OR P PACKAGE
(TOP VIEW)



[†] The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN65ALS1176DR).

description

The SN65ALS1176 differential bus transceiver is designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.

The SN65ALS1176 combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS1176 is characterized for operation from -25°C to 85°C .



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
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SN65ALS1176

DIFFERENTIAL BUS TRANSCEIVER

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Function Tables

DRIVERS

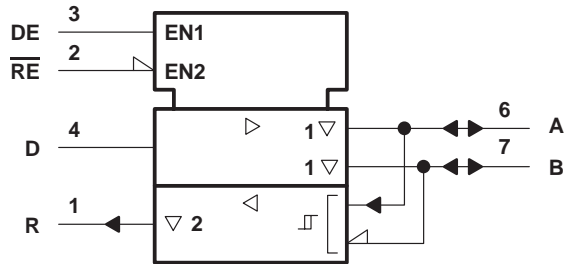
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE \overline{RE}	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Inputs open	L	H

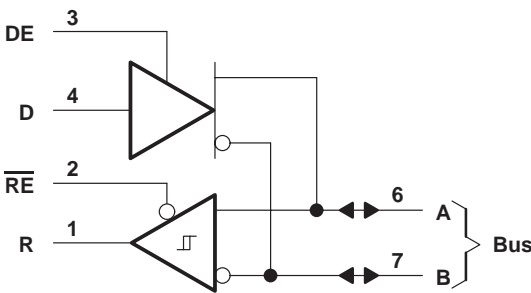
H = high level, L = low level, X = irrelevant,
? = Indeterminate, Z = high impedance (off)

logic symbol†

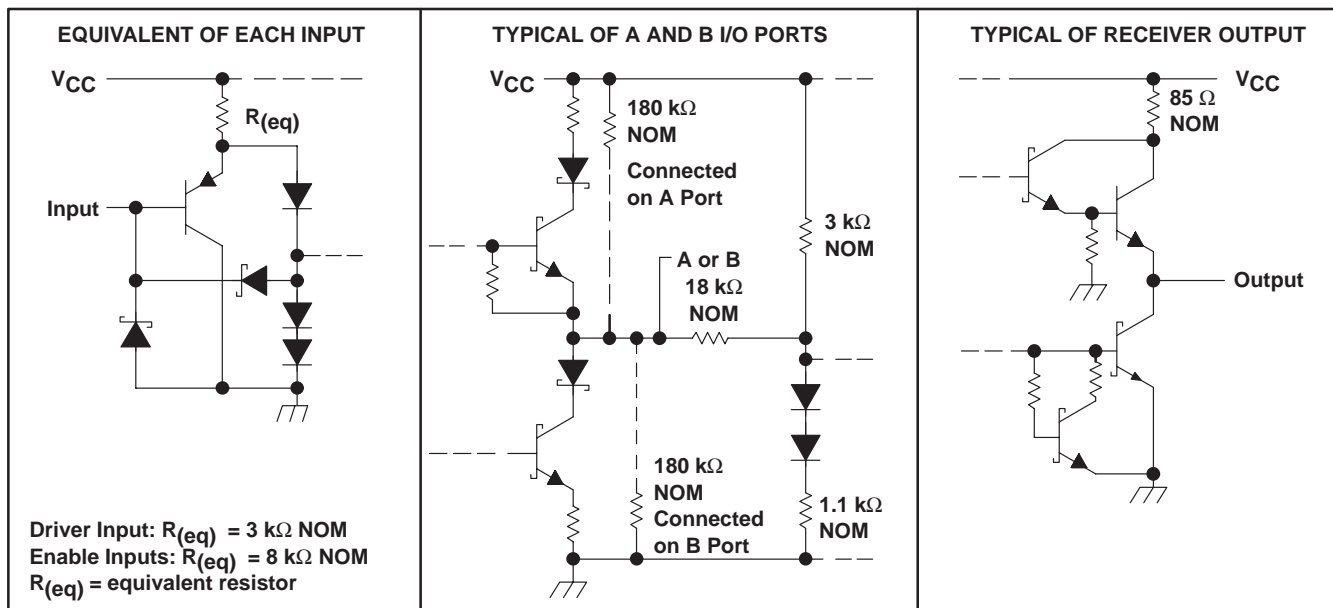


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage range at any bus terminal	–7 V to 12 V
Enable input voltage, V_I	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package	97°C/W
P package	85°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				–7	
High-level input voltage, V_{IH}	D, DE, and \overline{RE}	2			V
Low-level input voltage, V_{IL}	D, DE, and \overline{RE}			0.8	V
Differential input voltage, V_{ID} (see Note 3)				±12	V
High-level output current, I_{OH}	Driver			–60	mA
	Receiver			–400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		–25		85	°C

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

SN65ALS1176

DIFFERENTIAL BUS TRANSCEIVER

SLLS295A – APRIL 1998 – REVISED DECEMBER 1999

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION†	MIN	TYP‡	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_O Output voltage	$I_O = 0$	0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		6	V
$ V_{OD2} $ Differential output voltage	$R_L = 100 \Omega$, See Figure 1	$1/2 V_{OD1}$ or 2§			V
	$R_L = 54 \Omega$, See Figure 1	2.1	2.5	5	V
V_{OD3} Differential output voltage	$V_{test} = -7 \text{ V to } 12 \text{ V}$, See Figure 2	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of differential output voltage¶	$R_L = 54 \Omega$ or 100Ω , See Figure 1			± 0.2	V
V_{OC} Common-mode output voltage				3 -1	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage¶				± 0.2	V
I_O Output current	Outputs disabled, See Note 4	$V_O = 12 \text{ V}$		1	mA
		$V_O = -7 \text{ V}$		-0.8	
I_{IH} High-level input current	$V_I = 2.4 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_I = 0.4 \text{ V}$			-400	μA
I_{OS} Short-circuit output current#	$V_O = -4 \text{ V}$			-250	mA
	$V_O = 0$			-150	
	$V_O = V_{CC}$			250	
	$V_O = 8 \text{ V}$			250	
I_{CC} Supply current	No load	Outputs enabled	23	30	mA
		Outputs disabled	19	26	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

§ The minimum V_{OD2} with a $100\text{-}\Omega$ load is either $1/2 V_{OD1}$ or 2 V , whichever is greater.

¶ $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from one logic state to the other.

Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for both power on and power off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54\ \Omega$, See Figure 3		0	15	ns
$t_{sk(p)}$	Pulse skew‡				2	ns
$t_{t(OD)}$	Differential output transition time				8	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$, See Figure 4			80	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$, See Figure 5			30	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$, See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$, See Figure 5			30	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{Oa}, V_{Ob}	V_{Oa}, V_{Ob}
$ V_{OD1} $	V_O	V_O
$ V_{OD2} $	$V_t (R_L = 100\ \Omega)$	$V_t (R_L = 54\ \Omega)$
$ V_{OD3} $	None	V_t (test termination measurement 2)
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - \bar{V}_{os} $	$ V_{os} - \bar{V}_{os} $
I_{OS}	$ I_{sa} , I_{sb} $	None
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

SN65ALS1176

DIFFERENTIAL BUS TRANSCEIVER

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RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+} Positive-going input threshold voltage	$V_O = 2.7\text{ V}$, $I_O = -0.4\text{ mA}$			0.2	V
V_{IT-} Negative-going input threshold voltage	$V_O = 0.5\text{ V}$, $I_O = 8\text{ mA}$	$-0.2\ddagger$			V
V_{hys} Hysteresis voltage ($V_{IT+} - V_{IT-}$)			60		mV
V_{IK} Enable-input clamp voltage	$I_I = -18\text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{ID} = 200\text{ mV}$, See Figure 6 $I_{OH} = -400\text{ }\mu\text{A}$,	2.7			V
V_{OL} Low-level output voltage	$V_{ID} = -200\text{ mV}$, See Figure 6 $I_{OL} = 8\text{ mA}$,			0.45	V
I_{OZ} High-impedance-state output current	$V_O = 0.4\text{ V to } 2.4\text{ V}$			± 20	μA
V_I Line input current	Other input = 0 V, See Note 5 $V_I = 12\text{ V}$ $V_I = -7\text{ V}$			1 -0.8	mA
I_{IH} High-level-enable input current	$V_{IH} = 2.7\text{ V}$			20	μA
I_{IL} Low-level-enable input current	$V_{IL} = 0.4\text{ V}$			-100	μA
r_I Input resistance		12	20		$\text{k}\Omega$
I_{OS} Short-circuit output current	$V_{ID} = 200\text{ mV}$, $V_O = 0$	-15		-85	mA
I_{CC} Supply current	No load				
	Outputs enabled		23	30	mA
	Outputs disabled		19	26	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd} Propagation time	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$, $C_L = 15\text{ pF}$, See Figure 7			25	ns
$t_{sk(p)}$ Pulse skew§			0	2	ns
t_{pZH} Output enable time to high level	$C_L = 15\text{ pF}$, See Figure 8		11	18	ns
t_{pZL} Output enable time to low level			11	18	ns
t_{PHZ} Output disable time from high level				50	ns
t_{PLZ} Output disable time from low level				30	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.



PARAMETER MEASUREMENT INFORMATION

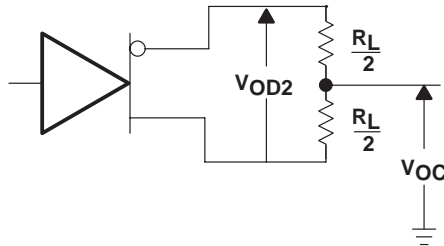


Figure 1. Driver V_{OD2} and V_{OC} Test Circuit

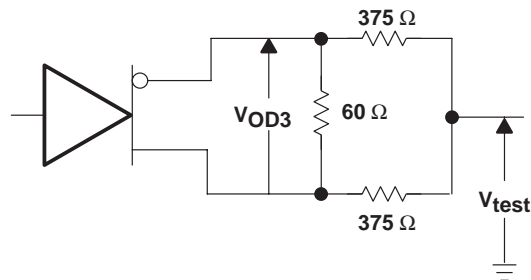
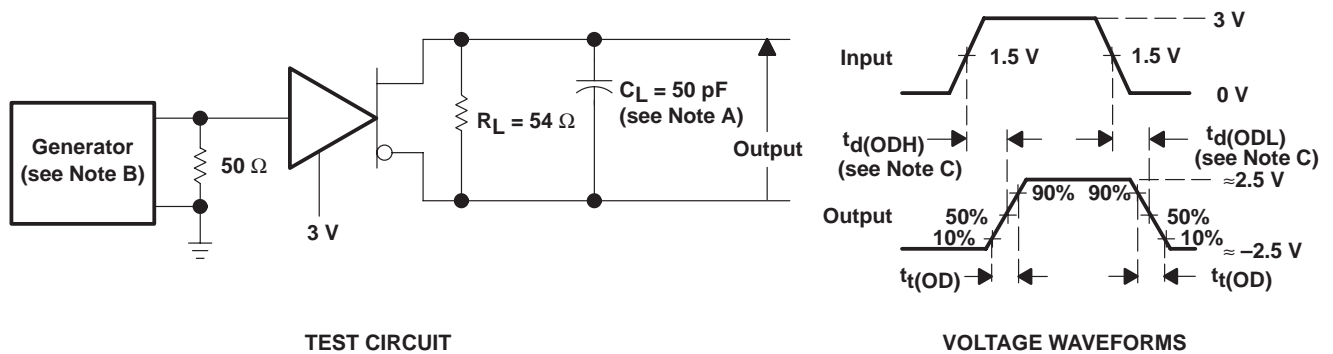


Figure 2. Driver V_{OD3} Test Circuit



TEST CIRCUIT

VOLTAGE WAVEFORMS

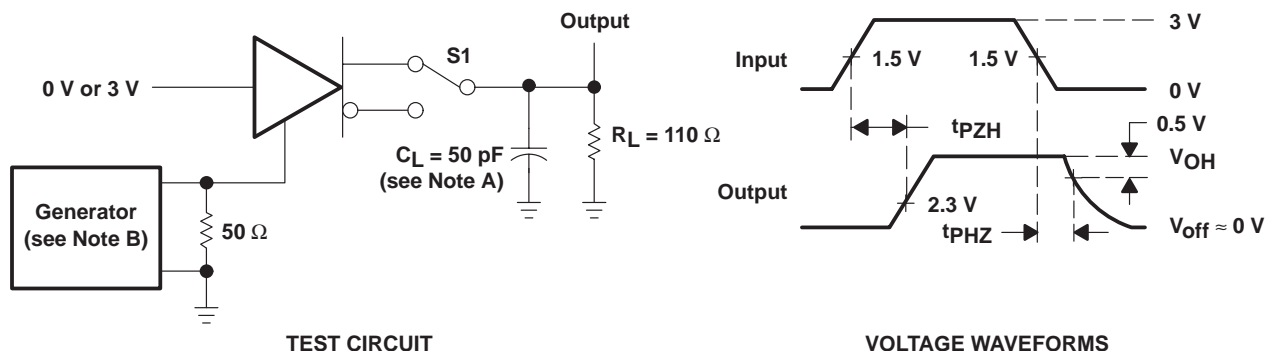
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 - C. $t_d(OD) = t_d(ODH)$ or $t_d(ODL)$

Figure 3. Driver Differential-Output Delay and Transition Times

SN65ALS1176 DIFFERENTIAL BUS TRANSCEIVER

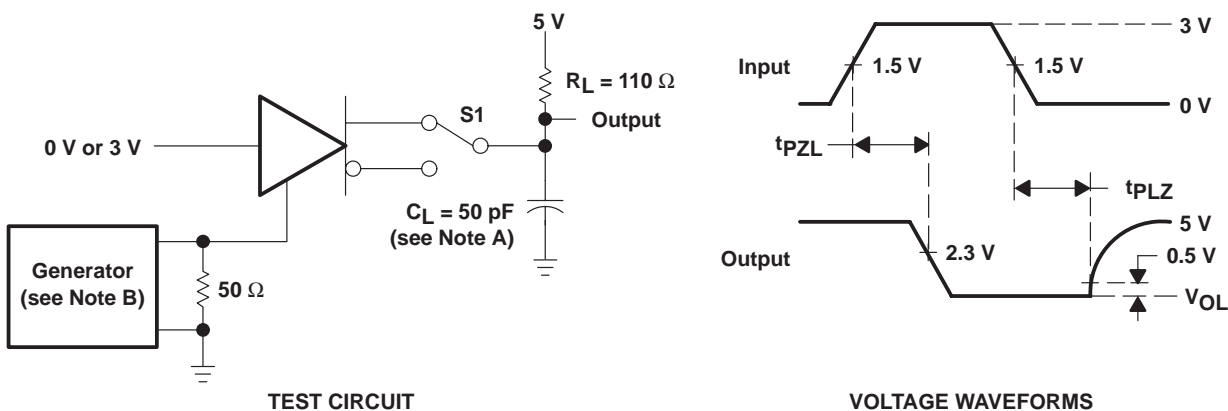
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 4. Driver Enable and Disable Times



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 5. Driver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION

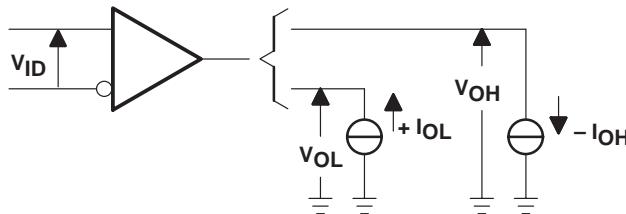
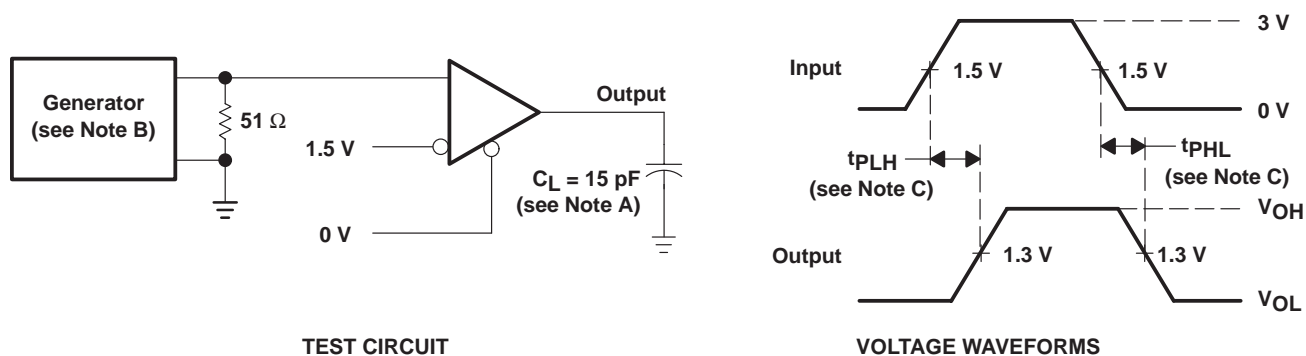


Figure 6. Receiver V_{OH} and V_{OL} Test Circuit



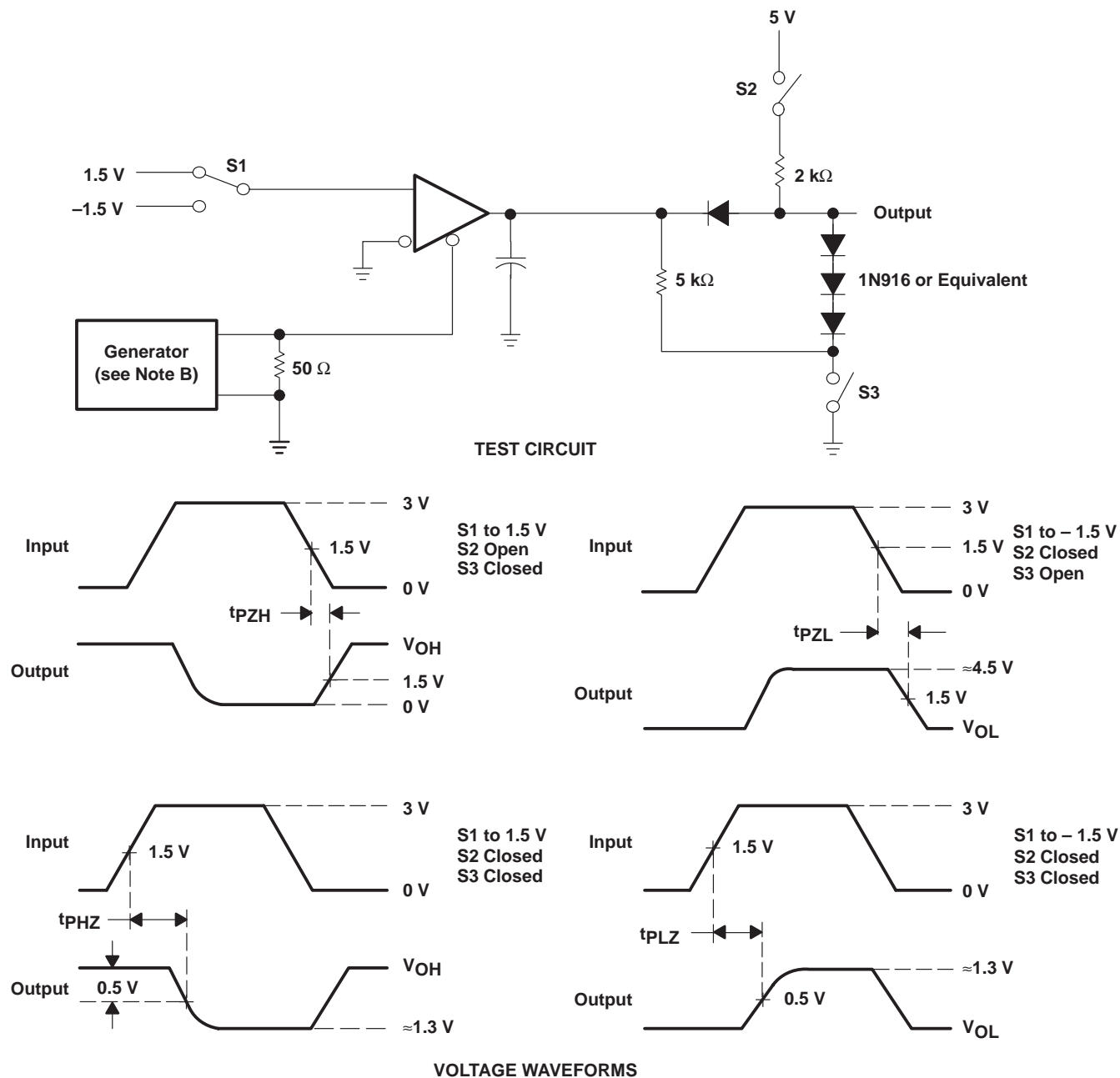
- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
C. $t_{pd} = t_{PLH}$ or t_{PHL}

Figure 7. Receiver Propagation-Delay Times

SN65ALS1176 DIFFERENTIAL BUS TRANSCEIVER

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PARAMETER MEASUREMENT INFORMATION

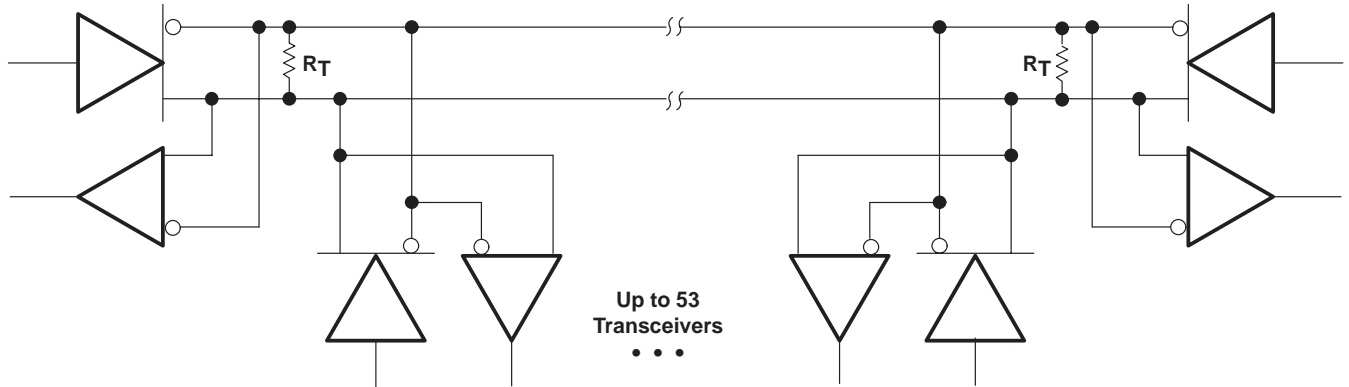


NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 8. Receiver Output Enable and Disable Times

APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 9. Typical Application Circuit

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65ALS1176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65ALS1176DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65ALS1176DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65ALS1176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65ALS1176DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65ALS1176DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65ALS1176P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65ALS1176PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

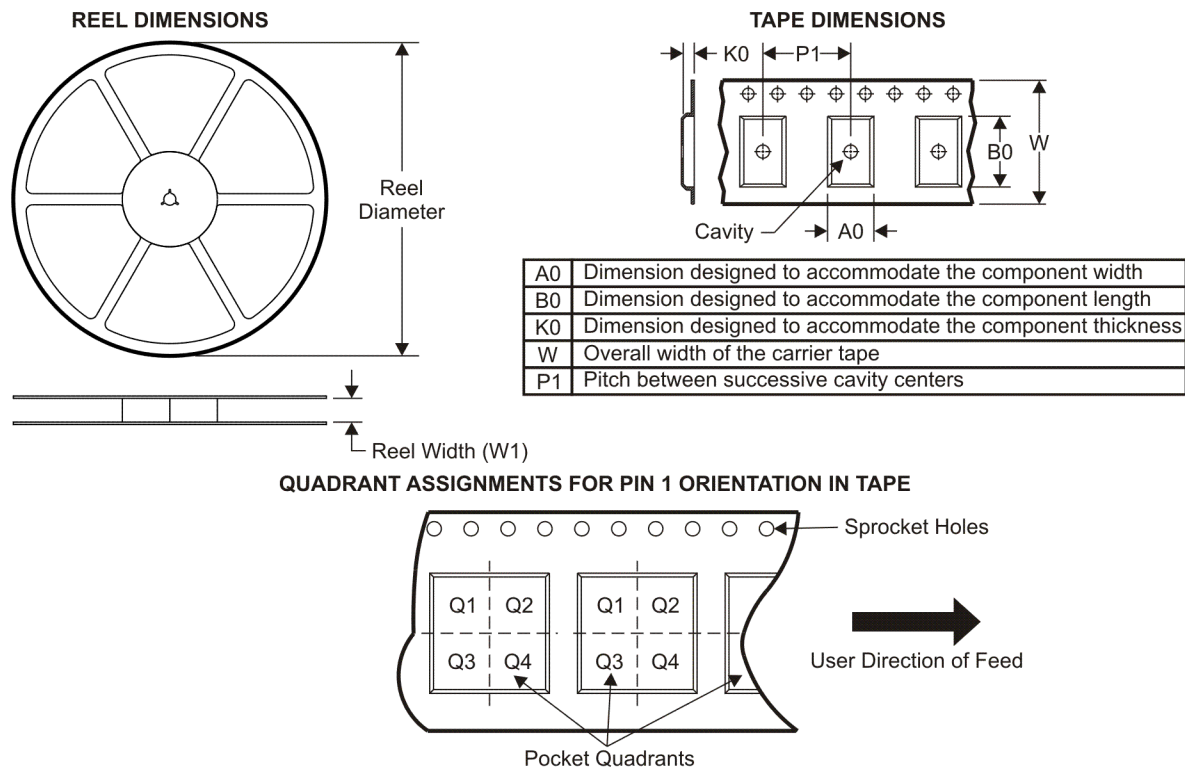
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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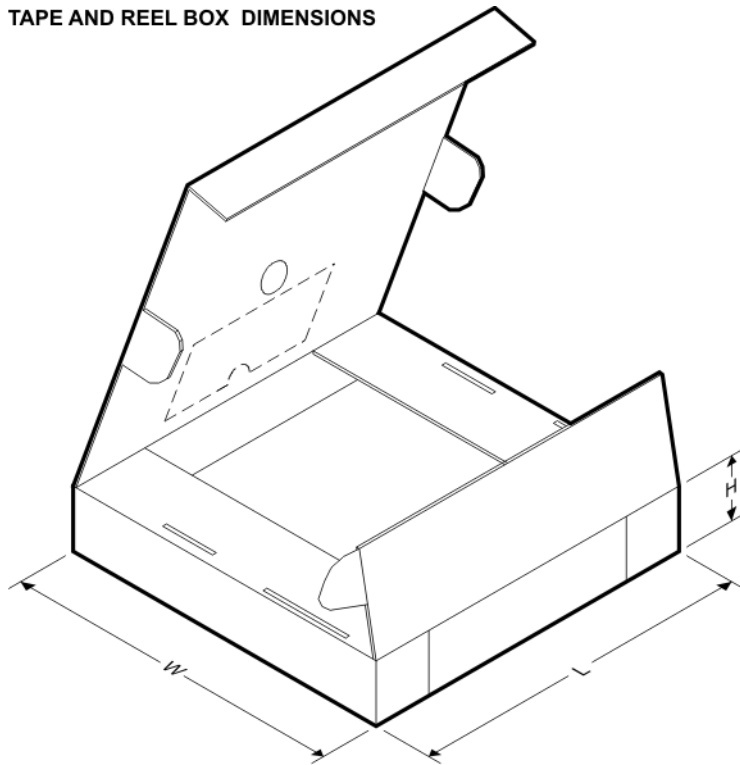
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

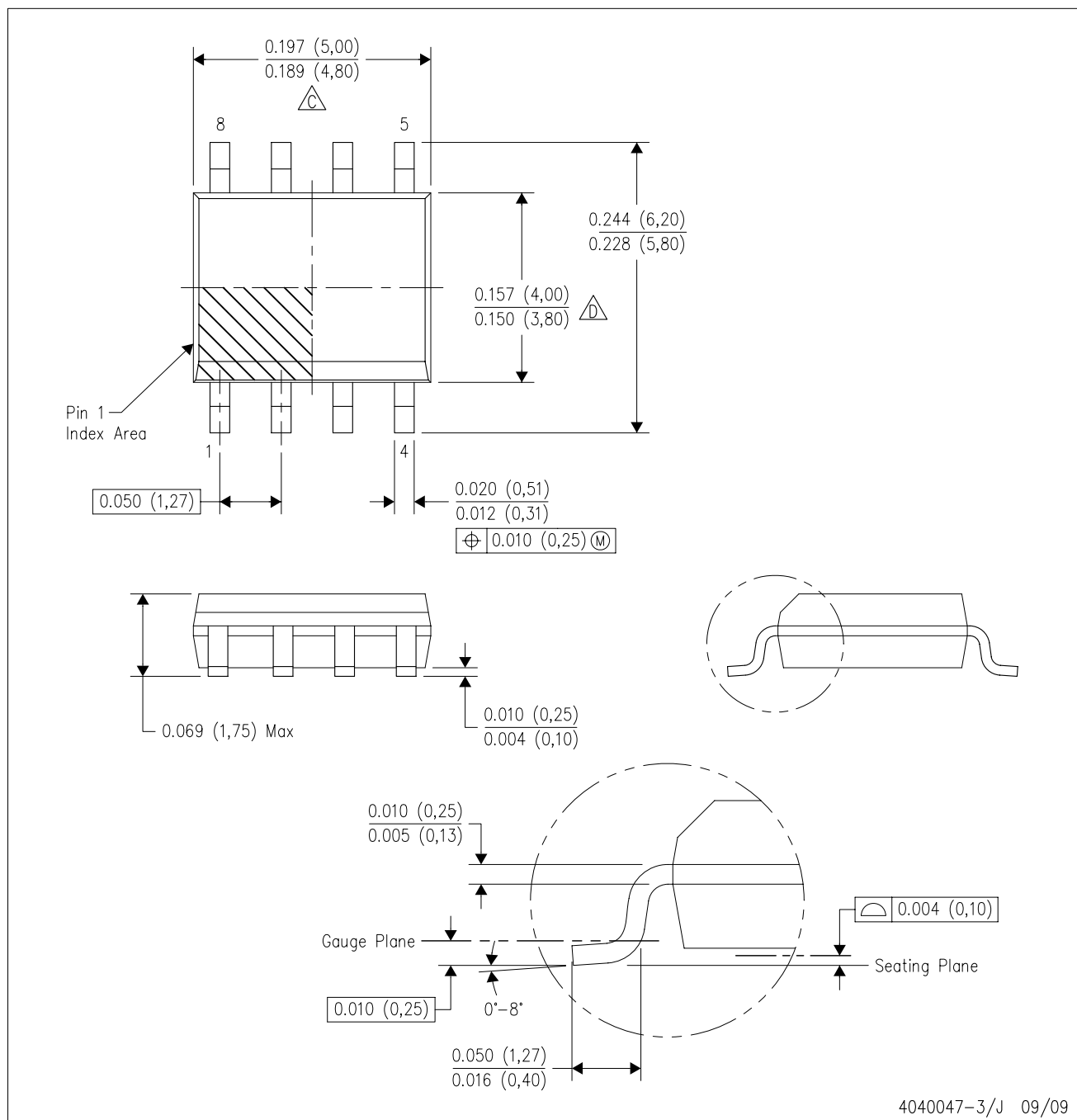


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS1176DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8)

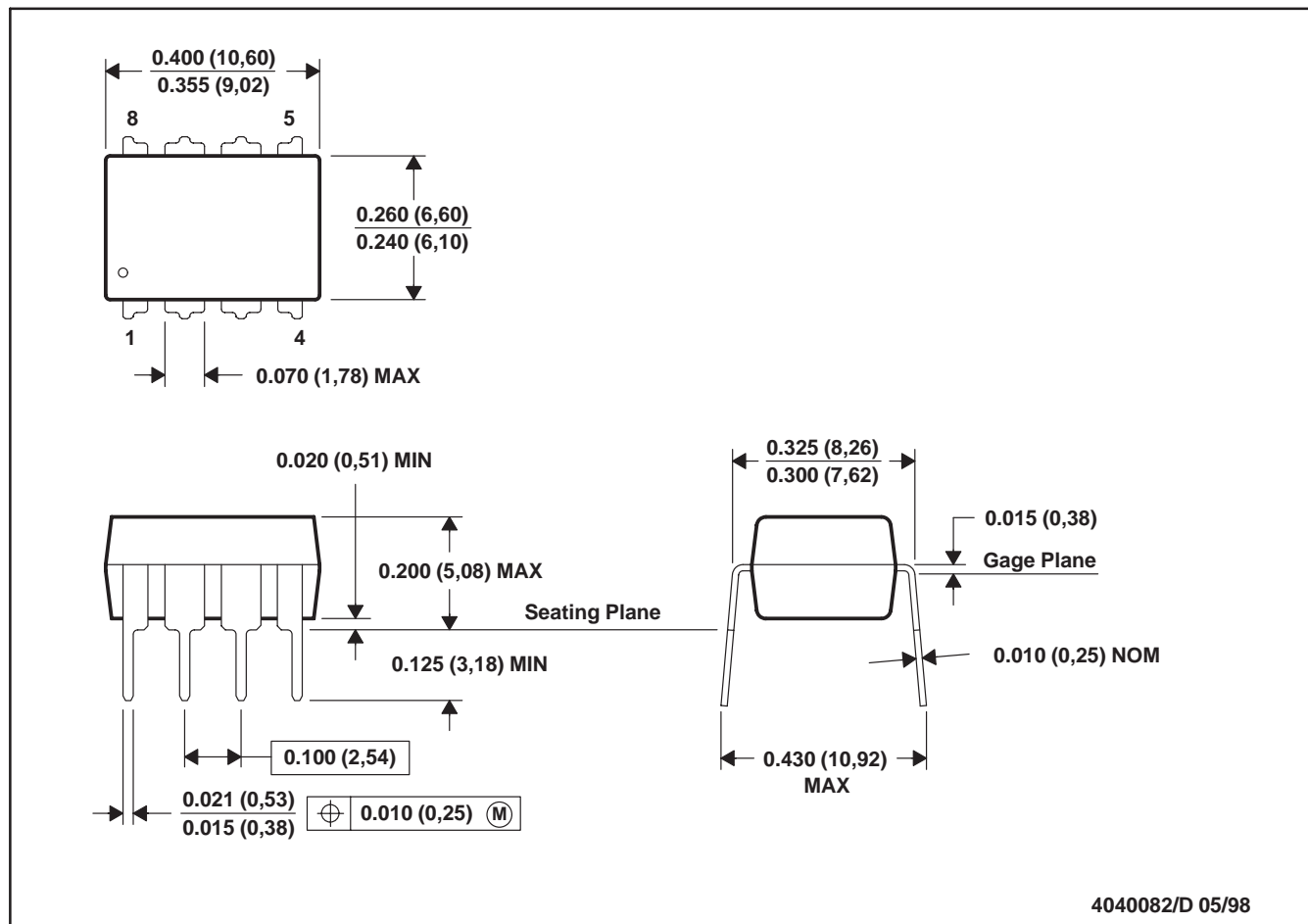
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

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