Data Sheet, DS1, June 2003

Ringing FlexiSLIC

Subscriber Line Interface Circuit

PBL 38774/1, Version 2.0

Wired Communications

Never stop thinking.

Ringing FlexiSLIC

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Ringing FlexiSLIC
Subscriber Line Interface Circuit

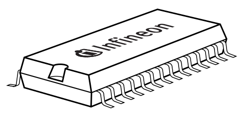
PBL 38774/1

Version 2.0

1 Overview

1.1 Features

- On-chip ringing generation
  – Balanced, up to 81 VPeak
  – Any waveform
  – 5 REN ringing load
  – Automatic gain control of ring signal (AGC-R)
  – Short circuit safe
- Low on-hook power consumption in Active (65 mW @ V_{BAT} = -80 V)
- Automatic current controlled battery switching between on-hook battery (V_{BAT}) and talk battery (V_{TBAT})
- Pulse metering and on-hook transmission
- UL-1950 and MTU compliant on-hook line voltage
- 3.3 V compatible logic interface
- Programmable Ring-Trip level
- Silent or fast polarity reversal



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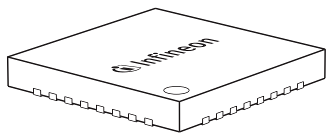


P-VQFN-32-6

1.2 Typical Applicationsh

- Integrated Access Device (IAD)
- Residential gateways
- Voice over DSL (VoDSL)
- Voice over IP (VoIP)
- Terminal adapters (CPE)
- ISDN terminal adapters
- Routers
- Cable modems
- Other Shortloop applications

Type	Package
PBL 38774/1 SO	P-DSO-28-20
PBL 38774/1 ML	P-VQFN-32-6

1.3 Description

The ringing FlexiSLIC PBL 38774/1 Subscriber Line Interface Circuit (SLIC) is a 90 V bipolar integrated circuit for use in short loop applications. The PBL 38774/1 SLIC has been optimized for low power consumption, low total line interface cost and for a high degree of flexibility in various applications.

The PBL 38774/1 SLIC supplies a balanced, sinewave, square or trapezoidal ringing signal of up to 81 VPeak (85 V DC supply) to the subscriber line across a load of up to 5 REN. The PBL 38774/1 supplies programmable constant current to the subscriber loop, sourced from the talk battery. The On-Hook line voltage of 43 V to 56 V is derived from the battery. All battery switching is internal to the device and is automatic. To further reduce power consumption the automatic gain control for the ring signal (AGC-R) keeps the level always adjusted to the maximum, that can be sourced from the available battery.

The SLIC incorporates loop current, ground key and ring-trip detection functions. The PBL 38774/1 is compatible with loop start and ground start signalling. Two- to four-wire and four- to two-wire voice frequency (vf) signal conversion is accomplished by the SLIC in conjunction with a standard codec. The line terminating impedance and balance impedance is programmable and may be complex or real for worldwide compliance.

Longitudinal balance specifications and other device characteristics are in compliance with Telcordia (Bellcore) and ITU-T requirements.

Tip and ring voltages are UL-1950 compliant; i.e. no two-wire line voltage exceeds 56 V. The PBL 38774/1 SLIC is packaged in a surface mount 28-pin SOIC or 32-pin MLP (32-pin VQFN) package.

1.4 Block Diagram

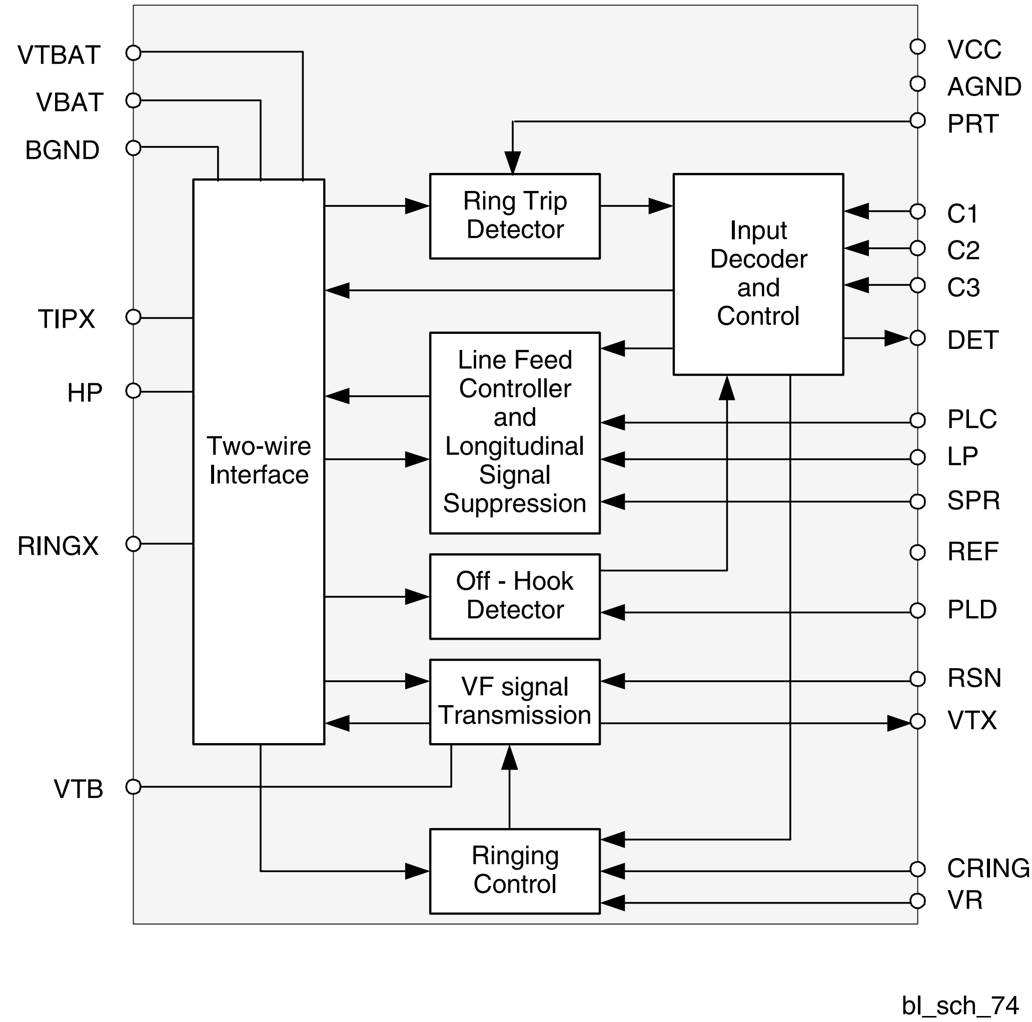


Figure 1 Block Diagram

2 Pin Configuration

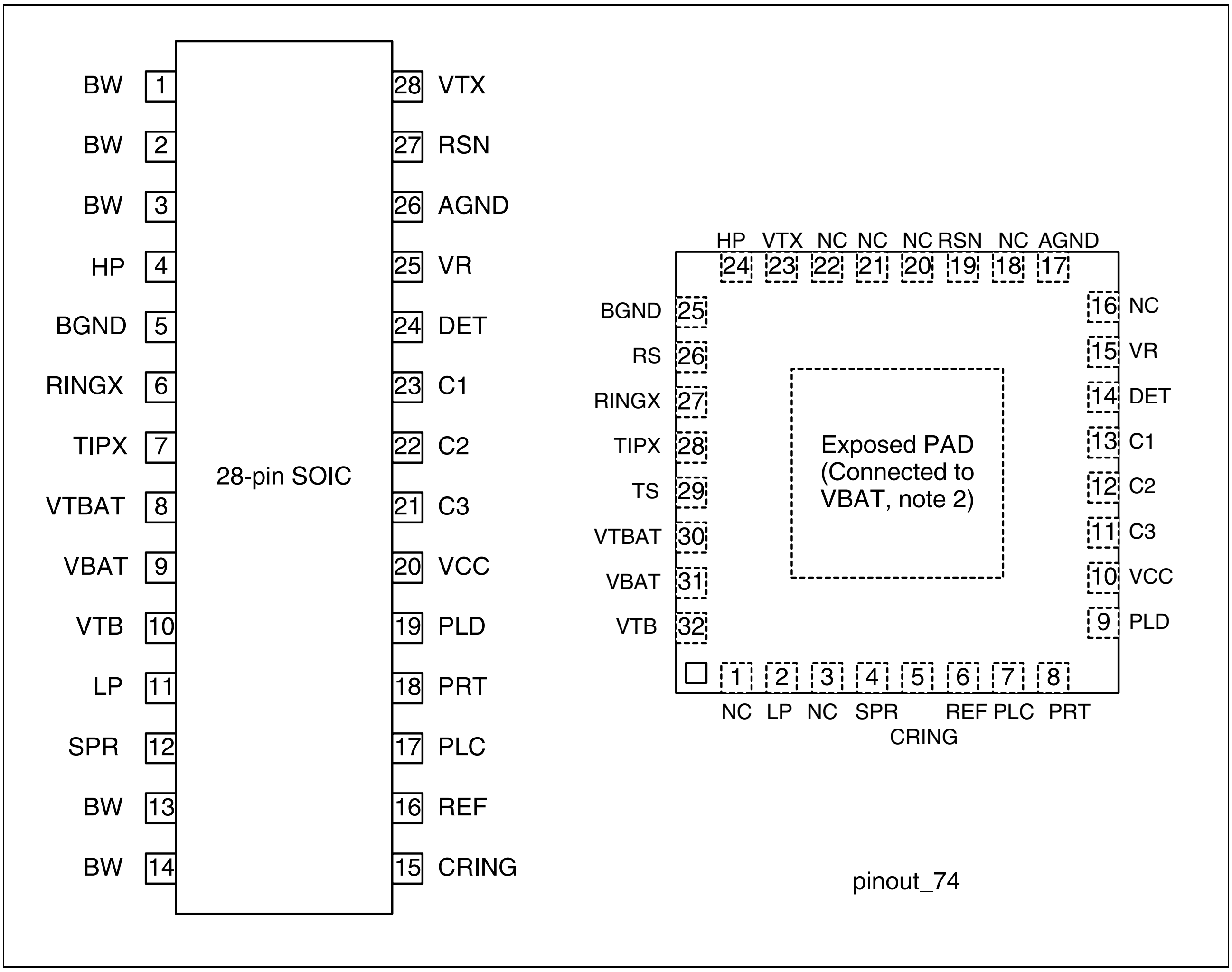


Figure 2 Pin Configuration 28L-SOIC (top view) **and 32L-MLP** (top view).

Table 1 Pin Definition and Functions

SOIC Pin No.	MLP Pin No.	Name	I/O	Function
1,2,3,13,14	-	BW	-	Batwing[1)]
4	24	HP	I	High Pass AC/DC separation capacitor C_{HP} connects between this pin and TIPX.
5	25	BGND	I	Battery Ground. Shall be tied together with AGND.
6	27	RINGX	O	The RINGX pin connects to the ring lead of the two-wire interface via over voltage protection components.

Table 1 Pin Definition and Functions (cont'd)

SOIC Pin No.	MLP Pin No.	Name	I/O	Function
7	28	TIPX	O	The TIPX pin connects to the tip lead of the two-wire interface via over voltage protection components.
8	30	VTBAT	I	Talk Battery. The DC loop current is supplied to TIPX and RINGX from this battery voltage. Negative with respect to BGND.
9	31	VBAT	I	On-hook and Ringing Battery supply voltage. Negative with respect to BGND.
10	32	VTB	I	Internal SLIC bias voltage. Connected to the talk battery supply. Refer to the application diagram in **Figure 9**. May be connected to any voltage between -32 V and -10 V.
11	2	LP	I	Low Pass saturation guard filter capacitor C_{LP} connects between this pin and VTBAT to filter out noise and improve $PSRR$.
12	4	SPR	I	Silent Polarity Reversal. The capacitor C_{SPR} connects between this pin and AGND. Required when soft polarity reveral is necesary.
15	5	CRING	I	The capacitor C_{RING} connects between this pin and AGND. Required for the ring loop.
16	6	REF	I	A 15 kΩ resistor connected between this pin and AGND sets an internal SLIC reference current. The value must not be changed.
17	7	PLC	I	Programmable Line Current. The constant current DC feed is programmed by a resistor ,R_{LC} ,connected from this pin to AGND.
18	8	PRT	O	Programmable Ring-trip Resistor, R_{RT} ,connected between this pin and AGND. The capacitor, C_{RT} , together with resistor, R_{RT} , filters the ring-trip detector.
19	9	PLD	O	Programmable Loop detector threshold. The loop detection threshold is set by a resistor, R_{LD}, between this pin and AGND.
20	10	VCC	I	+5 V power supply.

Table 1 Pin Definition and Functions (cont'd)

SOIC Pin No.	MLP Pin No.	Name	I/O	Function
21	11	C3	I	C1, C2, C3 are digital inputs, which control the SLIC operating states. Refer to **Table 2** for details.
22	12	C2	I	
23	13	C1	I	
24	14	DET	O	Detector output. Active low when indicating loop or ring-trip detection, active high when indicating ground key detection.
25	15	VR	I	Low voltage ring signal input.
26	17	AGND	I	Analog Ground, shall be tied to BGND.
27	19	RSN	I	Receive Summing Node. 400 times the current flowing out of this pin equals the metallic (transversal) current flowing from RINGX to TIPX. Programming networks for two-wire impedance and receive gain connect to the receive summing node.
28	23	VTX	O	Transmit vf output. The AC voltage difference between TIPX and RINGX, the AC metallic voltage, is reproduced at VTX with a gain of 0.5. The two-wire impedance programming network connects between VTX and RSN.
-	26	RS	I	RINGX Sense connects to RINGX with a short lead.
-	29	TS	I	TIPX Sense connects to TIPX with a short lead
-	1,3,16,18, 20,21,22, 26,29	NC	-	Not Connected, must be left open.

1) A batwing is a package pin, which provides a low thermal resistance path to the silicon chip via the lead frame. By soldering the batwing pins to PCB copper foil the device can be efficiently cooled. Note that batwing pins are at the same voltage as the VBAT pin (substrate voltage).

2) Exposed pad should be connected to V_{BAT}, note that this is used for cooling the chip.

Table 2 SLIC Operating States

State	C3	C2	C1	SLIC Operating State	Active Detector (DET Response)
0	0	0	0	Open circuit	No active detector (DET is set high)
1	0	0	1	Ringing	Ring-trip detector (DET active low)
2	0	1	0	Active	Loop current detector (DET active low)
3	0	1	1	Active	Loop voltage measurement (DET pulse train)
4	1	0	0	TIPX open circuit, RINGX active	Loop detector, RINGX current (DET active low)
5	1	0	1	Active	Ground key detector and loop ground fault detector (DET active high)
6	1	1	0	Active, reverse polarity	Loop current detector (DET active low)
7	1	1	1	Active, reverse polarity	Ground key detector and loop ground fault detector (DET active high)

3 Electrical Characteristics

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Temperature, Humidity						
Storage temperature range	T_{Stg}	-55	–	+150	°C	–
Operating temperature range	T_{Amb}	-40	–	+110	°C	–
Operating junction temperature range[1]	T_J	-40	–	+140	°C	–
Power Supply (-40 °C ≤ T_{Amb} ≤ +85 °C)						
V_{CC} with respect to AGND	V_{CC}	-0.4	–	6.5	V	–
V_{TB} with respect to AGND	V_{TB}	V_{BAT}	–	0.4	V	–
V_{TBAT} with respect to AGND/BGND	V_{TBAT}	V_{BAT}	–	0.4	V	–
V_{BAT} with respect to BGND, continuous	V_{BAT}	-85	–	0.4	V	–
Power Dissipation						
Continuous power dissipation	P_D	–	–	1.5	W	T_{Amb} ≤ +85 °C
Peak power dissipation	P_{PD}	–	–	4	W	T_{Amb} = +85 °C, t < 100 ms, t_{Rep} > 1 s
Ground						
Voltage between AGND and BGND	V_G	-5	–	V_{CC}	V	–
Digital Inputs, Outputs (C1, C2, C3, DET)						
Input voltage	V_{ID}	-0.4	–	V_{CC}	V	–
Output voltage (DET not active)	V_{OD}	-0.4	–	V_{CC}	V	–
Output current (DET)	I_{OD}	–	–	30	mA	–
Ring Voltage, Input (V_R)						
Input voltage	V_R	-1.1	–	V_{CC}	V	–

Table 3 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
TIPX and RINGX Terminals (-40 °C $\leq T_{Amb} \leq$ +85 °C, V_{BAT} = -75 V)						
TIPX or RINGX current	I_{TIPX}, I_{RINGX}	-100	–	100	mA	–
TIPX or RINGX voltage, continuous (referenced to AGND)	V_{TA}, V_{RA}	V_{BAT}	–	2	V	–
TIPX or RINGX[2)]	V_{TA}, V_{RA}	V_{BAT} - 15	–	5	V	pulse < 10 ms, t_{Rep} > 10 s
TIPX or RINGX[2)]	V_{TA}, V_{RA}	V_{BAT} - 20	–	10	V	pulse < 1 µs, t_{Rep} > 10 s
TIP or RING[2)3)]	V_{TA}, V_{RA}	V_{BAT} - 25	–	15	V	pulse < 250 ns, t_{Rep} > 10 s
TIPX and RINGX Terminals (-40 °C $\leq T_{Amb} \leq$ +85 °C, V_{BAT} = -80 V)[4)]						
TIPX or RINGX current	I_{TIPX}, I_{RINGX}	-100	–	100	mA	–
TIPX or RINGX voltage, continuous (referenced to AGND)	V_{TA}, V_{RA}	V_{BAT}	–	2	V	–
TIPX or RINGX[2)]	V_{TA}, V_{RA}	V_{BAT} - 10	–	5	V	pulse < 10 ms, t_{Rep} > 10 s
TIPX or RINGX[2)]	V_{TA}, V_{RA}	V_{BAT} - 15	–	10	V	pulse < 1 µs, t_{Rep} > 10 s
TIP or RING[2)3)]	V_{TA}, V_{RA}	V_{BAT} - 15	–	15	V	pulse < 250 ns, t_{Rep} > 10 s

1) The circuit includes thermal protection. Operation above max. junction temperature may degrade device reliability.

2) With the diodes D_B and D_{TB} included, see **Figure 9**.

3) R_{F1} and R_{F2} > 20 Ω is also required. Pulse is supplied to RING and TIP outside R_{F1} and R_{F2}.

4) If the same duration is needed as in VBat = -75 V add a diode to the HP pin to VBat (Anode to VBat, Catode to HP pin).

Attention: ***Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.***
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 4 Operating Range

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Ambient temperature	T_{Amb}	-40	–	+85	°C	–
V_{CC} with respect to AGND	V_{CC}	4.75	–	5.25	V	–
V_{TB} with respect to A/BGND[1)]	V_{TB}	-32	–	-10	V	–
V_{BAT} with respect to BGND	V_{BAT}	-80	–	–	V	–

1) The voltage of V_{TB} sets the maximum line length, see **Figure 13**. The diode D_{TB} is required, see **Figure 9**.

Note: In the operating range, the functions given in the circuit description are fulfilled.

3.1 Characterictics

The specification is made with following setup: -40 °C ≤ T_{Amb} ≤ +85 °C, V_{CC} = +5 V ±5%, V_{TBAT} = -32 V to -10 V, V_{BAT} = -80 V, Z_L = 600 Ω, V_R = 0.81 Vpeak, R_{LC} = 18.7 kΩ, (I_L = 26.8 mA), R_{LD} = 49.9 kΩ, R_{F1} = R_{F2} = 0, R_{Ref} = 15.0 kΩ, R_{RT} = 62.4 kΩ, C_{HP} = 33 nF, C_{LP} = 0.47 µF, R_T = 120 kΩ, R_{RX} = 120 kΩ, R_{VR} = 200 kΩ, C_{VR} = 0.47 µF;
Current definition: current is positive if flowing into a pin unless stated otherwise.

Table 5 Characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Two-Wire Port						
Overload level[1], see **Figure 3**, Active	V_{TRO}	1.0	–	–	VPeak	Off-Hook, I_{LDC} ≥ 10 mA, 1% THD
		1.0	–	–	VPeak	On-Hook, I_{LDC} ≤ 5 mA
		–	0.7	–	VPeak	Metering, I_{LDC} ≥ 10 mA, Z_{LM} = 200 Ω, f = 16 kHz
Input impedance[2]	Z_{TRX}	–	Z_T/ 200	–	Ω	–
Longitudinal impedance	Z_{LOT}, Z_{LOR}	–	20	35	Ω/wire	0 < f < 100 Hz
Longitudinal current limit	I_{LOT}, I_{LOR}	28	–	–	mA_{rms}/ wire	Active
Longitudinal to metallic balance (Active),(IEEE standard 455-1985), Z_{TRX} = 736 Ω	B_{LM}	58	70	–	dB	0.2 kHz ≤ f ≤ 1.0 kHz
		54	70	–	dB	1.0 kHz < f < 3.4 kHz
Longitudinal to metallic balance (Active), B_{LME} = 20 × log(E_{LO}/V_{TR}), see **Figure 4**	B_{LME}	58	70	–	dB	0.2 kHz ≤ f ≤ 1.0 kHz
		54	70	–	dB	1.0 kHz < f < 3.4 kHz

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Longitudinal to four-wire balance (Active), $B_{LFE} = 20 \times \log(E_{LO}/V_{TX})$, see **Figure 4**	B_{LFE}	58	76	–	dB	0.2 kHz $\leq f \leq$ 1.0 kHz
		54	76	–	dB	1.0 kHz $< f <$ 3.4 kHz
Metallic to longitudinal balance (Active), $B_{MLE} = 20 \times \log(V_{TR}/V_{LO})$, E_{RX} = 0 V, see **Figure 5**	B_{MLE}	40	58	–	dB	0.2 kHz $< f <$ 3.4 kHz
Four-wire to longitudinal balance (Active), $B_{FLE} = 20 \times \log(E_{RX}/V_{LO})$, see **Figure 5**	B_{FLE}	40	58	–	dB	0.2 kHz $< f <$ 3.4 kHz
Two-wire return loss[3)] $r = 20 \times \log\frac{\lvert Z_{TRX} + Z_L \rvert}{\lvert Z_{TRX} - Z_L \rvert}$	r	25	–	–	dB	0.2 kHz $< f <$ 0.5 kHz
		27	–	–	dB	0.5 kHz $< f <$ 1.0 kHz
		23	–	–	dB	1.0 kHz $< f <$ 3.4 kHz
TIPX idle voltage	V_{TI}	–	-0.9	–	V	Active, $I_L = 0$
RINGX idle voltage	V_{RI}	–	-51	–	V	Active, $I_L = 0$
Open loop voltage	$\lvert V_{TR\,Open} \rvert$	43	50	56	V	Active, $I_L = 0$
Four-Wire Transmit Port (V_{TX})						
Overload level[4)], see **Figure 6**	V_{TXO}	0.5	–	–	VPeak	Off-Hook, $I_L \geq$ 10 mA, Load imp. > 20 kΩ 1% THD
		0.5	–	–	VPeak	On-Hook, $I_L \leq$ 5 mA, Load imp. > 20 kΩ,
Output offset voltage	V_{TX}	-100	–	100	mV	–
Output impedance	Z_{TX}	–	5	20	Ω	0.2 kHz $< f <$ 3.4 kHz

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Four-Wire Receive Port (receive summing node = RSN)						
RSN DC offset voltage	V_{RSNdc}	-25	–	25	mV	I_{RSN} = 0 mA
RSN impedance		–	10	50	Ω	0.2 kHz < f < 3.4 kHz
RSN current to metallic loop current I_L gain, α_{RSN}	I_{RSN}	–	400	–	ratio	0.3 kHz < f < 3.4 kHz
Frequency Response						
Two-wire to four-wire, relative to 0 dBm, 1.0 kHz, E_{RX} = 0 V, see **Figure 7**	G_{2-4}	-0.15	–	0.15	dB	0.3 kHz < f < 3.4 kHz
		-0.5	-0.1	0.1	dB	f = 8 kHz, 12 kHz, 16 kHz
Four-wire to two-wire, relative to 0 dBm, 1.0 kHz, E_{LO} = 0 V, see **Figure 7**	G_{4-2}	-0.15	–	0.15	dB	0.3 kHz < f < 3.4 kHz
		-1.0	-0.2	0	dB	f = 8 kHz, 12 kHz
		-1.0	-0.3	0	dB	f = 16 kHz
Four-wire to four-wire, relative to 0 dBm, 1.0 kHz, E_{LO} = 0 V, see **Figure 7**	G_{4-4}	-0.15	–	0.15	dB	0.3 kHz < f < 3.4 kHz
Insertion Loss						
Two-wire to four-wire[5], $G_{2-4} = 20 \times \log(V_{TX}/V_{TR})$, E_{RX} = 0 V, see **Figure 7**	G_{2-4}	-6.22	-6.02	-5.82	dB	0 dBm, 1.0 kHz
Four-wire to two-wire[5][6], $G_{4-2} = 20 \times \log(V_{TR}/V_{RX})$, E_L = 0 V, see **Figure 7**	G_{4-2}	-0.2	–	0.2	dB	0 dBm, 1.0 kHz
Gain Tracking						
Two-wire to four-wire[7], $R_{LDC} \leq 2$ kΩ, Ref. -10 dBm, 1.0 kHz, see **Figure 7**		-0.1	–	0.1	dB	-40 dBm to +3 dBm
		-0.2	–	0.2	dB	-55 dBm to -40 dBm

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Four-wire to two-wire[7], $R_{LDC} \leq 2$ kΩ, Ref. -10 dBm, 1.0 kHz, see **Figure 7**		-0.1	–	0.1	dB	-40 dBm to +3 dBm
		-0.2	–	0.2	dB	-55 dBm to -40 dBm
Noise						
Idle channel noise at two-wire port[8] (TIPX-RINGX)		–	7	12	dBrnC	C-message weighting
		–	-83	-78	dBmp	Psophometrical weighting
Harmonic Distortion						
Two-wire to four-wire, see **Figure 7**		–	–	-50	dB	0.3 kHz $< f <$ 3.4 kHz 0 dBm, 1.0 kHz test signal
Four-wire to two-wire		–	–	-50	dB	0.3 kHz $< f <$ 3.4 kHz 0 dBm, 1.0 kHz test signal
Battery Feed Characteristics						
Constant loop current	I_{LConst}	0.92× I_{LProg}	I_{LProg}	1.08× I_{LProg}	mA	18 mA $< I_{LProg} <$ 30 mA $R_{LC} = \frac{500}{I_{LProg}} - \frac{10.4 \times \ln(32 \times I_{LProg})}{I_{LProg}}$
Tip Open Circuit, (See Figure 8)						
Tip open circuit TIPX current	I_{Leak}		-100		µA	S = Closed $R_L = 600\ \Omega$
Tip open circuit RINGX current	I_{LRTO}		I_L		mA	$R_{LRTO} = 0$ $V_{BAT} = -80$ V
			19		mA	$R_{LRTO} = 2{,}5$ kΩ $V_{BAT} = -80$ V

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Tip open circuit RINGX Voltage	V_{RTO}		-48.5		V	$I_{LRTO} < 23$ mA
Tip Voltage (ground start)		-4	0		V	Active, S = Open Ring lead via 150 Ω to GND
Tip Voltage (ground start)		-6	0		V	Active, Tip lead to -48 V via 7 kΩ (S = Closed) Ring lead via 150 Ω to GND
Open circuit loop current		-100	0	100	µA	$R_L = 0\ \Omega$
Loop Current Detector						
Programmable threshold, $I_{LTh} = 500/R_{LD}$	I_{LTh}	$0.9 \times I_{LTh}$	I_{LTh}	$1.1 \times I_{LTh}$	mA	$I_{LTh} > 10$ mA
Ringing						
VR input impedance		50	–	–	MΩ	–
Input bias current VR		–	7	–	nA	–
VR input voltage	VR_{PK}	–	0.81	–	V_{Peak}	Ref to AGND
Ring injection suppression		–	100	–	dB	Active, $R_L = 600\ \Omega$
Ringing gain[9)]		–	94	–	ratio	V_R to two-wire
Ringing voltage total distortion[9)]		–	0.4	2	%	$R_L = 1.4$ kΩ, f_{VR}=25 Hz
Voltage offset between TIPX and RINGX[9)]		–	0	–	V	
Common mode voltage TIPX and RINGX		-0.4	0	0.4	V	Related to $V_{BAT}/2 + 0.65$
Ring-Trip Detector						
Ring-trip current threshold[10)]	I_{LRTh}	$0.88 \times I_{LRTh}$	I_{LRTh}	$1.12 \times I_{LRTh}$	mA	–

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Loop Voltage Measurement						
Frequency		–	f	–	Hz	$f = 900x10^3/(\lvert V_{TR}\rvert + 1)$
Ground Key Detector and Loop Ground Fault Detector						
Ground key detector threshold		9	15	19	mA	–
Digital Inputs (C1, C2, C3)						
Input low voltage	V_{IL}	0	–	0.5	V	–
Input high voltage	V_{IH}	2.5	–	V_{CC}	V	–
Input low current	$\lvert I_{IL}\rvert$	-200	–	–	µA	V_{IL} = 0.5 V
Input high current	$\lvert I_{IH}\rvert$	-100	–	–	µA	V_{IH} = 2.5 V
Detector Output (DET)						
Output low voltage	V_{OL}	–	0.1	0.6	V	I_{OL} = 1 mA
Internal pull-up resistor to V_{CC}		–	10	–	kΩ	–
Power Dissipation[11] (V_{BAT} -80 V, V_{BAT} = -24 V)						
Power Dissipation	P_1	–	16	–	mW	Open circuit
Power Dissipation	P_2	–	65	–	mW	Active, Longitudinal current 0 mA I_L = 0 mA
Power Dissipation	P_3	–	500	–	mW	Active, R_L = 300 Ω (Off-hook)
Power Dissipation	P_4	–	290	–	mW	Active, R_L = 600 Ω (Off-hook)
Power Dissipation	P_5	–	320	–	mW	Ringing, R_L = 7 kΩ (AC load ≈ 1REN), Sine wave, 20 Hz, max. amplitude

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Power Supply Currents (V_{BAT} = -80 V)						
V_{CC} current	I_{CC}	–	1.4	–	mA	Open circuit
V_{TBAT} current	I_{TBAT}	–	0	–	mA	Open circuit
V_{TB} current	I_{TB}	–	-0.13	–	mA	Open circuit
V_{BAT} current	I_{BAT}	–	-0.07	–	mA	Open circuit
V_{CC} current	I_{CC}	–	2.4	–	mA	Active, On-hook
V_{TBAT} current	I_{TBAT}	–	0	–	mA	Active, On-hook
V_{TB} current	I_{TB}	–	-0.2	–	mA	Active, On-hook
V_{BAT} current	I_{BAT}	–	-0.6	–	mA	Active, On-hook
V_{CC} current	I_{CC}	–	7.1	–	mA	Ringing, On-hook, No ring signal
V_{TBAT} current	I_{TBAT}	–	0	–	mA	Ringing, On-hook, No ring signal
V_{TB} current	I_{TB}	–	-1	–	mA	Ringing, On-hook, No ring signal
V_{BAT} current	I_{BAT}	–	-2.7	–	mA	Ringing, On-hook, No ring signal
Power Supply Rejection Ratios						
V_{CC} to 2-wire port		30	45	–	dB	Active, f = 1 kHz, V_n = 100 mV
V_{CC} to 4-wire port		36	51	–	dB	Active, f = 1 kHz, V_n = 100 mV
V_{TB} to 2-wire port		28.5	60	–	dB	Active, f = 1 kHz, V_n = 100 mV
V_{TB} to 4-wire port		34.5	66	–	dB	Active, f = 1 kHz, V_n = 100 mV
V_{BAT} to 2-wire port		40	60	–	dB	Active, f = 1 kHz, V_n = 100 mV
V_{BAT} to 4-wire port		46	66	–	dB	Active, f = 1 kHz, V_n = 100 mV

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Temperature Guard						
Junction threshold temperature	T_{JG}	–	155	–	°C	–
Thermal Resistance						
Junction to pin	Θ_{JP}	–	22	–	°C/W	SOIC package
Junction to ambient	Θ_{JA}	–	41.6	–	°C/W	SOIC package
Junction to pin	Θ_{JP}	–	3	–	°C/W	MLP package
Junction to ambient	Θ_{JA}	–	27	–	°C/W	MLP package

1) The overload level is automatically expanded to needed signal level, maximum 1.7 VPeak when the signal level is > 1.0 VPeak, and is specified at the two-wire port with the signal source at the four-wire receive port. For more information see **Chapter 5.11**.

2) The two-wire impedance is programmable by selection of external component values according to:
$Z_{TRX} = Z_T/(|G_{2-4S} \times \alpha_{RSN}|)$ where:
Z_{TRX} = impedance between the TIPX and RINGX terminals
Z_T = programming network between the VTX and RSN terminals
G_{2-4S} = transmit gain, nominally = 0.5
α_{RSN} = receive current gain, nominally 400 (current defined as positive flowing into the receive summing node, RSN, and when flowing from ring to tip). See **Chapter 5**.

3) Higher return loss values can be achieved by adding a reactive component to Z_T, the two-wire terminating impedance programming resistances, e.g. by dividing Z_T, into two equal halves and connecting capacitors from the common points to ground.

4) The overload level is automatically expanded as needed up to 1.25 VPeak (using the AOV function) when the signal level > 0.5 VPeak and is specified at the four-wire transmit port, (VTX) with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2-4S} = 0.5$.

5) Secondary protection resistors R_{F1} and R_{F2} impact the insertion loss (refer to **Chapter 5**). The specified insertion loss is for $R_{F1} = R_{F2} = 40\ \Omega$.

6) The specified insertion loss tolerance does not include errors caused by external components.

7) The level is specified at the four-wire receive port (E_{RX}, **Figure 7**) and referenced to a 600 Ω impedance level.

8) The two-wire idle noise is specified with the four-wire receive port grounded ($E_{RX} = 0$, **Figure 7**). The four-wire idle noise at V_{TX} is the two-wire value reduced by 6 dB and is specified with the two-wire port terminated in 600 Ω (R_L). The V_{TX} noise specification is referenced to a 600 Ω impedance level.

9) PBL 38774/1 contains an Automatic Gain Control Ringing (AGC-R) unit. This unit controls the Gain in the ringing loop to keep an undistorted ringing signal due to variation in V_{BAT}, V_R input signal amplitude and Voltage offset. For more information see **Chapter 7** further on.

10) See **Chapter 7.2** for information about this.

11)The V_{TBAT} voltage is optimized for R_L = 600 Ω, I_L = 26.8 mA, no metering signal, R_F = 40 and the current controlled battery switch. See **Chapter 6.4** for further information.

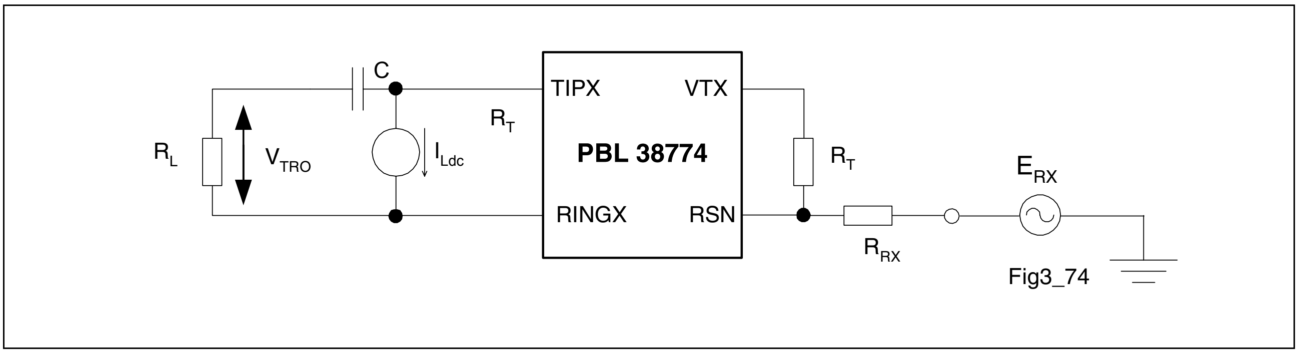


Figure 3 Overload Level, V_{TRO}, Two-Wire Port

$1/\omega C << R_L$, R_L = 600 Ω, R_T = 120 kΩ, R_{RX} = 120 kΩ

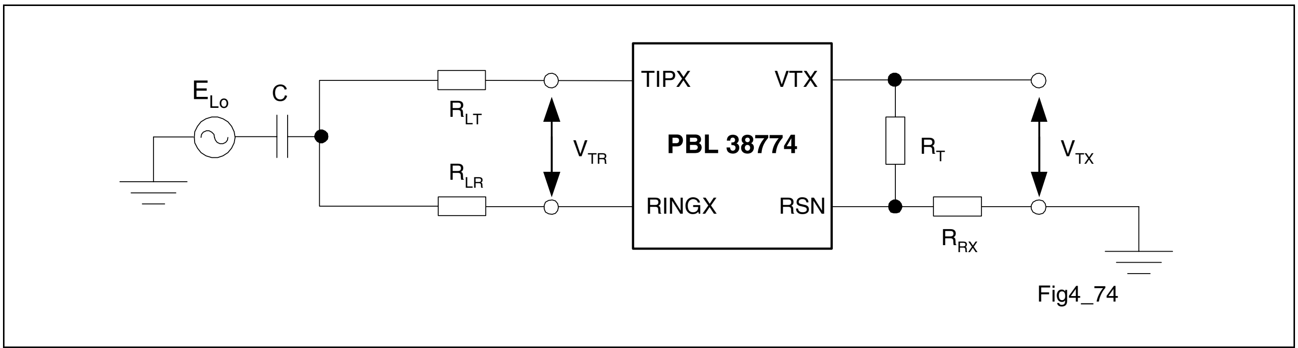


Figure 4 Longitudinal to Metallic, B_{LME} and Longitudinal to Four-Wire, B_{LFE} Balance

$1/\omega C << 150$ Ω, $R_{LT} = R_{LR}$ = 300 Ω or 368 Ω, R_T = 120 kΩ, R_{RX} = 120 kΩ

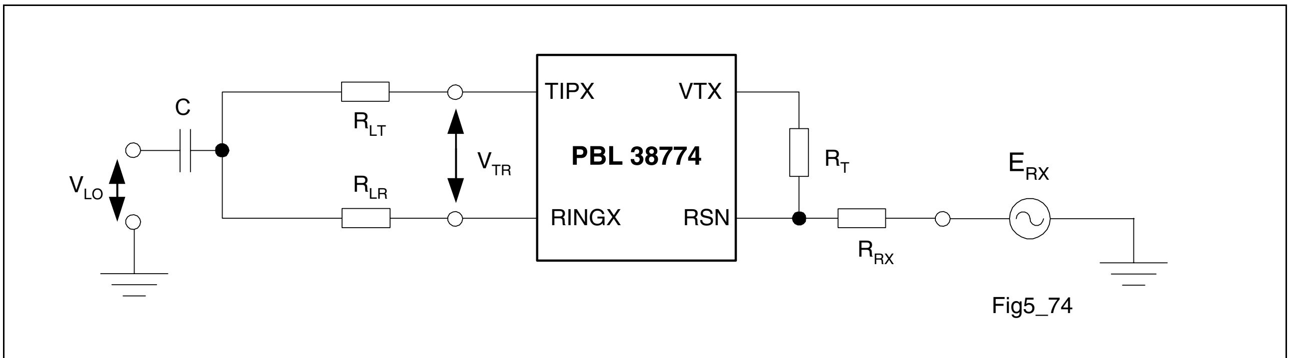


Figure 5 Metallic to Longitudinal, B_{MLE} and Four-Wire to Longitudinal Balance, B_{FLE}

$1/\omega C << 150$ Ω, $R_{LT} = R_{LR}$ = 300 Ω, R_T = 120 kΩ, R_{RX} = 120 kΩ

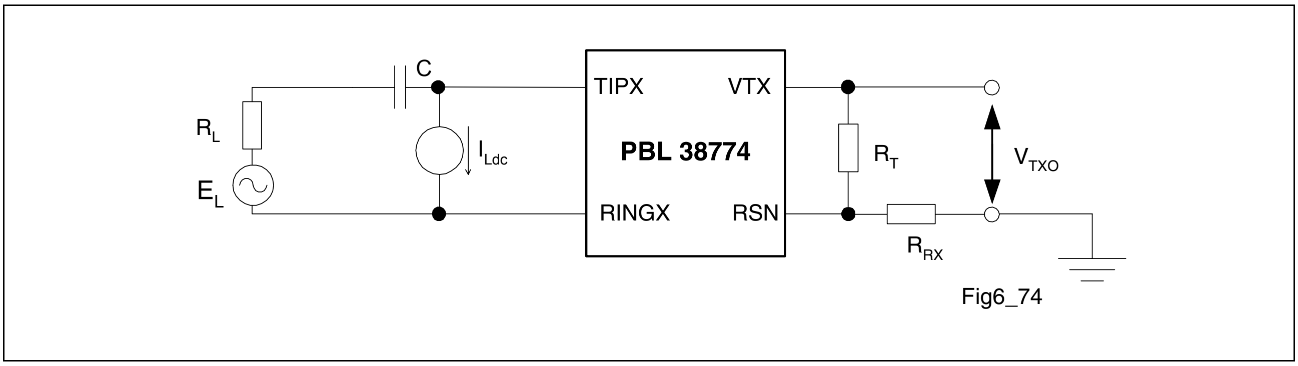


Figure 6 Overload Level, V_{TXO}, Four-Wire Transmit Port

$1/\omega C << R_L$, R_L = 600 Ω, R_T = 120 kΩ, R_{RX} = 120 kΩ

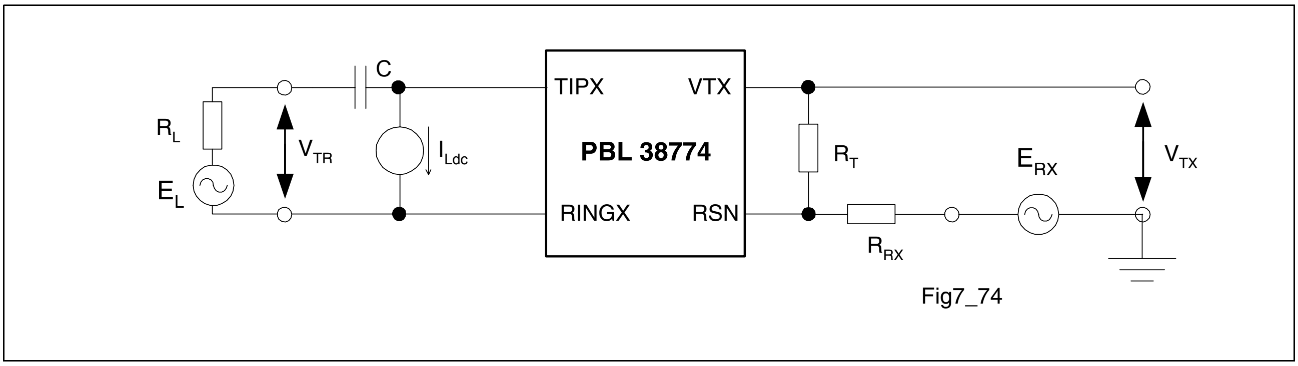


Figure 7 Frequency Response, Insertion Loss, Gain Tracking

$1/\omega C << R_L$, R_L = 600 Ω, R_T = 120 kΩ, R_{RX} = 120 kΩ

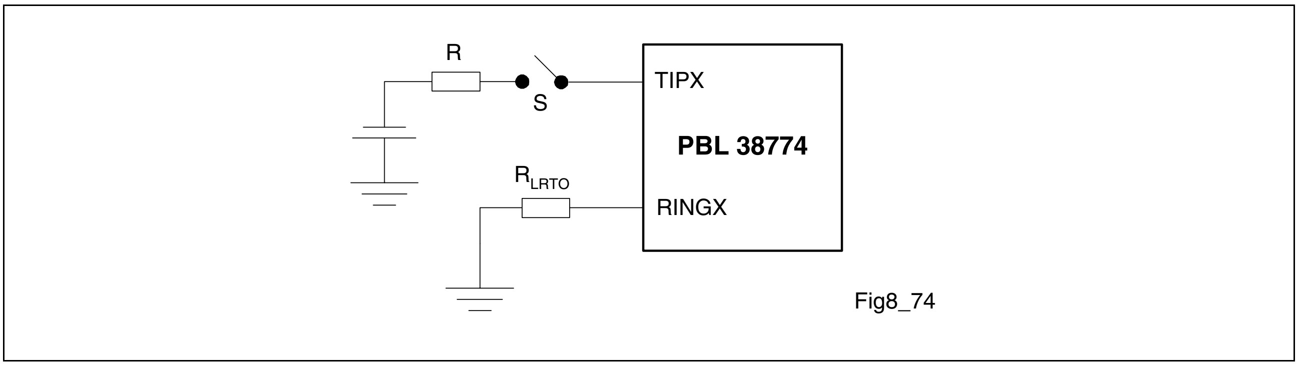


Figure 8 TIP Open Voltage

4 Functional Description and Applications Information

This chapter describes the Functional Description and Applications Information of the surrounding components.

4.1 Introduction

This SLIC is suitable in short loop power sensitive applications like, Cable modem, Voice over DSL, ISDN terminal adapter (NT1+), Voice over IP, Integrated Access Device (IAD), Residential Gateway or other short loop applications. The **Figure 9** shows the PBL 38774/1 in a typical application with a non-programmable, Combo I, codec. The SLIC can equally well be used with programmable codecs. The component values chosen for the application diagram example yield a two-wire impedance of 600 Ω, resistive. The balance resistor, R_T, is calculated for line impedance, Z_L (compromise impedance), of 600 Ω. The transmit gain is set by R_{TX} and R_{FB} (those resistors value are codec specific) to produce the digital mW level at the PCM transmit bus.

R_{F1}, R_{F2} , C_{GG} and the clamp “OVP” make up the overvoltage protection network.

Table 6 Functional Description

Component	Function
C_{TC} and C_{RC}	Clamp fast transients that may bypass the OVP clamp and also filter high frequency interference (RFI filter).
C_{HP} and C_{LP}	Are coupling capacitors within two SLIC feedback loops that control SLIC battery feed and SLIC voice frequency transmission.
C_{TB}, C_B, C_{VCC}	Are power supply bypass capacitors.
D_{TB}	Is a diode that is part of the battery switching function.
D_B	Prevents reverse currents from the V_B supply rail during application of negative over voltages.
D_{BB}	Is normally reverse biased, but conducts supply V_{TB} to the VBAT terminal in case the voltage V_B would fail.
R_T	Sets the two-wire impedance (note that R_T may be replaced with a complex impedance, Z_T, to implement complex terminating impedance).
R_{RX}	Sets the receive gain.
R_{LD}	Sets the loop current detector threshold.
R_{LC}	Sets the constant DC loop current.
R_{REF}	Sets a SLIC reference current (must be 15.0 kΩ, 1%, as specified).
R_{RT}	Sets the ring trip loop current detector threshold.

Table 6 Functional Description (cont'd)

Component	Function
C_{RING}	Is used for the high voltage ringing signal AGC (automatic gain control) function.
V_{TB}	Is the talk battery supply, i.e. the negative supply voltage that sources the loop current.
V_B	Is the ringing battery, i.e. the negative supply voltage that is used to power the SLIC, while ringing the line. This battery is also used to provide on-hook voltage.

4.2 Design Supporting Tools

The following supporting tools are available for the PBL 38774/1:

- Test board TB 215 SOIC
- Test board TB 215 MLP
- Pspice model PBL 38774/1

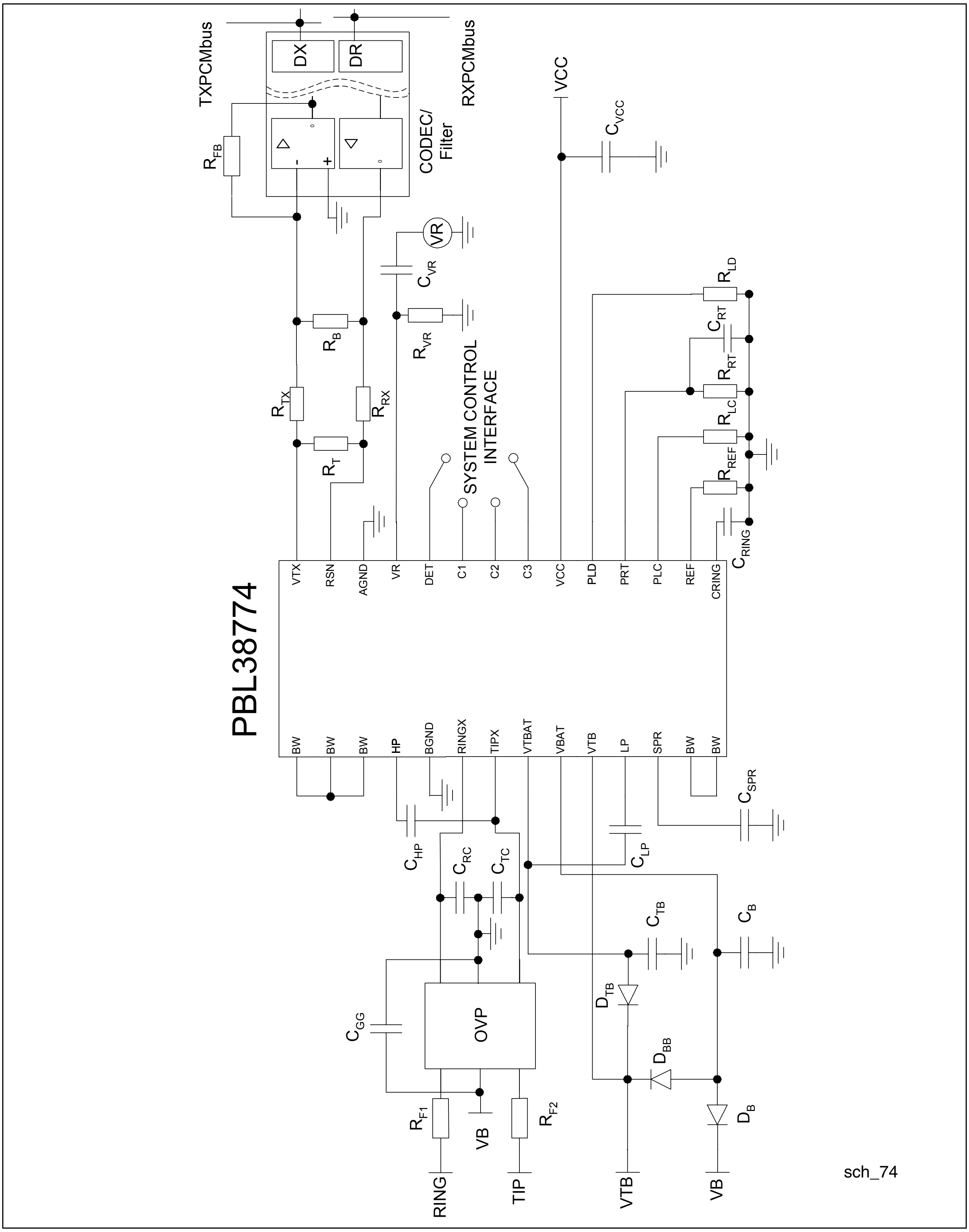


Figure 9 Application Example of PBL 38774/1 with a Combo/Codec

4.3 Recommended Components

Table 7 **Resistors** (values according to IEC-63 E96 series)

Resistor	Value	Tolerance	Specification
R_{LD}	49.9 kΩ	1%	1/10 W
R_{LC}	18.7 kΩ	1%	1/10 W
R_{RT}	69.6 kΩ	1%	1/10 W @ V_{BAT} = 80 V
R_{REF}	15 kΩ	1%	1/10 W
R_{T}	105 kΩ	1%	1/10 W (for 600 Ω two-wire impedance with the R_{F1} and R_{F2} included.)
R_{RX}	105 kΩ	1%	1/10 W (The gain is set to 1)
R_{VR}	200 kΩ	1%	1/10 W
R_{TX}	32.4 kΩ	1%	1/10 W
R_{B}	57.6 kΩ	1%	1/10 W
R_{FB}	depending on codec	–	–
$R_{F1} = R_{F2}$	Line protection resistor, 40 Ω 1% match, e.g. by Bourns	–	–

Table 8 **Capacitors** (values according to IEC-63 E6 series)

Capacitor	Value	Tolerance	Specification
C_{TB}	150 nF	20%	100 V
C_{B}	100 nF	20%	100 V
C_{HP}	33 nF	20%	100 V
C_{LP}	470 nF	20%	100 V
C_{GG}	220 nF	20%	100 V
C_{VCC}	100 nF	20%	10 V
C_{RING}	470 nF	20%	10 V
C_{RT}	10 nF/22 nF	20%	10 V (squarewave = 22 nF)
C_{VR}	470 nF	20%	10 V

Table 9 Optional Capacitors

Capacitor	Value	Tolerance	Specification
C_{TC}	1.0 nF	20%	100 V
C_{RC}	1.0 nF	20%	100 V
C_{SPR}	4 µF	20%	10 V

Table 10 Diodes

Diode	Value	Tolerance	Specification
D_{B}	1N4935		100 V
D_{TB}	1N4935		100 V
D_{BB}	1N4935		100 V

OVP

Secondary protection clamp Bourns (former Power Innovations) TISP PBL2, TISP PBL3 or TISP 6NTP2A, (which serves two lines).

The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferably to a ground plane.

5 Transmission

5.1 General

A simplified AC model of the transmission circuit is shown in **Figure 10**.

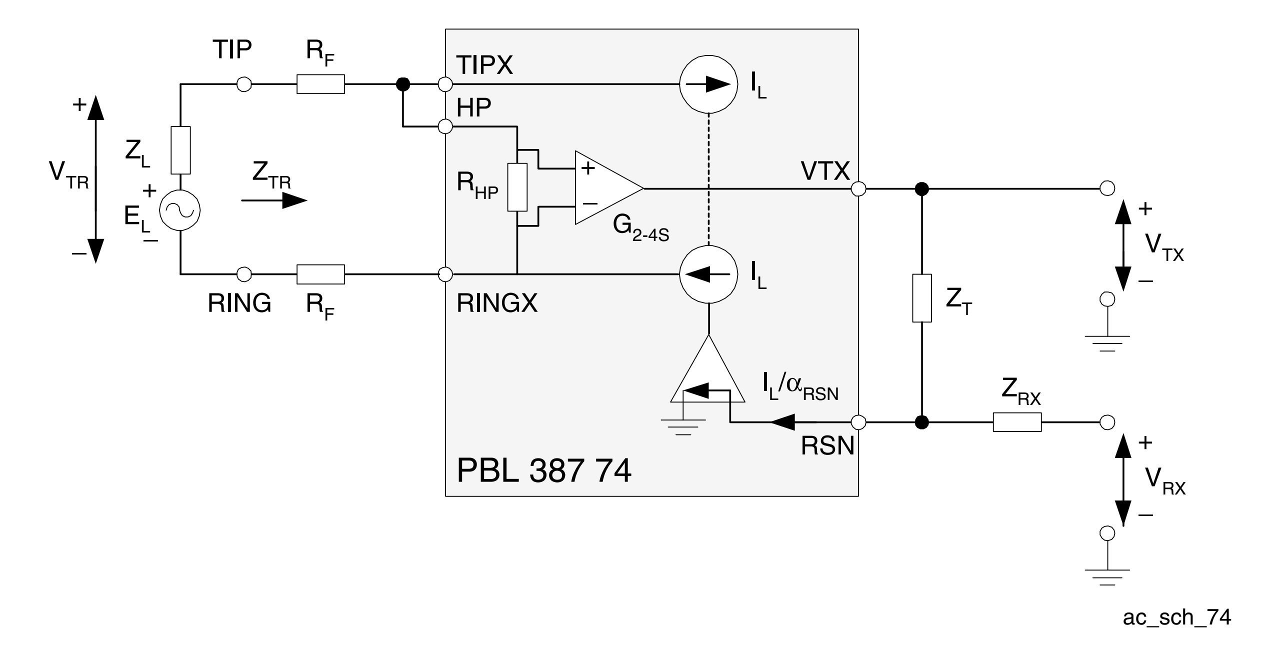


Figure 10 Simplified AC Model of PBL 38774/1

Circuit analysis from the Ac model in **Figure 10** yields following equations:

$$V_{TR} = \frac{V_{TX}}{G_{2-4S}} + I_L \times 2R_F \qquad [1]$$

$$\frac{I_L}{\alpha_{RSN}} = \frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} \qquad [2]$$

$$V_{TR} = E_L - I_L \times Z_L \qquad [3]$$

where:

V_{TX}	Is the ground referenced AC voltage at the VTX terminal.
V_{TR}	Is the AC metallic voltage between TIP and RING.
E_L	Is the line open circuit AC metallic voltage.

I_L	Is the AC metallic current.
R_F	Is a line over voltage protection resistor.
$G_{2\text{-}4S}$	Is the SLIC two-wire to four-wire gain (transmit direction) with a nominal value of 0.5.
Z_L	Is the total line impedance.
Z_{RX}	Controls four- to two-wire gain.
Z_T	Determines the SLIC TIPX to RINGX AC impedance for signals at voice frequencies.
V_{RX}	Is the analog ground referenced receive signal.
α_{RSN}	Is the receive summing node current to metallic loop current gain. $\alpha_{RSN} = 400$
R_{HP}	Internal resistor, approx. 400 kΩ, filters the AC signal together with C_{HP}

5.2 Two-Wire Impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the line protection resistors R_F, let $V_{RX} = 0$.

From **Equation [1]** and **Equation [2]**:

$$Z_{TR} = \frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F \qquad [4]$$

Thus with Z_{TR}, $G_{2\text{-}4S}$, α_{RSN} and R_F known:

$$Z_T = \alpha_{RSN} \times G_{2-4S} \times (Z_{TR} - 2R_F) \qquad [5]$$

5.3 Two-Wire to Four-Wire Gain

From **Equation [1]** and **Equation [2]** with $V_{RX} = 0$:

$$G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T / \alpha_{RSN}}{\dfrac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F} \qquad [6]$$

5.4 Four-Wire to Two-Wire Gain

From **Equation [1]** to **Equation [3]** with $E_L = 0$:

$$G_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \times \frac{1}{G_{2-4S}} \times \frac{Z_L}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_I} \qquad [7]$$

For applications where

$$\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F = Z_L \qquad [8]$$

the expression for $G_{4\text{-}2}$ simplifies to:

$$G_{4-2} = -\frac{Z_T}{Z_{RX}} \times \frac{1}{2 \times G_{2-4S}} \qquad [9]$$

5.5 Four-Wire to Four-Wire Gain

From **Equation [1]** to **Equation [3]** with $E_L = 0$:

$$G_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \times \frac{Z_L + 2R_F}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_F} \qquad [10]$$

5.6 Hybrid Function

The PBL 38774/1 SLIC may be used together with either software programmable or non-programmable codec/filters. When used together with programmable codec/filters the system controller permits adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the transmit and receive gains may be adjusted under software control. Please, refer to applicable programmable codec/filter data sheets for design information.

The hybrid function can also be implemented utilizing the uncommitted amplifier in conventional non software programmable codec/filters. Please, refer to **Figure 11**. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination codec/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain, $G_{4\text{-}4}$, a voltage proportional to V_{RX} is returned to V_{TX}. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} = \frac{-V_{RX}}{Z_B} = 0 \quad (E_L = 0) \tag{11}$$

The four-wire to four-wire gain, G_{4-4}, includes the required phase shift and thus the balance network Z_B can be calculated from:

$$Z_B = -R_{TX} \times \frac{V_{RX}}{V_{TX}} = R_{TX} \times \frac{Z_{RX}}{Z_T} \times \frac{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R}{Z_L + 2R_F} \tag{12}$$

When selecting the R_{TX} resistance value, make sure the load resistance on the V_{TX} terminal is at least 20 kΩ, i.e.:

$$\left|\frac{Z_T \times R_{TX}}{Z_T + R_{TX}}\right| \geq 20\text{k}\Omega \tag{13}$$

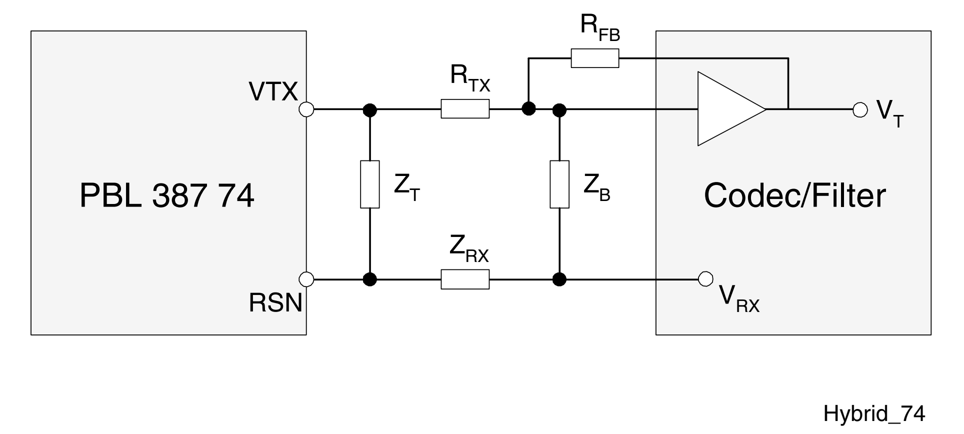


Figure 11 Hybrid Function

5.7 Longitudinal Impedance

A feedback loop within the SLIC counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range.

The SLIC longitudinal impedance per wire, Z_{LOT} and Z_{LOR}, appears as typically 20 Ω to longitudinal disturbances. It should be noted that longitudinal currents may exceed the DC loop current without disturbing the vf transmission.

5.8 Capacitors C_{TC} and C_{RC} (Optional)

The primary function of the capacitors C_{TC} and C_{RC} is as a part of the overvoltage protection network. The overvoltage protection clamp may not respond quickly enough to very fast transients and therefore damaging voltages may reach the SLIC pins TIPX and RINGX. C_{TC} and C_{RC} will protect the SLIC by shorting such fast transients to ground.

C_{TC} and C_{RC} may be utilized for RFI filtering when needed. C_{TC} and C_{RC} form RFI filters in conjunction with suitable series impedances (i.e. resistances, inductances). Resistors R_{F1} and R_{F2} may be sufficient, but series inductances can be added to form a second order filter. Current-compensated inductors (common mode chokes) are suitable since they impose little metallic impedance but high longitudinal impedance, therefore having minimum influence on two-wire transmission. Recommended values for C_{TC} and C_{RC} are 1 nF or less. Lower values implies less influence on the return loss and less degradation of the longitudinal balance caused by missmatching between C_{TC} and C_{RC}. On the other hand with lower values of C_{TC} and C_{RC} will decrease the attenuation of longitudinal induced radio frequencies. The influence of these capacitors on the two-wire terminating impedance must be considered when selecting a value for $C_{TC} = C_{RC}$. C_{TC} and C_{RC} contribute to a metallic impedance of $1/(2\pi \times f \times C_{TC}) = 1/(2\pi \times f \times C_{RC})$, a TIPX to ground impedance of $1/(2\pi \times f \times C_{TC})$ and a RINGX to ground impedance of $1/(2\pi \times f \times C_{RC})$.

5.9 AC - DC Separation Capacitor, C_{HP}

The high pass filter capacitor connected between terminals HP and TIPX provides the separation of the AC and DC signals, such that only AC signals are forwarded to the VTX terminal. C_{HP} positions the low end frequency response break point of the AC feedback loop in the SLIC. The C_{HP} value of 33 nF will position the low end frequency response 3 dB break point of the AC loop at 12 Hz (f_{3dB}) according to $f_{3dB} = 1/(2\pi \times R_{HP} \times C_{HP})$ where R_{HP} = 400 kΩ.

5.10 Capacitor C_{LP}

The capacitor C_{LP}, which connects between the terminals LP and VTBAT, positions the high end frequency break point of the low pass filter in the DC feedback loop (battery feed controlling loop) of the SLIC. Both C_{LP} and C_{HP} influence the two-wire impedance at low frequencies (primarily below the vf band) by adding an impedance in parallel with the programmed two-wire impedance (set by R_T and/or the Z-filter in the codec). The SLIC SPICE model includes the effects of C_{LP} and C_{HP} on the vf transmission. The C_{LP}

value of 470 nF will position the high end frequency response 3 dB break point of the AC loop at 0.3 Hz (f_{3dB}).

5.11 Adaptive Overhead Voltage, AOV

The Adaptive Overhead Voltage feature minimizes the SLIC power dissipation by permitting the TIPX and RINGX DC voltages to operate very close to the supply rails. When the SLIC detects a condition where the AC signal on TIPX/RINGX is approaching the supply rail and therefore would become distorted, the SLIC adjusts the overhead voltage, such that the TIPX/RINGX DC bias is moved away from the rails and thereby yielding enough peak signal swing for the AC signal. High level signal conditions such as when voice and metering signals are transmitted simultaneously are therefore automatically accommodated for the duration of the high level signal condition. This AOV system provides the designer with a flexible solution for different system requirements and possible future changes regarding voice, metering and other signal levels. There is no DC overhead level that must be set to a fixed value on account of worst case predicted peak AC signal value. Overhead voltage is defined as the voltage between TIPX and RINGX or RINGX and VTB (depending on selected state or used battery). The PBL 38774/1 will behave as a SLIC with fixed overhead voltage for signals in the 0-20 kHz range and with an amplitude less than 1 V_{Peak}. For signal amplitudes between 1 V_{Peak} and 1.25 V_{Peak} the adaptive overhead function will expand the overhead voltage making it possible for the signal to propagate through the SLIC without distortion. The expansion of the overhead occurs instantaneously. When the signal amplitude decreases, the overhead returns to its initial value with a time constant of approximately one second.

During operation the influence of the adaptive overhead function will not effect the SLIC performance in the constant current region of operation. If, however, the SLIC is in the off-hook, constant voltage region of operation, then the influence of the adaptive headroom will be apparent as a slight decrease in line voltage (and hence line current) as the SLIC adjusts to accommodate the larger signal (e.g. voice + metering).

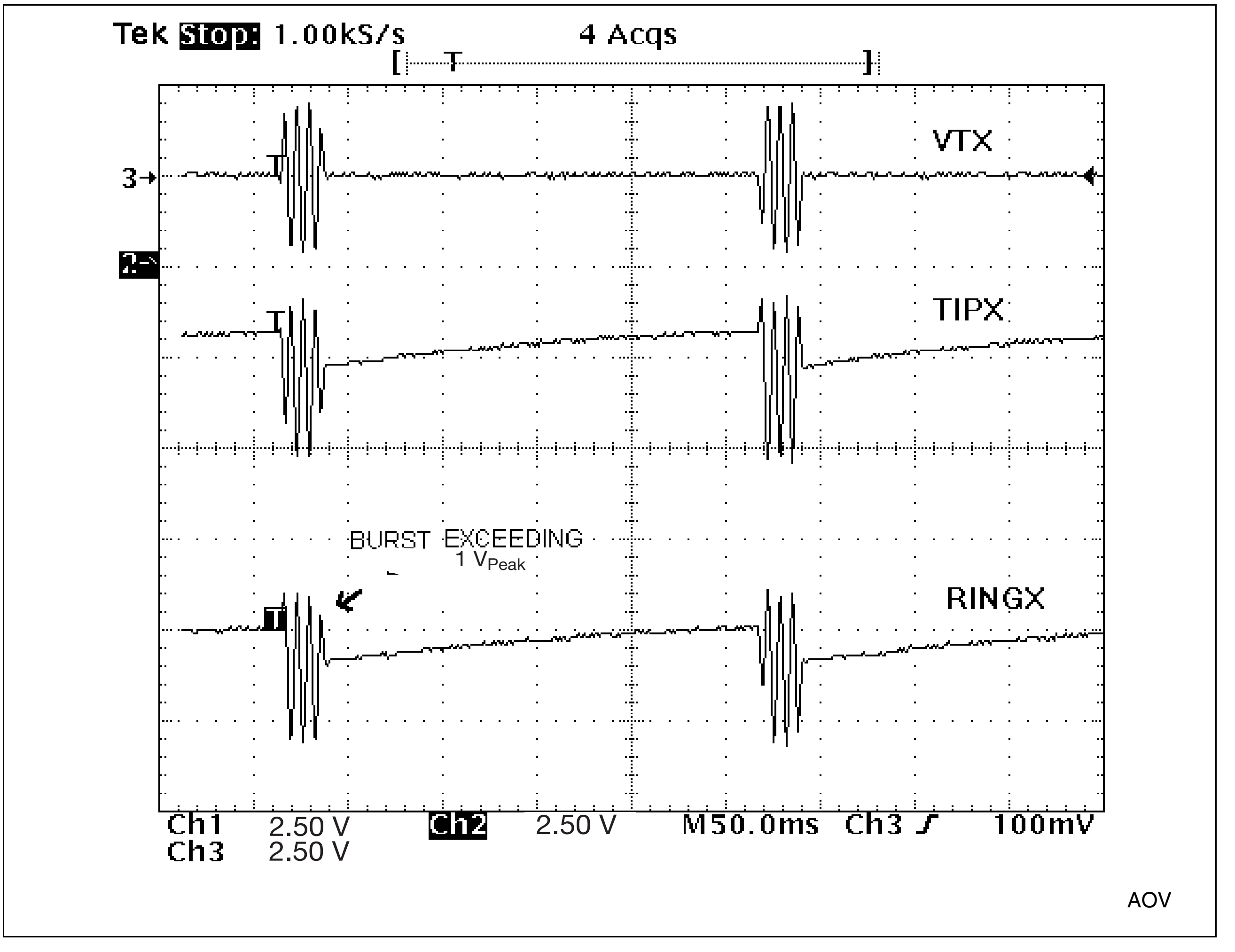


Figure 12 The AOV Function

Note: Observe that burst is undersampled.

5.12 Metering Applications

Subscriber Pulse Metering (SPM), also known as Advice-of-Charge signaling (AOC), is used in several European countries to provide the subscriber with an accurate indication of the cost of a call in progress. Pulses of an out-of-speechband signal are sent at the same time as the speech signal down the telephone line, the rate of the pulses indicating the cost of the call - faster pulse rates indicate a more expensive call. An electronic meter at the subscriber counts the pulses as they arrive and indicates the call cost on a digital display. This meter is normally wired in parallel with the telephone circuit and also provides filtering of the signal so that the subscriber at the telephone does not hear it.

There are two frequencies used for SPM signaling: 12 kHz and 16 kHz. The frequency used depends on the national requirements. The frequency of the SPM signal must be quite accurate, ±0.5% is typical. Furthermore the signal must be sinusoidal with < 5% total harmonic distortion. Pulse metering signals can be applied to the two-wire line via the PBL 38774/1 SLIC by connecting the pulse-metering source through coupling capacitor (C_{TTX}) and resistor (R_{TTX}) to the RSN node. The capacitor in series isolates the RSN input from any DC voltage that may be superimposed on the metering signal. The signal level of metering has to be included when optimizing talk battery V_{TB}. It is possible to mix speech and metering up to 1.7 V_{Peak} using the AOV function.

The metering signal gain can be calculated from the equation:

$$G_{4-2TTX} = \frac{V_{TRTTX}}{V_{RTTX}} = -\frac{Z_T}{Z_{TTX}} \times \frac{1}{G_{2-4S}} \times \frac{Z_{LTTX}}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_{LTTX} + 2R_F} \qquad [14]$$

where:

V_{TRTTX}	Is the desired metering voltage between the TIP and RING terminals.
V_{RTTX}	Is the metering voltage injected via the resistor R_{TTX}.
Z_{LTTX}	Is the line impedance seen by the 12 or 16 kHz metering signal, typically 200 Ω
Z_{TTX}	Sets the metering gain
$G_{2\text{-}4S}$	Is the transmit gain through the SLIC (0.5).

6 Battery Feed and Automatic Battery Switching

To reduce short loop power dissipation a second lower battery voltage, Off-hook or Talk battery, must be connected to the device via an external diode at terminal VTBAT. The SLIC automatically switches between the two battery supply voltages without need for external control. The silent battery switching to V_{BAT} occurs when the line current is below 5.5 mA. This means that the current in On-hook, V_{BAT}, battery is limited to 6 mA in the Active. The On-hook voltage is derived from V_{BAT} with the range of -43 V to -56 V at the TIPX and RINGX wires.

6.1 Constant Current Feed Region

See **Figure 13**, curve segment A-B-C.

For TIPX to RINGX voltages $V_{TR} < |V_{TB}|$ - 5.7 V, where:

V_{TR}	The tip to ring DC voltage
V_{TB}	The talk battery voltage
5.7 V	The voltage drop from $\|V_{TB}\|$ to the line voltage at point C in the graph of **Figure 13**, calculated according to: $0.7\text{ V} + 3.7\text{ V} + (27\text{ mA} \times 2 \times 25\ \Omega) \approx 5.7\text{ V}$

The PBL 38774/1 emulates constant current loop feed. The constant current value is adjustable between 18 mA and 30 mA by setting a value for resistor R_{LC}:

$$R_{LC} = \frac{500}{I_{LProg}} - \frac{10.4 \times \ln(32 \times I_{LProg})}{I_{LProg}} \qquad [15]$$

which may be approximated by

$$R_{LC} \approx \frac{500}{I_{LProg}} \qquad [16]$$

where:

I_{LProg}	Desired constant current in A
R_{LC}	Programming resistance in Ω
ln( )	Natural logarithm

6.2 Resistive Feed Region

See **Figure 13**, curve segment C-D-E.

For $V_{TR} > |V_{TB}|$ - 5.7 V the PBL 38774/1 emulates resistive loop feed with feed resistance equal to $2 \times 25\ \Omega$. The slope of the resistive feed region is made steep to extend the constant current region as close to the talk battery voltage (V_{TBAT}) as possible.

6.3 On-Hook Region

See **Figure 13**, curve segment E-G-H-J.

For loop currents I_L < 5.5 mA the PBL 38774/1 automatically switches to feed loop current from the ring battery, V_{BAT}. The switch from talk battery, V_{TBAT}, to ring battery, V_{BAT}, occurs without hysteresis at point E in **Figure 13**. For loop currents I_L within the on-hook range 0 mA < I_L < 5.0 mA (curve segment G-H-J) the line voltage remains nearly constant. This feature maintains a high on-hook voltage in the presence of DC line leakage currents or when a subscriber device consumes some current from the battery feed, e.g. to power displays. The On-hook voltage tracks the V_{BAT} voltage up to |54.5| V, $V_{TROpen} = |V_{BAT}|$ - 4.5 V. For V_{BAT} higher than |54.5| V the On-hook voltage is limited to |50| V typical.

In the presence of leakage currents I_{LLk} < 5 mA during on-hook: (**Figure 13**, curve segment G-H-J).

$V_{TROn\text{-}hook} = V_{TROpen} - I_{LLk} \times R_{Feed}$ where $R_{Feed} = 2 \times 25\ \Omega$

6.4 Optimizing V_{TB}

To optimize V_{TB} with actual load on the line:

$V_{TB} = (R_{LMax} + R_{FEED} + 2R_F) \times I_{LProg} + V_F + 3.7$, where:

R_{Lmax}	Is the maximum loop length including Off-hook phone load
R_{Feed}	$2 \times 25\ \Omega$
R_F	Is the resistance of one fuse resistor.
I_{LProg}	Is the programmed line current.
V_F	Is the forward voltage of D_{TB}. Normal value is 0.7 V.

Example: $R_{Lmax} = 600\ \Omega$, $R_F = 40\ \Omega$, I_{LProg} = 26.8 mA. This will give a V_{TB} of 24 V.

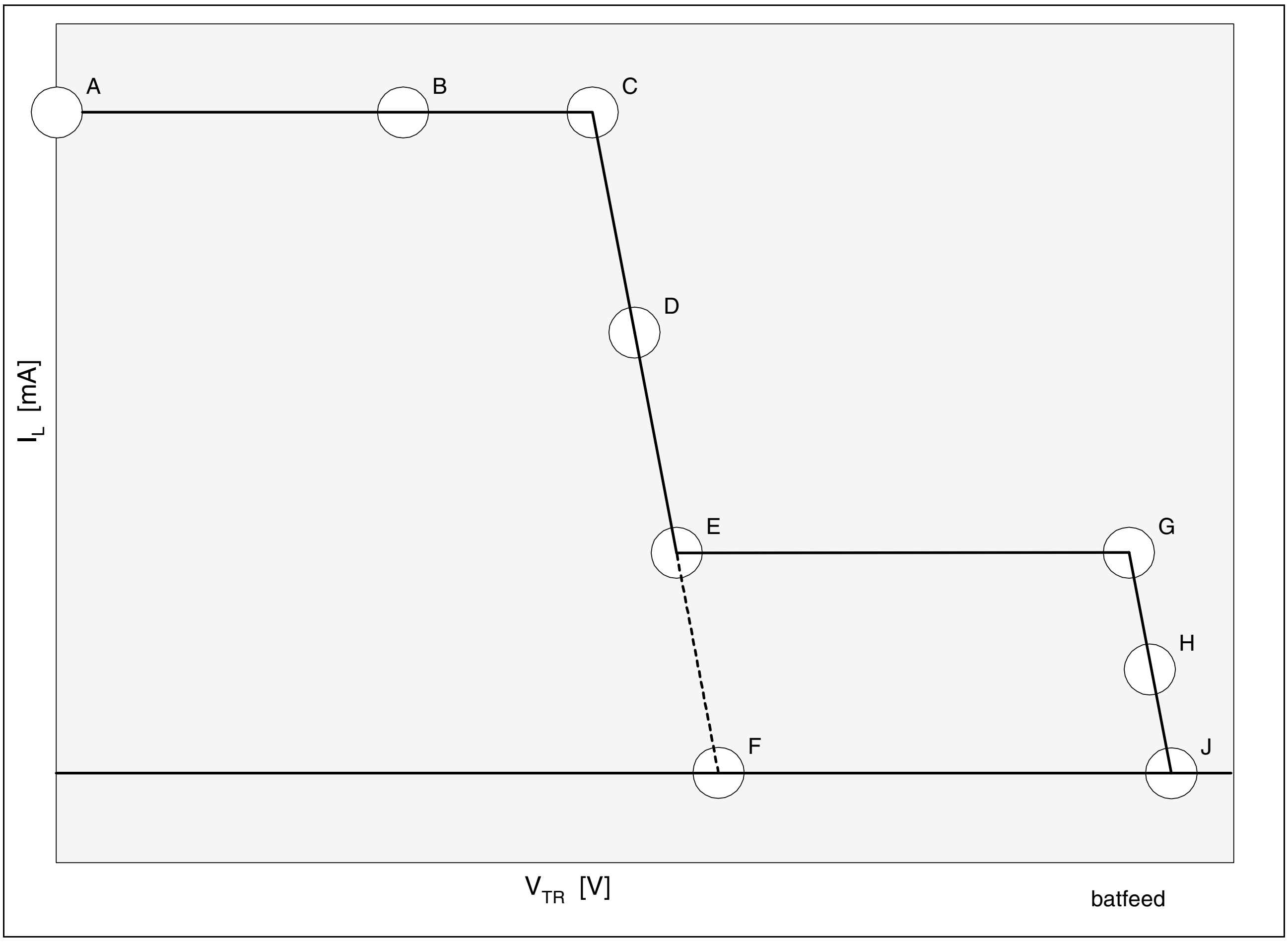


Figure 13 Battery Feed Characteristics

A	$I_L(@V_{TR} = 0) = I_{LConst} = I_{LProg}$ $R_{LC} = \frac{500}{I_{LProg}} - \frac{10.4 \times \ln(32 \times I_{LProg})}{I_{LProg}}$
B, C	$I_L = I_{LConst}$, $V_{TR}(@C) = V_{App} - R_{FEED} \times I_{LProg}$
D	$R_{FEED} = 2 \times 25\ \Omega$
E	$I_L \approx$ 5.5 mA, $V_{TR} = V_{App} - R_{FEED} \times 5.5$ mA
F	$V_{App}(@I_L = 0) = V_{TB} - V_F$[1] - 3.7 V
G	$I_L \approx$ 5 mA
H	$R_{FEED} = 2 \times 25\ \Omega$
J	The On-hook voltage tracks the V_{BAT} voltage up to: |54.5| V, $V_{TROpen} = \|V_{BAT}\|$ - 4.5 V, for V_{BAT} > |54.5| V, V_{TROpen} = 50 V

1) V_F is the forward voltage drop across diode D_{TB}.

6.5 Silent Polarity Reversal

With this feature it is possible to setup the time for TIPX and RINGX to reverse.

6.5.1 Polarity Reversal Time

The reversal time is set by the capacitor, C_{SPR}, connected between the pin SPR and AGND. The silent polarity reversal time is the same in both directions. To calculate the slient polarity reversal time use following formula;

$$t_r = C_{SPR} \times 9500 \quad [17]$$

6.5.2 Polarity Reversal Setup Time

The setup time is defined as the time changing the digital inputs to reversal until the reversal actually commences on TIPX and RINGX. The time is different in the two directions, Active to Reversal and Reversal to Active. The setup time is calculated from following expressions

Active to Reversal

$$t_{Act-Rev} = C_{SPR} \times 17500 \quad [18]$$

Reversal to Active

$$t_{Rev-Act} = C_{SPR} \times 15500 \quad [19]$$

7 Ringing Voltage

When designing PBL 38774/1 the object was to design a robust ringing SLIC that supports balanced ringing and that handles the high power dissipation and the different fault conditions that may occur when ringing. For power handling see **Chapter 8.1**.

Figure 14 shows a high level schematic of the ring loop.

The ring loop in the PBL 38774/1 is designed as a voltage amplifier. An internal feedback loop from the two-wire to the input sets a predetermined voltage gain. The voltage gain is adjusted to 94 by the AGC-R when ringing. The power amplifiers are of the current feed type that makes it possible to provide a reliable control of the ringing current. This arrangement makes it possible to add a control device, including an Automatic Gain Control unit, that provides protecting functions, such as:

- Automatic Gain Control-Ringing, AGC-R: If the amplifiers that supply TIPX and RINGX are forced to saturation due to i.e. variations of the V_{BAT} voltage or the V_{R} input signal level, the AGC-R will decrease the output signal. The shape of the output signal is kept undistorted. This function guarantees a low output impedance, approximately $2 \times 20\ \Omega$, and also allows variations in the input signal and the V_{BAT} voltage.
- Current limit: At off-hook or in fault conditions, i.e. TIPX and RINGX are shorted, the control device will limit the ringing current to approximately 10 mA above the programmed ring-trip threshold.
- Foreign voltage protection: The control device will detect if TIPX and/or RINGX are shorted to e.g. ground. The output voltage will be shut off to keep the power down. The detector output will be high.
- Temperature management: If the chip temperature exceeds 155 °C the control device will reduce the output voltage until the chip temperature equals 155 °C, and increase it again when the temperature drops. The detector output, DET, is forced to a logic low level when the temperature guard is active.

The VR pin is a high impedance input and has to have a resistor, R_{VR} = 200 kΩ, connected to ground, and a capacitor, C_{VR} = 470 nF, in series to decouple the DC component. The voltage V_{R} has a reference to AGND. The VR input handles any waveform, e.g. sinusoidal, trapezoid or square-wave shaped signals, since the SLIC acts like a linear amplifier. A DC-offset can be obtained by adding a DC part to the input signal. The capacitor C_{RING} forms a low pass filter that is an essential part of the control device. The control device is used to control e.g. the applied output voltage, the ringing current or the chip temperature. The resistor R_{RT} is a programming resistor that sets the ring-trip detector threshold. The current through the resistor is a rectified version of the line current divided by a factor. The capacitor C_{RT} filters the ring-trip detection device. PRT-pin is connected to the negative input of an OP-amplifier. The positive input is connected to a reference voltage. The output of the OP-amplifier is connected to the detector output DET. When the voltage over the resistor R_{RT} exceeds the reference voltage the detector output changes state.

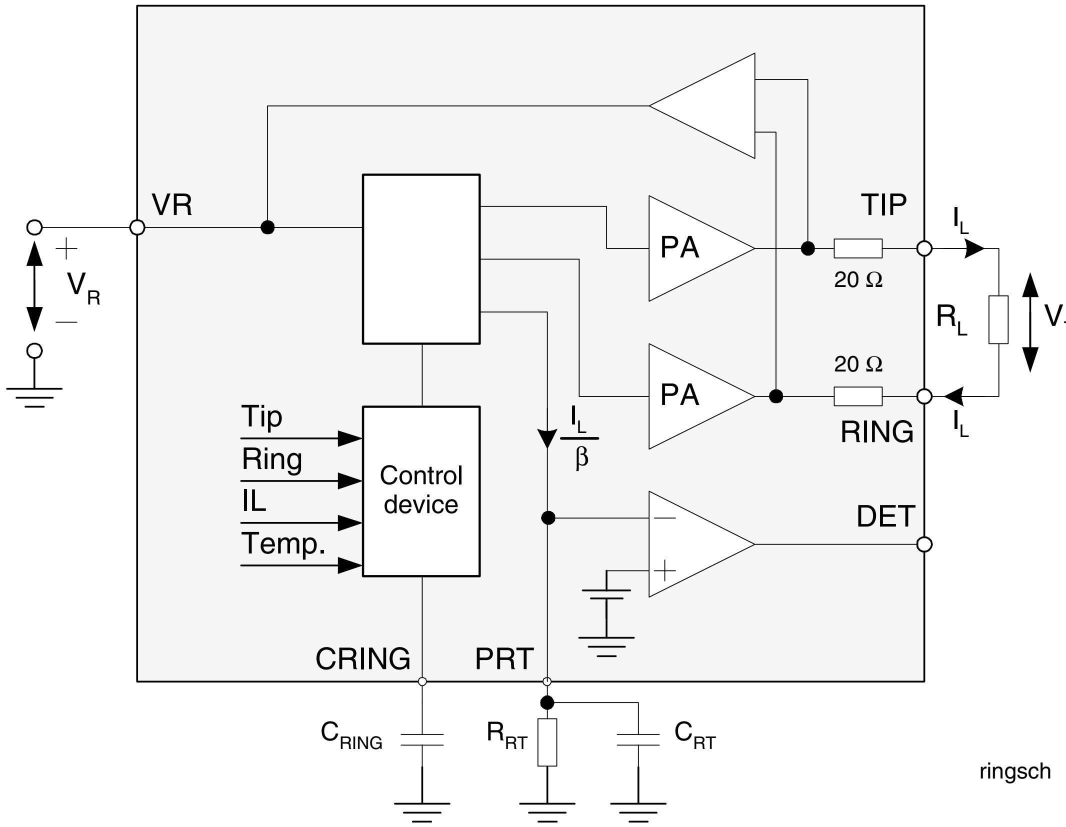


Figure 14 Ring Loop Schematic

The ring injection will be described in more detail in **Figure 15** and **Figure 16**. **Figure 15** shows a ring sequence with an off-hook at time t_1. The first diagram shows the voltage applied to the input, V_R, together with the voltages at TIPX and RINGX pins. The voltage of the TIP wire follows the voltage of the V_R pin. The second diagram shows the rectified current, I_L/β through the resistor R_{RT}. The dotted line represent the programmed ring-trip threshold, I_{LTH}/β The third diagram shows the voltage on the detector output. Before time t_1, the phone is on-hook. The ring voltage is applied symmetrically around a fixed voltage, $V_{BAT}/2$, to the load. As long as the telephone is on-hook the rectified current I_L/β will not exceed I_{LTH}/β. The DET output will be high. The control device will make sure that the voltage over the load is as high as possible without saturating the power amplifiers. When the telephone goes off-hook, at time t_1, the impedance of the load will decrease. The line current will increase and the control device will reduce the line current to a maximum of approximately 10 mA above the programmed ring-trip threshold, I_{LTH}. When the rectified current, I_L/β exceeds or equals to I_{LTH}/β the detector output, DET, will change to a logic low level, i.e. an off-hook. The voltage of the load will be reduced as a result of the control device limiting the line current. **Figure 16** illustrates ringing with a DC offset. This method is useful when trying to extend the ring-trip capability. When programming the ring-trip threshold there must be some margin so that no false ring-trip occurs when ringing at high REN. In on-hook the DC voltage will not have any affect on the load since there is no DC path, but when the telephone goes off-hook there will be a DC path and the extra voltage will give a high ring current. This arrangement makes it possible to set a higher ringtrip threshold value and thereby gives a larger margin between the ring current in on-hook, with low RENs, and the ring current in off-hook. To keep the same amplitude on the AC signal, as when ringing without DC offset, the battery has to be increased by the same value as the programmed DC offset. The signal to V_R-pin is supplied with a positive DC offset to AGND. The signal on the Tip-wire will be applied with a positive DC offset to the fixed voltage $V_{BAT}/2$. The signal on the Ring-wire will be applied with a negative DC offset.

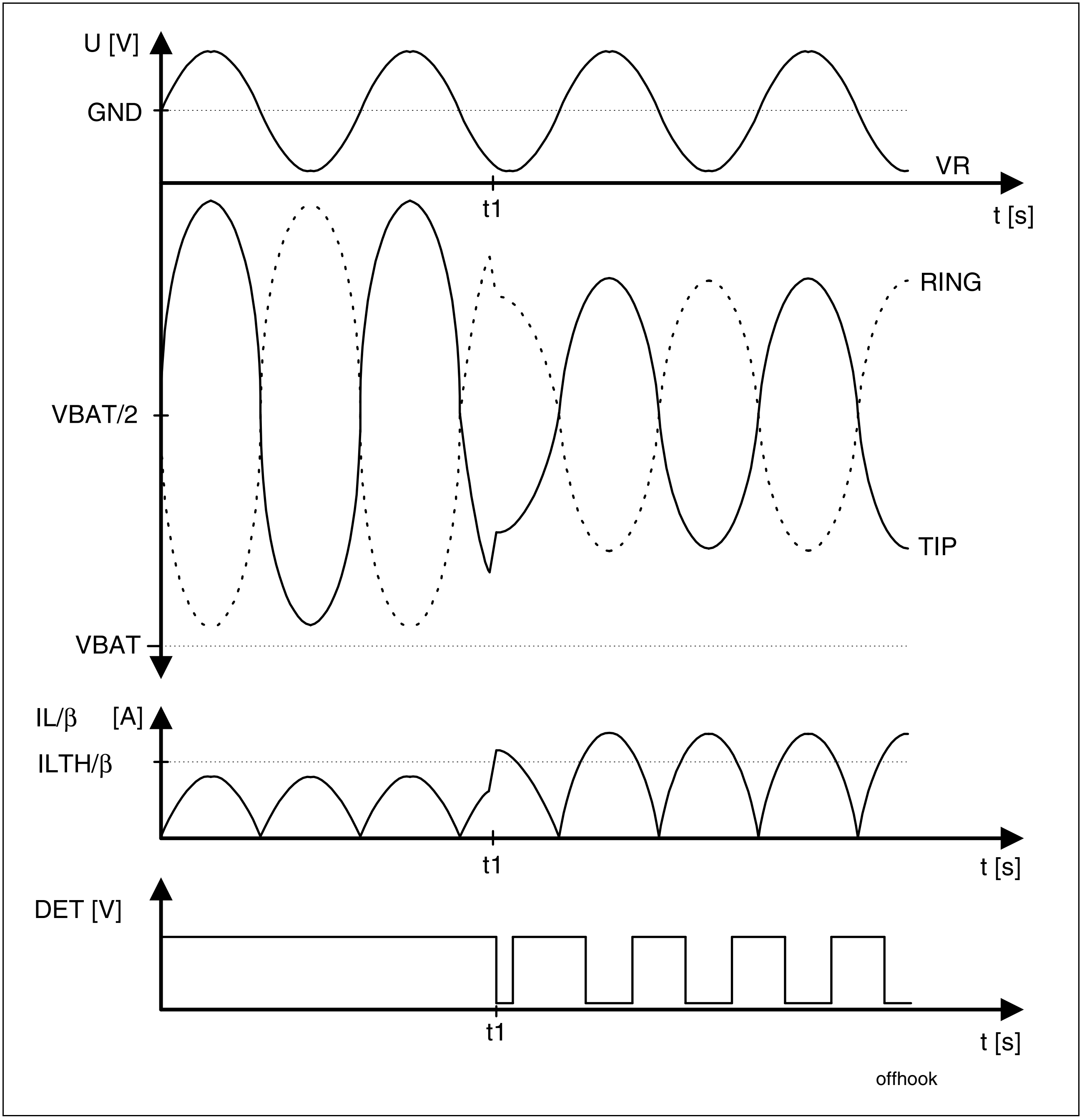


Figure 15 Off-Hook During Ringing

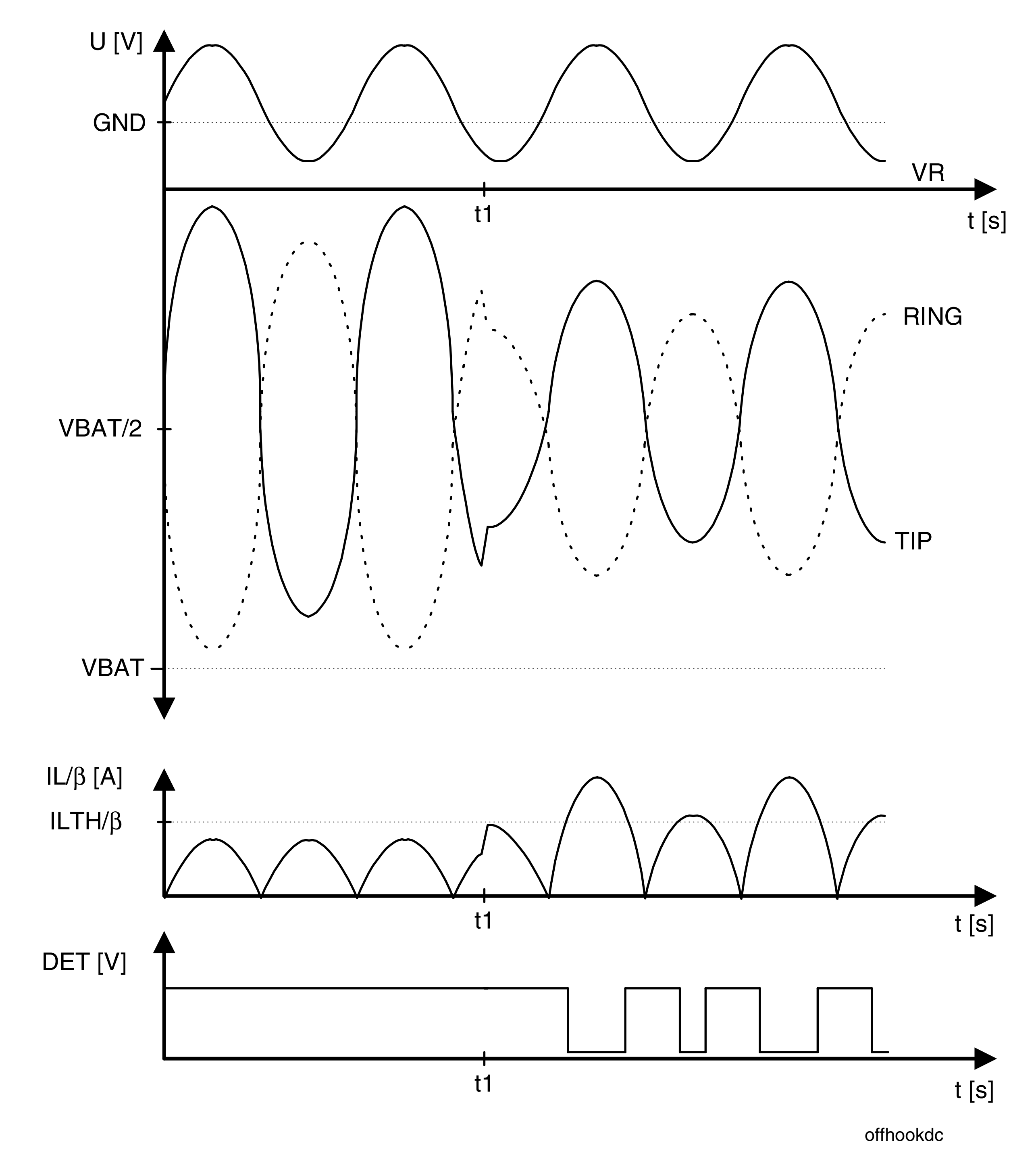


Figure 16 Off-Hook During Ringing with an Applied DC Offset

7.1 Calculation of the Input Signal

The VR input has to be connected to a signal generator or via impedance in all states. The following equations are valid for ring load between 0.25 and 5 REN. The optimal signal at VR pin is calculated as follows:

$$VR_{\mathrm{PK}} = \frac{|V_{\mathrm{BAT}}| - 3.5}{94.4} \qquad [20]$$

where:

VR_{PK}	Is the peak value at the VR pin.
V_{BAT}	Is the voltage of the VBAT pin.

Example: V_{BAT} = 80 V, this will give VR_{PK} = 0.81 Vpeak
With DC-offset:

$$VR_{\mathrm{DC}} = \frac{VR_{\mathrm{DCT-R}}}{103.8} \qquad [21]$$

$$VR_{\mathrm{PK+DC}} = \frac{|V_{\mathrm{BAT}}| - 3.5}{94.4} - VR_{\mathrm{DC}} \qquad [22]$$

where:

VR_{DC}	Is the positive DC offset in respect to GND at VR pin.
$VR_{\mathrm{DCT\text{-}R}}$	Is the DC voltage difference between the TIP and RING wires.
$VR_{\mathrm{PK+DC}}$	is the peak value of the AC-signal to be superimposed to the DC-voltage VR_{DC}

Example: V_{BAT} = -80 V, $VR_{\mathrm{DCT\text{-}R}}$ = 10 V
This will give: VR_{DC} = 0.096 V and $VR_{\mathrm{PK+DC}}$ = 0.714 Vpeak

7.2 Calculation of the Ring-Trip Threshold

The equations are only valid for sinusoidal waveforms with a frequency of 16-30 Hz applied to a REN load. It is important to take into account that when using other waveforms, frequencies or loads, peak line current can exceed the calculated $I_{\mathrm{LTHpeak.}}$. In these cases, replace the calculated $I_{\mathrm{LTHpeak.}}$, in the equations, with the actual peak line current. When using a square wave signal the C_{RT} should be increased to 22 nF. The ring-trip threshold is calculated according to the equation:

$$I_{\mathrm{LTHpeak}} = \frac{|V_{\mathrm{BAT}}| \times \alpha_{\mathrm{max}} - 3.5}{Z_{\mathrm{Bellmin}} + 40 + 2R_{\mathrm{F}} + R_{\mathrm{Lmin}}} \quad [23]$$

$$R_{\mathrm{RT}} = \frac{3480}{I_{\mathrm{LTHpeak}}} \quad [24]$$

With DC-offset:

$$I_{\mathrm{LTHpeak}} = \frac{|V_{\mathrm{BAT}}| \times \alpha_{\mathrm{max}} - 3.5 - VR_{DCT-R}}{Z_{\mathrm{Bellmin}} + 40 + 2R_{\mathrm{F}} + R_{\mathrm{Lmin}}} \quad [25]$$

$$R_{\mathrm{RT}} = \frac{3480}{I_{\mathrm{LTHpeak}}} \quad [26]$$

where:

$I_{\mathrm{LTHpeak.}}$	is the line peak current
40	Is the resistance of the SLICs internal resistors connected in series with output amplifiers (see **Figure 14**).
R_{RT}	Is the resistor value of the resistor connected between the PRT-pin and GND.
V_{BAT}	Is the voltage at the VBAT pin.
α_{Max}	Is the variation of the battery. 2% will give an $\alpha = 1.02$.
Z_{Bellmin}	Is the minimum resistance of the bell in on-hook. Typical 1400 Ω for 5 REN.
R_{F}	Is the resistance of one fuse resistor.
R_{Lmin}	Is the resistance of the minimum loop length.
$VR_{\mathrm{DCT\text{-}R}}$	Is the DC voltage difference between the Tip and Ring wire.

Example:

V_{BAT} = -80 V, Z_{Bellmin} = 1300 Ω, α_{Max} = 0%, R_{F} = 40 Ω, $VR_{\mathrm{DCT\text{-}R}}$ = 0, R_{Lmin} = 0 Ω, This will give: R_{RT} = 64.6 kΩ and a nominal Ring-trip current threshold I_{LRth} = 53.9 mA according to **Equation [27]**.

7.2.1 Nominal Ring-Trip Current

To calculate the nominal line ring-trip current use equation 27.

$$I_{\mathrm{LRth}} = \frac{4000}{R_{\mathrm{RT}}} \qquad [27]$$

8 Maximum Loop Length

The maximum loop length depends on three critical factors:

- Ringing voltage, waveform and number of RENs, **Chapter 8.1**
- Ring-trip current and number of RENs, **Chapter 8.2**
- The voltage of V_{TBAT} sets the Off-Hook Loop length, **Chapter 6.4**

8.1 Ringing Voltage, Waveform and Number of RENs

The SLIC is using the AGC-R feature. It is capable of producing high voltage over a large number of RENs together with minimum distortion when ringing at low number of RENs. Using a waveform with a lower crest factor,reducing the number of RENs or increasing the V_{TBAT} voltage will expand the loop length. The maximum loop length can be calculated using.

$$R_L = \frac{(|V_{BAT}| \times \alpha_{min} - 3.5\ ) \times Z_{Bell}}{V_{Bell} \times CF} - (Z_{Bell} + 40 + 2R_F) \qquad [28]$$

with DC-offset:

$$R_L = \frac{(|V_{BAT}| \times \alpha_{min} - 3.5 - VR_{DCT-R}) \times Z_{Bell}}{V_{Bell} \times CF} - (Z_{Bell} + 40 + 2R_F) \qquad [29]$$

where:

40	Is the resistance of the SLICs internal resistors connected in series with output amplifiers (see **Figure 14**).
V_{Bell}	Is the voltage, in VRMS, over the phone.
V_{BAT}	Is the voltage at the VBAT pin.
α_{min}	Is the variation of the battery. -2% will give an $\alpha = 0.98$.
Z_{Bell}	Is the resistance of the bell in on-hook. Typical 1400 Ω for 5 REN.
R_F	Is the resistance of one fuse resistor.
CF	Is the crestfactor. Use 1.41 for sinusoidal, 1.2 for trapezoidal and use 1 for squarewave.
VR_{DCT-R}	Is the DC voltage difference between the Tip and Ring wire.

Example:

V_{BAT} = -80 V, Z_{Bell} = 5 REN = 1400 Ω (1386 +40µF), α_{min} = 0%, R_F = 40 Ω, VR_{DCT-R} = 0, $CF = 1.41$, V_{Bell} = 40 V_{RMS}, This will give: R_L = 378 Ω

8.2 Ring-Trip Current and Number of RENs

The equations are only valid for sinusoidal waveforms with a frequency of 16-30 Hz applied to a REN load. It is important to take into account that when using other waveforms, frequencies or loads, peak line current can exceed the calculated $I_{LTHpeak.}$. In these cases, replace the calculated $I_{LTHpeak.}$, in the equations, with the actual peak line current. When using a square wave signal the C_{RT} should be increased to 22 nF. The programmable ring-trip current must be programmed to allow ringing on short lines, without false ring-trip on the specified number of RENs. At long loop, the off-hook current will be smaller than the programmed ring-trip current and no ring-trip is possible.This can be solved with a small DC-offset, but will instead decrease the ringing voltage in the example above. The value of the R_{RT} resistor and the maximum loop length for still detecting a ring-trip can be calculated using:

$$I_{\mathrm{LTHpeak}} = \frac{|V_{\mathrm{BAT}}| \times \alpha_{\mathrm{max}} - 3.5}{Z_{\mathrm{Bellmin}} + 40 + 2R_{\mathrm{F}} + R_{\mathrm{Lmin}}} \qquad [30]$$

$$R_{\mathrm{RT}} = \frac{3480}{I_{\mathrm{LTHpeak}}} \qquad [31]$$

$$R_{\mathrm{L}} = \frac{0,\ 66 \times (|V_{\mathrm{BAT}}| \times \alpha_{\mathrm{min}} - 3.5\ )}{I_{\mathrm{LTHpeak}}} - (R_{\mathrm{Offh}} + 40 + 2R_{\mathrm{F}}) \qquad [32]$$

With DC offset:

$$I_{\mathrm{LTHpeak}} = \frac{|V_{\mathrm{BAT}}| \times \alpha_{\mathrm{max}} - 3.5 - VR_{DCT-R}}{Z_{\mathrm{Bellmin}} + 40 + 2R_{\mathrm{F}} + R_{\mathrm{Lmin}}} \qquad [33]$$

$$R_{\mathrm{RT}} = \frac{3480}{I_{\mathrm{LTHpeak}}} \qquad [34]$$

$$R_{\mathrm{L}} = \frac{0,\ 66 \times (|V_{\mathrm{BAT}}| \times \alpha_{\mathrm{min}} - 3.5\ )}{I_{\mathrm{LTHpeak}}} - (R_{\mathrm{Offh}} + 40 + 2R_{\mathrm{F}}) \qquad [35]$$

Where:

$I_{\text{LTHpeak.}}$	is the line peak current
40	Is the resistance of the SLICs internal resistors connected in series with output amplifiers (see **Figure 14**).
R_{RT}	Is the resistor value of the resistor connected between the PRT-pin and GND.
V_{BAT}	Is the voltage at the VBAT pin.
$\alpha_{\text{min}}, \alpha_{\text{max}}$	Is the variation of the battery. 2% will give an α_{max} = 1.02 and -2% will give a α_{min} = 0.98.
Z_{Bellmin}	Is the minimum resistance of the bell in on-hook. Typical 1400 Ω for 5 REN.
R_{F}	Is the resistance of one fuse resistor.
R_{Lmin}	is the minimum resistance of the loop lenght
R_{Offh}	is the resistance of the phone in off hook, typical 400 Ω.
$VR_{\text{DCT-R}}$	Is the DC voltage difference between the Tip and Ring wire.
0.66	is the tolerance of the ringtrip detector with an included margin.

Example:

V_{BAT} = -80 V, Z_{Bellmin} = 5 REN = 1300 Ω, $\alpha_{\text{min}} = \alpha_{\text{max}}$= 0%, R_{Offh}= 400Ω, R_{F} = 40 Ω, $R_{LMIN} = 0$ $VR_{\text{DCT-R}}$ = 0, This will give: R_{L} = 417Ω.

9 Power Dissipation Considerations

9.1 Thermal Design Considerations

The thermal resistance, Θ_{Ja}, of the SLIC in a 28-pin SOIC package is 41.6 °C/W and the thermal resistance of 32-pin MLP package is 27 °C/W. The junction to ambient thermal resistance value, Θ_{Ja}, is extracted using the JEDEC standards and is representative of the natural airflow as seen in an application with a multilayer board. In this device the thermal resistance is lowered by using batwing pins, i.e. pins that are thermally and electrically shorted to the die. This also means that the potential of the batwing pins are the same as the substrate potential, i.e. the V_{BAT} potential. To reduce the thermal resistance in critical applications these batwing pins must be used. Typical demanding applications involves high ring voltages, high DC-offset, high REN numbers, high line currents together with high talk battery and used in high ambient temperatures. In these types of applications the batwing pins shall be soldered to a large metal layer using thermal conducting vias, i.e. small vias that will be filled with solder during the soldering process. The metal layer shall be of the order of 1sq inch and most effective is to use an outer layer, which can be cooled by convection. The PBL 38774/1 has a thermal shutdown protection at a typical temperature, T_{JG} of 155 °C, see **Chapter 12.1**.

There are three situations where high power dissipation occurs, see following chapters

- Ringing power dissipation on-hook, **Chapter 9.1.1**
- Ringing power dissipation off-hook, **Chapter 9.1.2**
- Off-hook power dissipation, **Chapter 9.1.3**

9.1.1 Ringing Power Dissipation On-Hook

The power dissipation can be calculated by the following formula:

$$P_{RNG} = P_R \times \frac{t_R}{t_R + t_A} + P_A \times \frac{t_A}{t_R + t_A} \qquad [36]$$

where:

P_{RNG}	Average power during ringing
P_R	Power dissipation in Ringing
P_A	Power dissipation in Active P2 in the specification typical 65 mW
t_R	Time in Ringing
t_A	Time in Active

Ringing, at two-wire, is normally applied with a defined ring cadence with burst and silent intervals where the SLIC is switched between the ring and active. Typically the time t_A is four times the time t_R. In some applications the time for the ringing and silent periods are equal, and the SLIC will dissipate more power.

The power dissipation in the SLIC for the burst can be calculated using (for a sinusoidal shaped ring signal):

$$P_R = P_S - P_L = \frac{2}{\pi} \times V_{BAT} \times \frac{V_{Ring}}{Z_{Loop}} - \frac{(V_{Ring})^2 \times \cos\Theta_L}{2Z_{Loop}} + P_{RingBias} \qquad [37]$$

where:

P_R	Power dissipation in Ringing
P_s	Supply power
P_L	The power in the Load
V_{BAT}	Potential at pin
V_{Ring}	Peak to peak voltage between tip and ring during ringing
$P_{RingBias}$	Power dissipation in Ringing without load, typical value 0.3 W
Z_{Loop}	Total line impedance, including fuse and the telephone impedance (in this case the on-hook resistance)

Z_{Loop} can be calculated using:

$$Z_{Loop} = \sqrt{(R_{Line} + R_{Bell} + 2R_F)^2 + \left(\frac{1}{2\pi \times f_{Ring} \times C_{Bell}}\right)^2} \qquad [38]$$

where:

R_{Line}	Line resistance, typical 0-500 Ω
R_{Bell}	Total bell resistance
R_F	Fuse and protection resistance, typical 40 Ω
f_{Ring}	Ring frequency
C_{Bell}	Total bell capacitance

$$\Theta_L = -\alpha\tan\left(\frac{1/\ (2\pi \times f_{Ring} \times C_{Bell})}{R_{CU} + R_{Bell} + 2R_F}\right) \qquad [39]$$

Example:

Calculate the SLIC power dissipation and junction temperature when V_{BAT} = -80 V, 5 REN, line resistance = 0 Ω, protection resistance = 2 × 40 Ω and ring cadence is 1:1. Ambient temperature is 85 °C.

Typical values in North America can be for 5 REN:
R_{Bell} = 1386 Ω, C_{Bell} = 40 µF, f_{Ring} = 20 Hz

$$Z_{Loop} = \sqrt{(0 + 1386 + 2 \times 40)^2 + \left(\frac{1}{2\pi \times 20 \times 40 \times 10^{-6}}\right)^2} = 1479\ \Omega$$

$V_{Ring} = V_{BAT}$ - 3.5 V = 76.5 V

The phase shift is very small so cos(Θ_L) is very near one and the formula above is simplified to:

$$P_R = \frac{2}{\pi} \times V_{BAT} \times \frac{V_{Ring}}{Z_{Loop}} - \frac{(V_{Ring})^2}{2Z_{Loop}} + P_{RingBias} = \frac{2}{\pi} \times 80 \times \frac{76.5}{1479} - \frac{76.5}{2958} + 0.3 \qquad [40]$$

P_R = 0.96 W

$$P_{RNG} = 0.96 \times \frac{1}{1+1} + 0.065 \times \frac{1}{1+1} = 0.51\ \text{W}$$

The Θ_{ja} = 41.6 °C/W and ambient temperature = 85 °C, T_j = 0.51 × 41.6 + 85 = 106.2 °C, which is less then the thermal protection at 155 °C.

9.1.2 Ringing Power Dissipation Off-Hook

Using the same formula as above and 300 Ω as the off-hook load the result will indicate several Watts of power dissipation. In that case the SLIC will limit the current to approx. 10 mA above the programmed ring-trip threshold, see **Chapter 7.2**. If the system do not force the SLIC into Active the temperature guard will be activated and the detector output, DET, will stay low.

9.1.3 Off-Hook Power Dissipation

The maximum off-hook power dissipation is dependent on the V_{TB} voltage, the line current I_L and the loop resistance R_{Loop}. The power dissipation in the SLIC can be calculated using:

$$P_{Off-hook} = P_S - P_L = V_{TB} \times I_L + P_q - (I_L)^2 \times R_{Loop} \quad [41]$$

where:

P_S	Supply power
P_L	The power in the Load
I_L	Programmed line current
P_q	Quiescent power, approx. 65 mW
R_{Loop}	The total line resistance, including fuse and the telephone impedance, in this case the off-hook resistance

Example:

Calculate the SLIC power dissipation and junction temperature when V_{TB} = -24 V, Programmed line current 27 mA, Off-hook resistance = 200 Ω, line resistance = 0 Ω, protection resistance = 2 × 40 Ω. Ambient temperature is 85 °C

$P_{Off\text{-}hook} = 24 \times 0.027 + 0.065 - (0.027)^2 \times (200 + 0 + 2 \times 40) = 0.51$ W

The junction temperature is calculated like the previous example.

10 Loop Monitoring Functions

The loop current, ground key and ring-trip detectors report their status through a common output, DET. The particular detector to be connected to the detector pin, DET, is selected via the three bit control interface C1, C2 and C3. Please refer to **Chapter 11** for a description of the control interface.

10.1 Detector Output (DET)

The SLIC incorporates a detector output driver designed as an open collector (npn), an internal 10 kΩ pull-up resistor to V_{CC}. The emitter of the drive transistor is connected to AGND. The logic high, 1, level is 5 V and the logic low, 0, is AGND.

10.2 Loop Current Detector

The loop current detector indicates that the telephone is off-hook and that DC current is flowing in the loop by setting the output pin DET to a logic low level when selected. The loop current detector threshold value, I_{LTh}, where the loop current detector changes state, is programmable with the R_{LD} resistor. R_{LD} connects between pin PLD and ground and is calculated according to:

$$R_{LD} = \frac{500}{I_{Lth}} \tag{42}$$

The loop current detector is internally filtered and is not influenced by the AC signal at the two-wire side. In the TIPX Open the DET output changes to logic low state when the RINGX current exceeds I_{LTh}.

10.3 Ground Key Detector, Loop Ground Fault Detector

The ground key detector circuit senses the difference between TIPX and RINGX currents. When triggered the output pin DET is set to a logic high level. The detector is triggered when the difference exceeds the internally set and fixed current threshold. Diagnostics: loop ground faults can be detected by the ground key detector.

10.4 Loop Voltage Measurement

The loop voltage, V_{TR} (V), is presented at the DET output as a pulse train with a repetition frequency, f_V (Hz), which is inversely proportional to the voltage according to:

$$f_V = \frac{900 \times 10^3}{|V_{TR}| + 1} \qquad [43]$$

The loop voltage measurement starts when commanding the SLIC into the loop voltage measurement state from any other state (refer to **Table 2**). Loop diagnostic purposes and setting line card gain are two examples of uses for the loop voltage information.

11 Control Inputs

The SLIC has three digital control inputs, C1, C2 and C3. A decoder in the SLIC interprets the control input condition and determining the commanded operating state. C1, C2 and C3 are internal pull-up inputs. The logic inputs are compatible with a 3.3 V logic interface.

11.1 Open Circuit (C3, C2, C1 = 0, 0, 0)

In the Open Circuit the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum and no detectors are active. DET output is set high.

11.2 Ringing (C3, C2, C1 = 0, 0, 1)

The low voltage ringing signal, which is connected to VR, is amplified and appears at TIPX and RINGX as a balanced high voltage ring signal. The ring-trip detector monitors hook status and sets the DET output low when off-hook line status is detected.

11.3 Active (C3, C2, C1 = 0, 1, 0)

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. The loop current detector is activated. The loop current detector indicates off-hook with a logic low level present at the detector output.

11.4 Active, Loop Voltage Measurement (C3, C2, C1 = 0, 1, 1)

A frequency inversely proportional to the line voltage will appear at the DET output when the SLIC is set to the active, loop voltage measurement state.

11.5 TIPX Open (C3, C2, C1 = 1, 0, 0)

In TIPX open the TIPX pin is set to present a high impedance, while the RINGX lead is active and able to sink current. The DET output monitors RINGX current level and changes to low when the RINGX current exceeds the threshold current set by resistor , R_{LD}. This operating state is used for interfaces wich require ground start signaling.

11.6 Active, Ground Key and Loop Ground Fault (C3, C2, C1 = 1, 0, 1)

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. The ground key detector is activated. The ground key detector will indicate active ground key with a logic high level present at the detector output. This state is also used for a diagnostic function as loop ground faults can be detected by the ground key detector.

11.7 Active Reversal, Loop Current Detector (C3, C2, C1 = 1, 1, 0)

TIPX and RINGX polarity is reversed compared to Active: RINGX is the terminal closest to ground and sources loop current while TIPX is the most negative terminal and sinks current. The loop detector will indicate off-hook with a logic low level present at the detector output.

11.8 Active Reversal, Ground Key and Loop Ground Fault (C3, C2, C1 = 1, 0, 1)

TIPX and RINGX polarity is reversed compared to Active: RINGX is the terminal closest to ground and sources loop current while TIPX is the most negative terminal and sinks current. The gound key detector is activated. The ground key detector will indicate active ground key with a logic high level present at the detector output. This state is also used for a diagnostic function as loop ground faults can be detected by the ground key detector.

12 Overtemperature and Overvoltage Protection

12.1 Analog Temperature Guard

The varying environmental conditions in which SLICs operate in conjunction with fault conditions may lead to the chip maximum temperature limitation being exceeded. The SLIC reduces the DC line current and the longitudinal current when the chip temperature reaches approximately 155 °C and increases the line current again automatically when the chip temperature drops. Due to the linear nature of the chip temperature regulation (e.g. DC loop current partially reduced) a talk path may still be functional while the temperature guard is active. The detector output, DET, is forced to a logic low level while the temperature guard is active.

12.2 Overvoltage Protection - General

The SLIC must be protected against foreign voltages on the telephone line. Overvoltages can result from lightning, AC power contact, induction and other causes. Refer to **Table 3**, TIPX and RINGX terminals, for maximum continuous and transient voltages that the SLIC TIPX and RINGX terminals can withstand. Overvoltage protection consists of primary protection located outside of the line card (e.g. gas tubes in a main distribution frame) and secondary protection (series line resistors and solid state clamping devices such as diodes and thyristors) located on the linecard printed circuit board.

12.3 Secondary Protection

The circuit shown in **Figure 9** utilizes series resistors (R_{F1}, R_{F2}) together with a programmable overvoltage protector (OVP, e.g. Power Innovations TISP PBL3 or TISP6NTP2AD) as secondary protection.

The TISP PBL3 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to the negative supply voltage (i.e. the battery voltage, V_{BAT}). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized. Positive overvoltages are clamped to ground by a diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage and the protector will crowbar into a low voltage on-state condition, by firing an internal thyristor.

A gate decoupling capacitor, C_{GG}, is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. C_{GG} should be placed close to the overvoltage protection device. Without the capacitor even the low inductance in the track to the V_{BAT} supply will limit the current and delay the activation of the thyristor clamp.

The line protection resistors R_{F1} and R_{F2} serve the dual purposes of being non-destructing energy dissipators when transients are clamped and of being fuses when the line is exposed to a power cross. If longitudinal balance requirements permit, PTC resistors may be used for R_{F1} and R_{F2}. Note, however, that it is important to use fixed resistors in series with PTCs since PTCs are capacitive. Fast transients will therefore experience much less PTC impedance than slower transients. Relying only on PTCs as the current limiting element could therefore result in excessive fast transient current through the clamp, with possible clamp current overload and resulting inability to protect the SLIC. A value of approximately 40 Ω for each of R_{F1} and R_{F2} limits the peak overvoltage transient current to a value that is compatible with the clamping device (OVP block in **Figure 9**) capability. Higher resistance values for R_{F1} and R_{F2} than 40 Ω will require more stringent matching of the R_{F1} and R_{F2} resistors and will also have a much greater impact on terminating impedance, gains and DC loop resistance. Lower resistance values for R_{F1} and R_{F2} than 40 Ω will result in peak clamp currents that may exceed the capability of standard clamping devices.

13 Power-Up Sequence

No special power-up sequence is necessary except that ground has to be present before all other power supply voltages. The digital inputs C1, C2 and C3 are internal pull-up terminals.

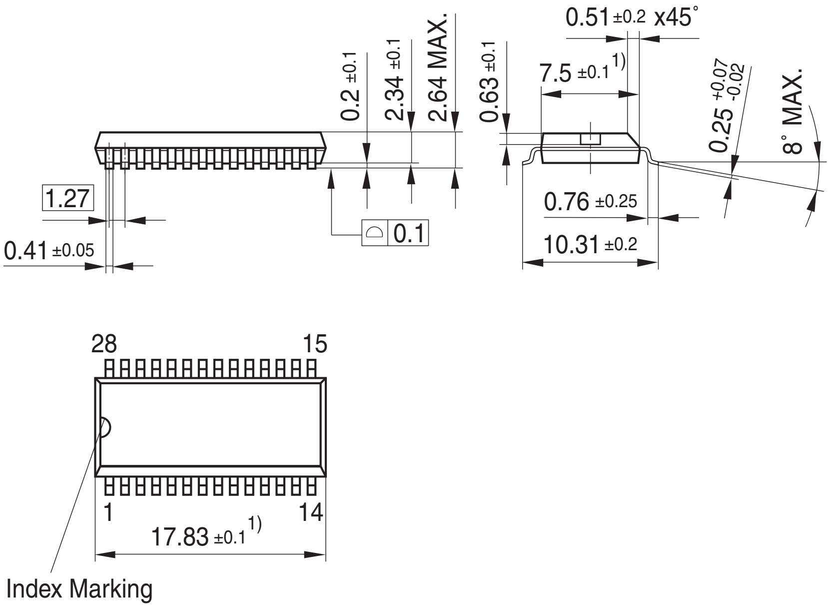
14 Printed Circuit Board Layout

Care in Printed Circuit Board (PCB) layout is essential for proper function. The components connection RSN input should be placed in close proximity to that pin, such that no interference is injected into the receive summing node (RSN). Ground plane surrounding the RSN pin is advisable. Analog Ground (AGND) should be connected to Battery Ground (BGND) near the SLIC package. R_{LC} and R_{REF} should be connected to AGND with short leads. Pin LP and HP are sensitive to leakage currents. The C_{LP} connection between pins LP and VTBAT should be as short as possible. C_B and C_{TB} must be connected near the pins VBAT and VTBAT with short vias to ground. The TS pin has to be connected to the TIPX pin with a short lead, ideal pins connected together. The RS pin has to be connected to the RINGX pin with a short lead, ideal pins connected together. The batwing pins, (SOIC) and exposed pad (MLP) are internally connected to VBAT and used for transferring the heat from the chip to the printed circuit board. It is therefore advisable to implement a PCB layout that facilitates heat conduction away from the batwing pins.

15 Package Outlines

The SLIC is provided in two different packages: 28-pin SOIC and 32-pin MLP.

15.1 28-Pin SOIC Package



1) Does not include mold protrusion of 0.25 max. per side

GPS09521

Figure 17 **P-DSO-28-20** (Plastic Dual Small Outline Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

15.2 32-pin MLP Package

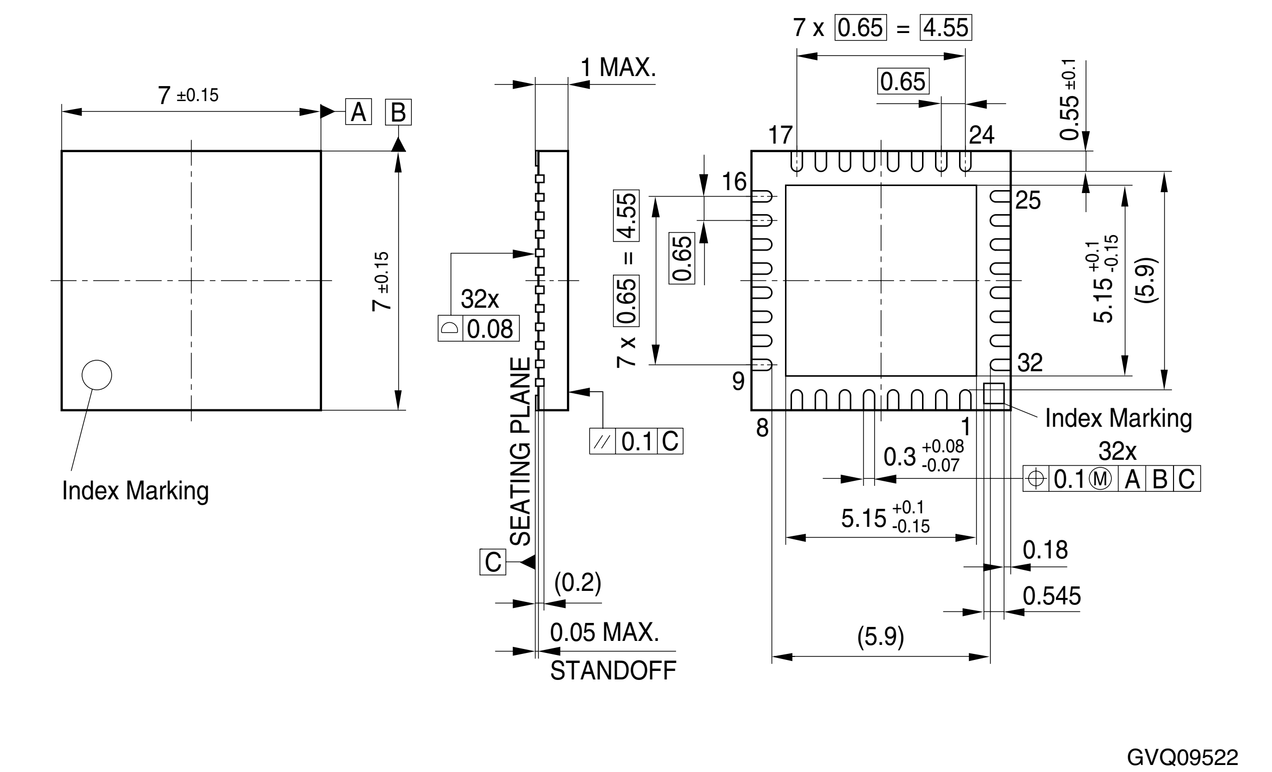


Figure 18 **P-VQFN-32-6** (Plastic Very Thin Profile Quad Flat Non Leaded)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

http://www.infineon.com

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