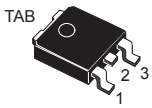
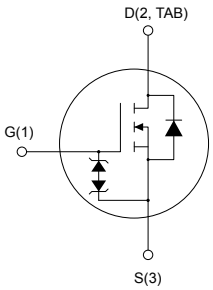
# N-channel 900 V, 3.6 Ω typ., 3 A SuperMESH Power MOSFET in a DPAK package




DPAK

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## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STD3NK90ZT4 | 900 V | 4.8 Ω | 3 A |

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

## Applications

- Switching applications

## Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

| Product status link |
|---|
| STD3NK90ZT4 |

| Product summary | |
|---|---|
| **Order code** | STD3NK90ZT4 |
| **Marking** | D3NK90Z |
| **Package** | DPAK |
| **Packing** | Tape and reel |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 900 | V |
| $V_{GS}$ | Gate-source voltage | ±30 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 3 | A |
| | Drain current (continuous) at $T_C$ = 100 °C | 1.89 | |
| $I_{DM}$(1) | Drain current (pulsed) | 12 | A |
| $P_{TOT}$ | Total power dissipation at $T_C$ = 25 °C | 90 | W |
| ESD | Gate-source, human body model (R = 1.5 kΩ, C = 100 pF) | 4 | kV |
| dv/dt(2) | Peak diode recovery voltage slope | 4.5 | V/ns |
| $T_{stg}$ | Storage temperature range | -55 to 150 | °C |
| $T_J$ | Operating junction temperature range | | °C |

1. *Pulse width limited by safe operating area.*
2. *$I_{SD}$ ≤ 3 A, di/dt ≤ 200 A/µs, $V_{DS}$ (peak) ≤ $V_{(BR)DSS}$, $V_{DD}$ = 80% $V_{(BR)DSS}$.*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJC}$ | Thermal resistance, junction-to-case | 1.38 | °C/W |
| $R_{thJA}$(1) | Thermal resistance, junction-to-ambient | 50 | °C/W |

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board.*

**Table 3. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width is limited by $T_J$ max.) | 3 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 180 | mJ |

# 2 Electrical characteristics

$T_C$ = 25 °C unless otherwise specified.

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 V | 900 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 900 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 900 V, $T_C$ = 125 °C(1) | | | 50 | |
| $I_{GSS}$ | Gate body leakage current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 50 µA | 3.00 | 3.75 | 4.50 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 1.5 A | | 3.6 | 4.8 | Ω |

1. *Specified by design, not tested in production.*

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 590 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 63 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 13 | - | pF |
| $C_{oss\ eq.}$(1) | Equivalent output capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 0 to 720 V | - | 35 | - | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 720 V, $I_D$ = 3 A, $V_{GS}$ = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior) | - | 22.7 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 4.2 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 12 | - | nC |

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.*

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 450 V, $I_D$ = 1.5 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 18 | - | ns |
| $t_r$ | Rise time | | - | 7 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 45 | - | ns |
| $t_f$ | Fall time | | - | 18 | - | ns |

**Table 7. Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 3 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 12 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 3 A, $V_{GS}$ = 0 V | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 3 A, di/dt = 100 A/µs, | - | 510 | | ns |
| $Q_{rr}$ | Reverse recovery charge | $V_{DD}$ = 40 V, $T_J$ = 150 °C | - | 2.2 | | nC |
| $I_{RRM}$ | Reverse recovery current | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 8.7 | | A |

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*
2. *Pulse width is limited by safe operating area.*

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

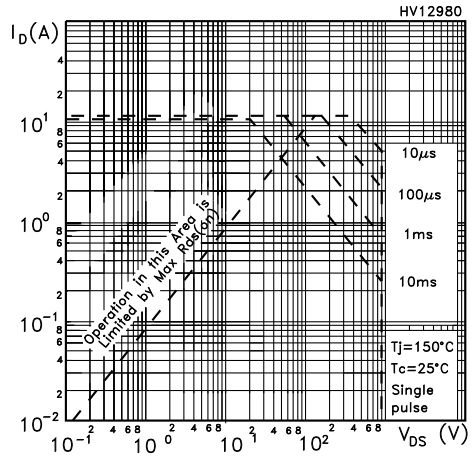



**Figure 2. Normalized transient thermal impedance**

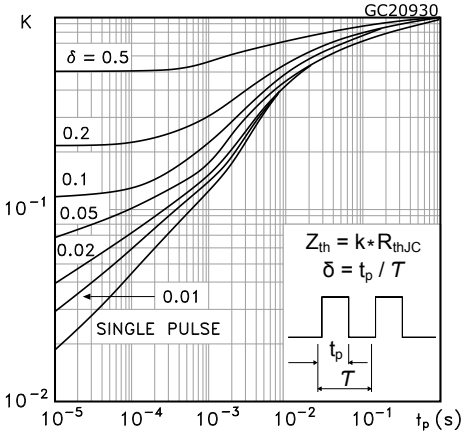



**Figure 3. Typical output characteristics**

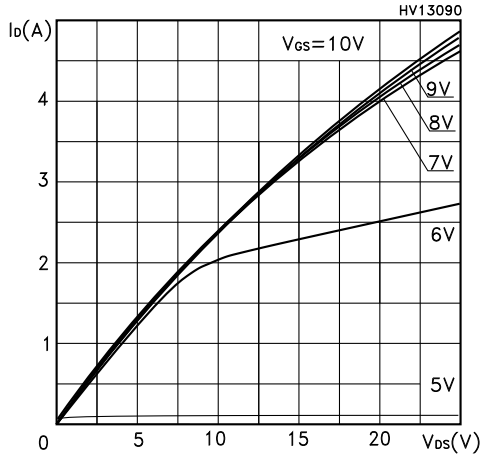



**Figure 4. Typical transfer characteristics**

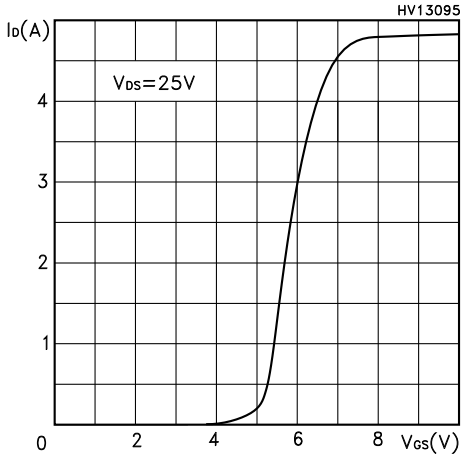



**Figure 5. Typical drain-source on-resistance**

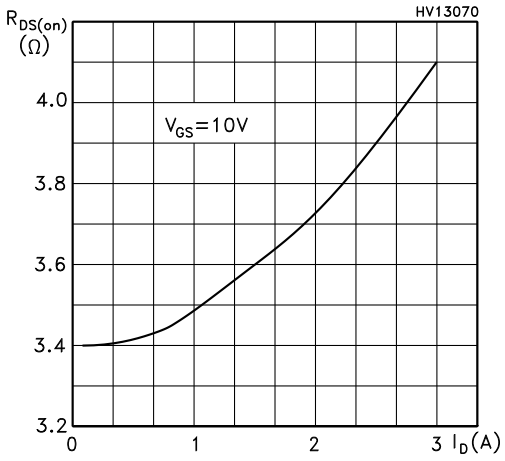



**Figure 6. Typical gate charge characteristics**

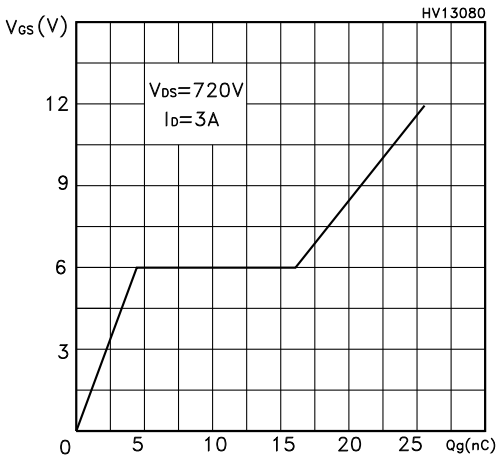


**Figure 7. Typical capacitance characteristics**

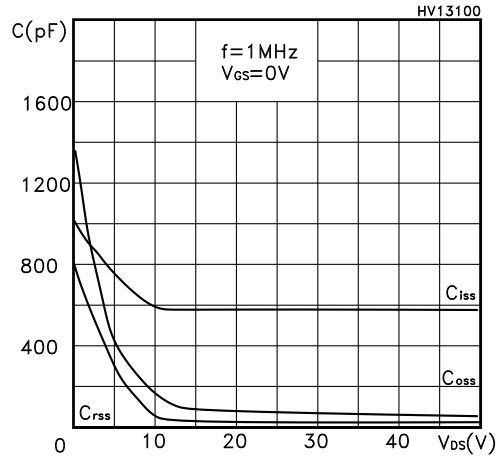



**Figure 8. Normalized gate threshold vs temperature**

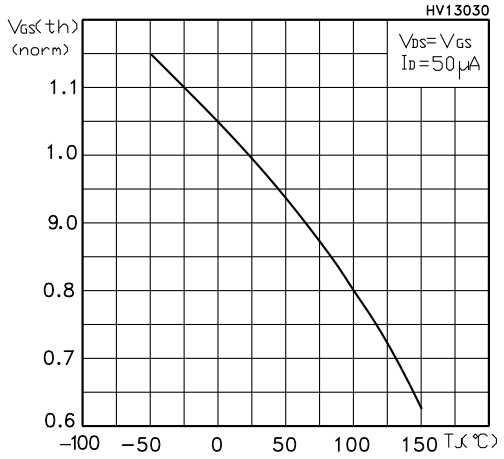



**Figure 9. Normalized on-resistance vs temperature**

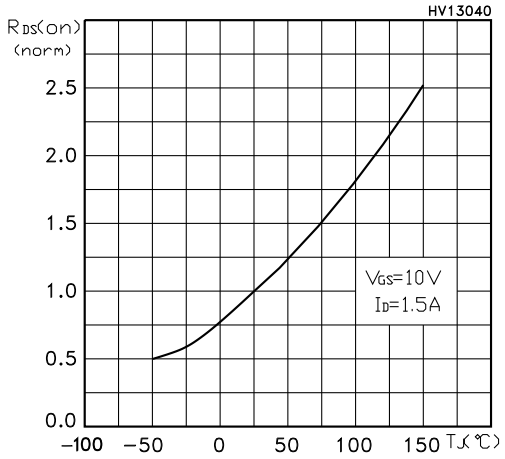



**Figure 10. Typical drain-source on-resistance**

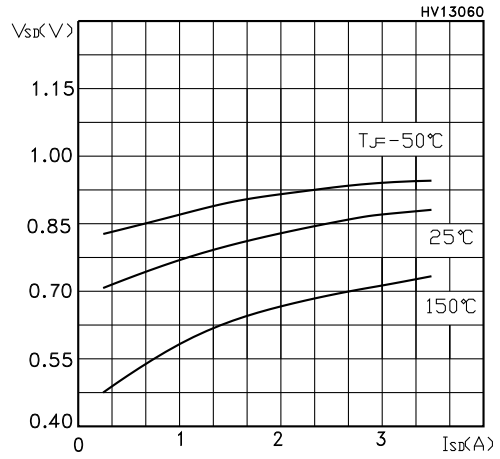



**Figure 11. Normalized breakdown voltage vs temperature**

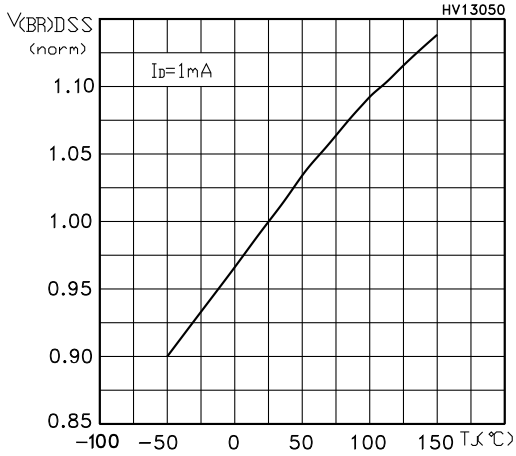
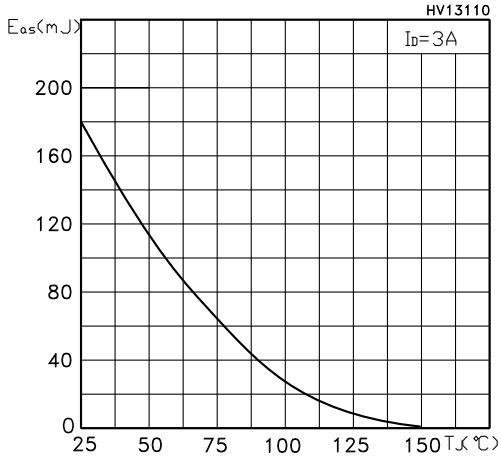



**Figure 12. Maximum avalanche energy vs temperature**



# 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**

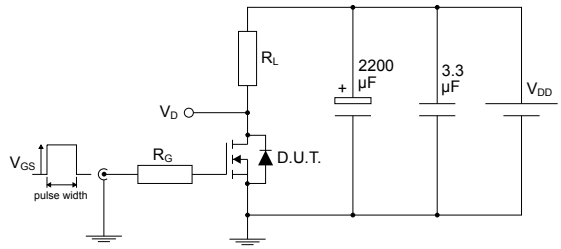



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**Figure 14. Test circuit for gate charge behavior**

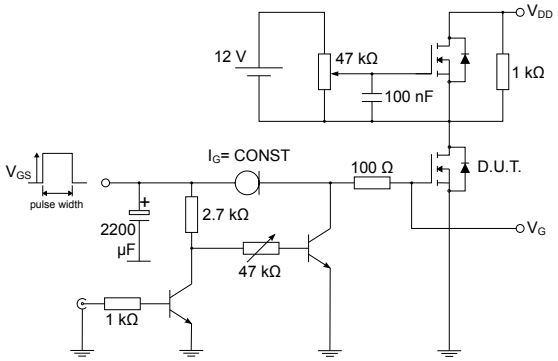


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**Figure 15. Test circuit for inductive load switching and diode recovery times**

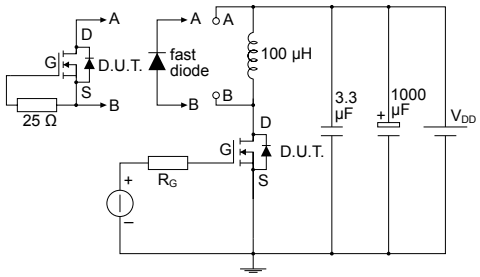


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**Figure 16. Unclamped inductive load test circuit**

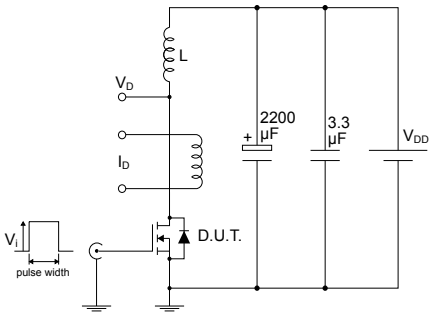


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**Figure 17. Unclamped inductive waveform**

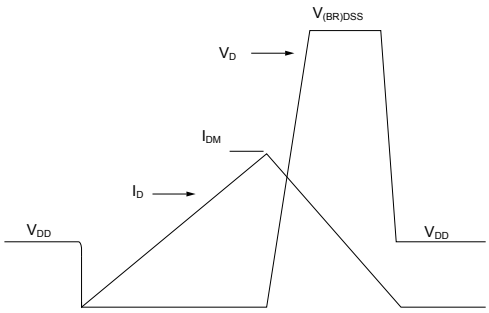


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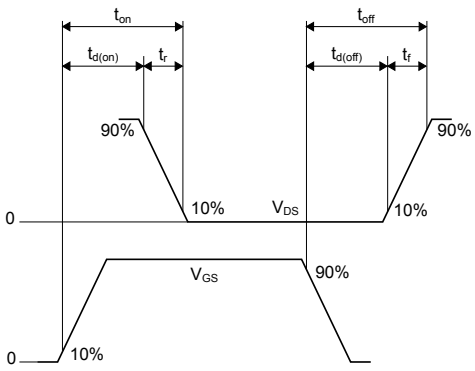
**Figure 18. Switching time waveform**

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# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 4.1 DPAK (TO-252) type C3 package information

Figure 19. **DPAK (TO-252) type C3 package outline**

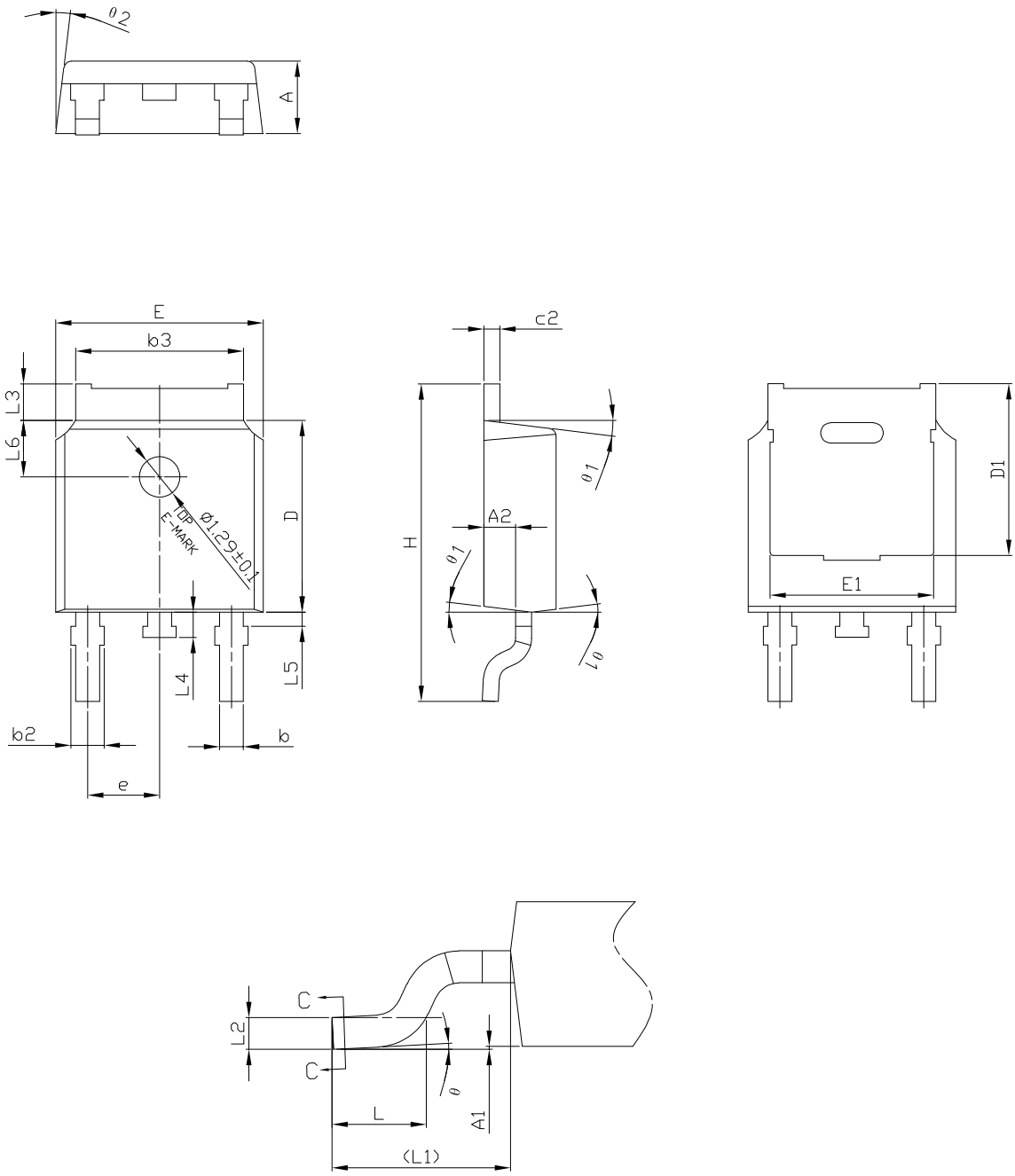


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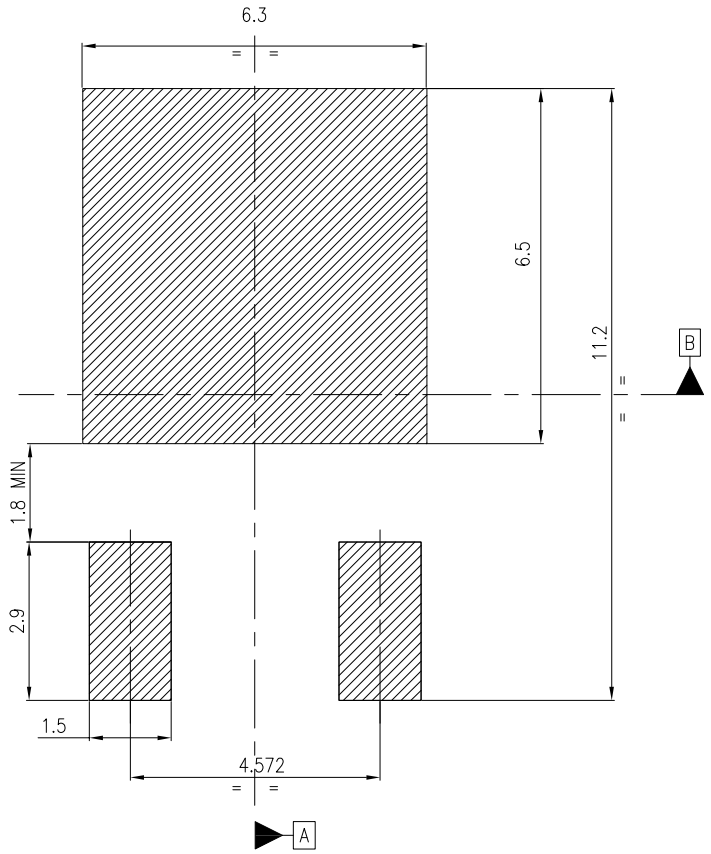
Table 8. **DPAK (TO-252) type C3 mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.20 | 2.30 | 2.38 |
| A1 | 0.00 | | 0.10 |
| A2 | 0.90 | 1.01 | 1.10 |
| b | 0.72 | | 0.85 |
| b2 | 0.72 | | 1.10 |
| b3 | 5.13 | 5.33 | 5.46 |
| c | 0.47 | | 0.60 |
| c2 | 0.47 | | 0.60 |
| D | 6.00 | 6.10 | 6.20 |
| D1 | 5.20 | 5.45 | 5.70 |
| E | 6.50 | 6.60 | 6.70 |
| E1 | 5.00 | 5.20 | 5.40 |
| e | 2.186 | 2.286 | 2.386 |
| H | 9.80 | 10.10 | 10.40 |
| L | 1.40 | 1.50 | 1.70 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.90 | | 1.25 |
| L4 | 0.60 | 0.80 | 1.00 |
| L5 | 0.15 | | 0.75 |
| L6 | 1.80 REF | | |
| θ | 0° | | 8° |
| θ1 | 5° | 7° | 9° |
| θ2 | 5° | 7° | 9° |

**Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)**




Notes:

1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664–1)

2) The device must be positioned within ⌖ 0.05 A B

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## 4.2 DPAK (TO-252) packing information

Figure 21. **DPAK (TO-252) tape outline**

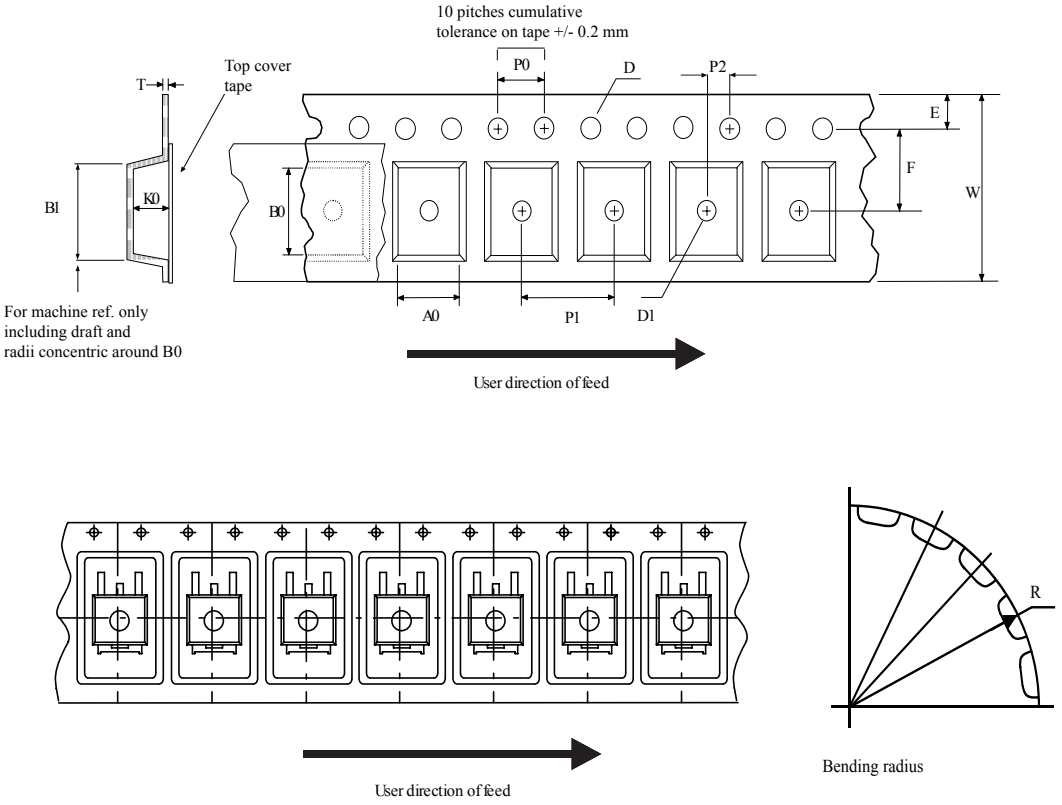

Figure 22. **DPAK (TO-252) reel outline**

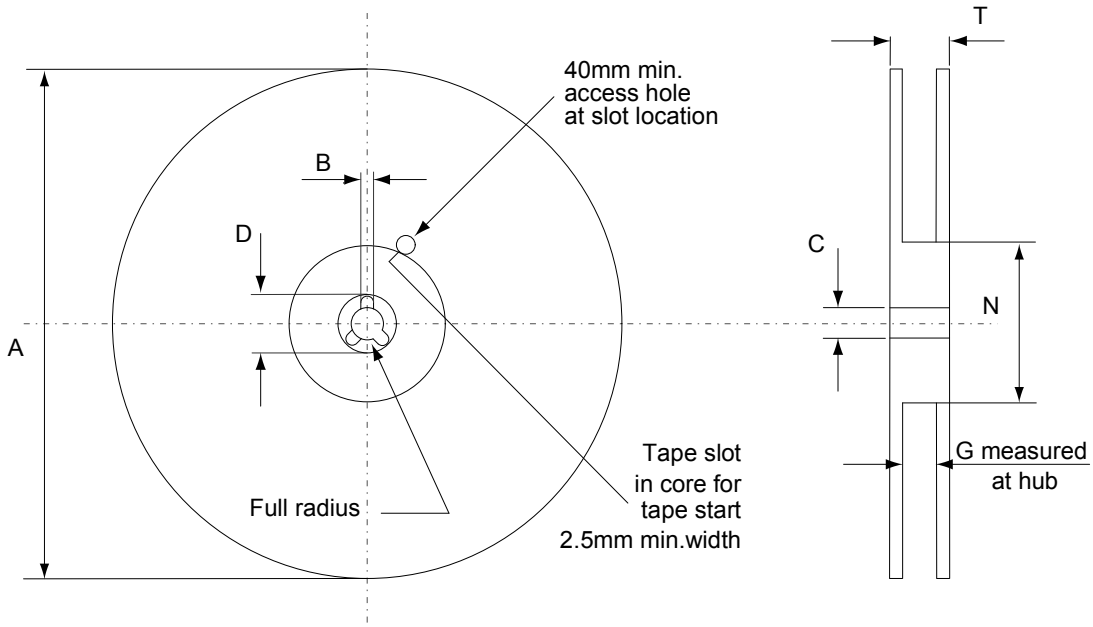


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Table 9. **DPAK (TO-252) tape and reel mechanical data**

| Tape | | | Reel | | |
|---|---|---|---|---|---|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 6.8 | 7 | A | | 330 |
| B0 | 10.4 | 10.6 | B | 1.5 | |
| B1 | | 12.1 | C | 12.8 | 13.2 |
| D | 1.5 | 1.6 | D | 20.2 | |
| D1 | 1.5 | | G | 16.4 | 18.4 |
| E | 1.65 | 1.85 | N | 50 | |
| F | 7.4 | 7.6 | T | | 22.4 |
| K0 | 2.55 | 2.75 | | | |
| P0 | 3.9 | 4.1 | Base qty. | | 2500 |
| P1 | 7.9 | 8.1 | Bulk qty. | | 2500 |
| P2 | 1.9 | 2.1 | | | |
| R | 40 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 15.7 | 16.3 | | | |

## Revision history

Table 10. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 24-Oct-2006 | 1 | First release. |
| 29-Jan-2013 | 2 | – The part number STD3NK90Z-1 has been moved to a separate datasheet<br>– Minor text changes<br>– Updated: Section 4: Package mechanical data |
| 20-Aug-2018 | 3 | Removed maturity status indication from cover page. The document status is production data.<br>Updated title in cover page, *Section 1 Electrical ratings*, *Section 2 Electrical characteristics* and *Section 4 Package information*.<br>Minor text changes. |
| 31-Aug-2023 | 4 | The part numbers STP3NK90Z and STP3NK90ZFP have been moved to separate datasheets and the document has been updated accordingly.<br>Updated Section 4 Package information.<br>Minor text changes. |

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