HIGH-SPEED DIFFERENTIAL I/O AMPLIFIERS

FEATURES

- **High Performance**
  - **– 150 MHz –3 dB Bandwidth (V_{CC} = ±5 V)**
  - **– 650 V/µs Slew Rate (V_{CC} = ±15 V)**
  - **– –89 dB Third Harmonic Distortion at 1 MHz**
  - **– –83 dB Total Harmonic Distortion at 1 MHz**
  - **– 7.6 nV/$\sqrt{Hz}$ Input-Referred Noise**
- **Differential Input/Differential Output**
  - **– Balanced Outputs Reject Common-Mode Noise**
  - **– Differential Reduced Second Harmonic Distortion**
- **Wide Power Supply Range**
  - **– V_{CC} = 5 V Single Supply to ±15 V Dual Supply**
- **$I_{CC(SD)}$ = 1 mA (V_{CC} = ±5) in Shutdown Mode (THS4150)**

KEY APPLICATIONS

- **Single-Ended To Differential Conversion**
- **Differential ADC Driver**
- **Differential Antialiasing**
- **Differential Transmitter and Receiver**
- **Output Level Shifter**

DESCRIPTION

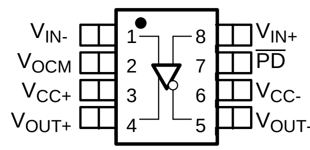
The THS415x is one in a family of fully differential input/differential output devices fabricated using Texas Instruments' state-of-the-art BiComI complementary bipolar process.

The THS415x is made of a true fully-differential signal path from input to output. This design leads to an excellent common-mode noise rejection and improved total harmonic distortion.

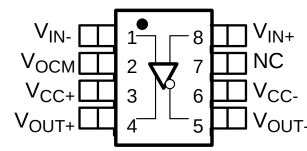
RELATED DEVICES

DEVICE	DESCRIPTION
THS412x	100 MHz, 43 V/µs, 3.7 nV/$\sqrt{Hz}$
THS413x	150 MHz, 51 V/µs, 1.3 nV/$\sqrt{Hz}$
THS414x	160 MHz, 450 V/µs, 6.5 nV/$\sqrt{Hz}$

THS4150
D, DGN, DGK PACKAGES
(TOP VIEW)



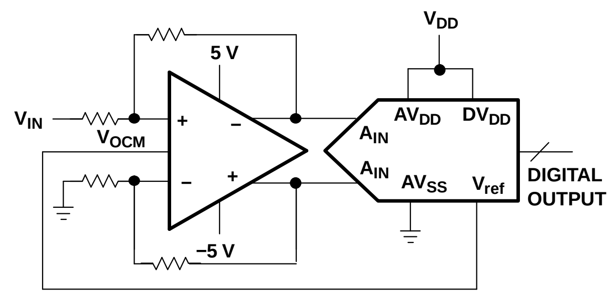
THS4151
D, DGN, DGK PACKAGES
(TOP VIEW)



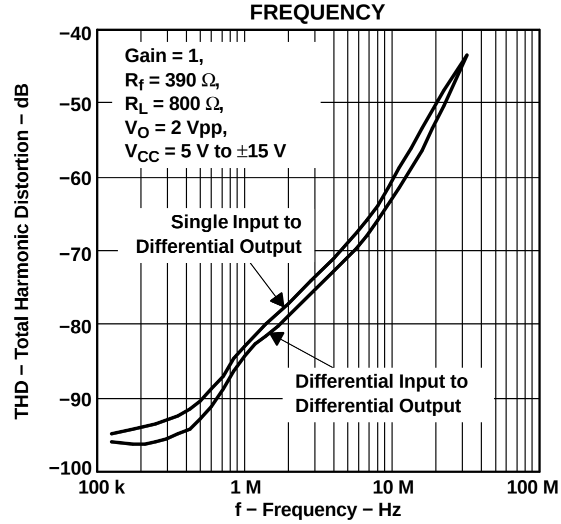
HIGH-SPEED DIFFERENTIAL I/O FAMILY

DEVICE	NUMBER OF CHANNELS	SHUTDOWN
THS4150	1	X
THS4151	1	-

Typical A/D Application Circuit



THS4151
TOTAL HARMONIC DISTORTION
vs
FREQUENCY



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES					EVALUATION MODULES
	SMALL OUTLINE(D)	MSOP PowerPAD™		MSOP		
		(DGN)	SYMBOL	(DGK)	SYMBOL	
0°C to 70°C	THS4150CD	THS4150CDGN	AQB	THS4150CDGK	ATT	THS4150EVM
	THS4151CD	THS4151CDGN	AQD	THS4151CDGK	ATU	THS4151EVM
–40°C to 85°C	THS4150ID	THS4150IDGN	AQC	THS4150IDGK	AST	-
	THS4151ID	THS4151IDGN	AQE	THS4151IDGK	ASU	-

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC-} to V_{CC+}	Supply voltage		±16.5 V
V_I	Input voltage		$\pm V_{CC}$
I_O	Output current(2)		150 mA
V_{ID}	Differential input voltage		±6 V
	Continuous total power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature(3)		150°C
	Maximum junction temperature, continuous operation, long term reliability(4)		125°C
T_A	Operating free-air temperature	C suffix	0°C to 70°C
		I suffix	–40°C to 85°C
T_{stg}	Storage temperature		–65°C to 150°C
	Lead temperature (5)		
	ESD ratings	HBM	2500 V
		CDM	1500 V
		MM	200 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The THS415x may incorporate a PowerPad™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the PowerPad™ thermally enhanced package.
(3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.
(5) See the MSL/Reflow Rating information provided with the material, or see TI's website at www.ti.com for the latest information.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} [(1)] (°C/W)	θ_{JC} (°C/W)	POWER RATING [(2)]	
			T_A = 25°C	T_A = 85°C
D	97.5	38.3	1.02 W	410 mW
DGN	58.4	4.7	1.71 W	685 mW
DGK	260	54.2	385 mW	154 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC+} to V_{CC-}	Supply voltage	Dual supply	±2.5		±15	V
		Single supply	5		30	
T_A	Operating free-air temperature	C suffix	0		70	°C
		I suffix	–40		85	

ELECTRICAL CHARACTERISTICS

V_{CC} = 15 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small signal bandwidth (–3 dB)	V_{CC} = 5	Gain = 1, R_f = 390 Ω		150		MHz
		V_{CC} = ±5			150		
		V_{CC} = ±15			150		
BW	Small signal bandwidth (–3 dB)	V_{CC} = 5	Gain = 2, R_f = 750 Ω		80		MHz
		V_{CC} = ±5			81		
		V_{CC} = ±15			81		
SR	Slew rate [(1)]	V_{CC} = ±15,	Gain = 1		650		V/µs
t_s	Settling time to 0.1%	Differential step voltage = 2 V_{PP}, Gain = 1			53		ns
	Settling time to 0.01%				247		
DISTORTION PERFORMANCE							
THD	Total harmonic distortion Differential input, differential output Gain = 1, R_f = 390 Ω, R_L = 800 Ω, V_O= 2 V_{PP}	V_{CC} = 5	f = 1 MHz		–85		dB
			f = 8 MHz		–66		
		V_{CC} = ±5	f = 1 MHz		–83		
			f = 8 MHz		–65		
		V_{CC} = ±15	f = 1 MHz		–84		
			f = 8 MHz		–65		
	Spurious free dynamic range (SFDR)	V_O = 2 V_{PP},	f = 1 MHz		–87		dB
	Third intermodulation distortion	V_O = 0.14 V_{RMS}, Gain = 1, f = 20 MHz			-95		dBc
NOISE PERFORMANCE							
V_n	Input voltage noise	f = 10 kHz			7.6		nV/√Hz
I_n	Input current noise	f = 10 kHz			1.78		pA/√Hz

(1) Slew rate is measured from an output level range of 25% to 75%.

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 15 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC PERFORMANCE							
	Open loop gain	T_A = 25°C		63	67		dB
		T_A = full range[(2)]		60			
V_{OS}	Input offset voltage	T_A = 25°C			1.1	7	mV
		T_A = full range				8.5	
	Input offset voltage, referred to V_{OCM}	T_A = 25°C			0.6	8	
	Offset drift	T_A = full range			7		µV/°C
I_{IB}	Input bias current	T_A = full range			4.3	15	µA
I_{OS}	Input offset current				250	1200	nA
	Offset drift	T_A = full range			0.7		nA/°C
	Shutdown delay to output	T_A = full range			1.1		µs
INPUT CHARACTERISTICS							
CMRR	Common-mode rejection ratio	T_A = full range		–75	–83		dB
V_{ICR}	Common-mode input voltage range				–3.8 to 5.6		V
r_i	Input resistance	Measured into each input terminal			14.4		MΩ
C_i	Input capacitance, closed loop				3.9		pF
r_o	Output resistance	Open loop/single ended			0.4		Ω
$r_{o(SD)}$	Output resistance	Shutdown			636		Ω
OUTPUT CHARACTERISTICS							
	Output voltage swing	V_{CC} = 5 V	T_A = 25°C	1.2 to 3.8	0.9 to 4.1		V
			T_A = full range	1.2 to 3.8			
		V_{CC} = ±5 V	T_A = 25°C	±3.7	±3.9		
			T_A = full range	±3.6			
		V_{CC} = ±15 V	T_A = 25°C	±11.6	±12.7		
			T_A = full range	±11			
I_O	Output current, R_L = 7Ω	V_{CC} = 5 V	T_A = 25°C	30	45		mA
			T_A = full range	25			
		V_{CC} = ±5 V	T_A = 25°C	45	60		
			T_A = full range	35			
		V_{CC} = ±15 V	T_A = 25°C	65	85		
			T_A = full range	50			
POWER SUPPLY							
V_{CC}	Supply voltage range	Single supply		4	30	33	V
		Split supply		±2	±15	±16.5	
I_{CC}	Quiescent current (per amplifier)	V_{CC} = ±5 V	T_A = 25°C		15.8	18.5	mA
			T_A = full range			21	
		V_{CC} = ±15 V	T_A = 25°C		17.5	21	
			T_A = full range			23	
$I_{CC(SD)}$	Quiescent current (shutdown) (THS4150)[(3)]	T_A = 25°C			1	1.3	mA
		T_A = full range				1.5	
PSRR	Power supply rejection ratio (dc)	T_A = 25°C		70	90		dB
		T_A = full range		65			

(2) The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.
(3) For detailed infomation on the behavior of the power-down circuit, see the *power-down mode* description in the *Principles of Operation* section of this data sheet.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Small signal frequency response		1, 2
	Large signal frequency response		3
	Settling time		4
SR	Slew rate	vs Temperature	5
	Total harmonic distortion	vs Frequency	6
		vs Output voltage	7
	Harmonic distortion	vs Frequency	8–13
		vs Output voltage	14–17
	Third intermodulation distortion	vs Output voltage	18
V_n	Voltage noise	vs Frequency	19
I_n	Current noise	vs Frequency	20
V_O	Output voltage	vs Single-ended load resistance	21
	Power supply current shutdown	vs Supply voltage	22
	Output current range	vs Supply voltage	23
V_{OS}	Single-ended output offset voltage	vs Common-mode output voltage	24
CMMR	Common-mode rejection ratio	vs Frequency	25
z	Impedance of the V_{OCM} terminal	vs Frequency	26
z_o	Output impedance (powered up)	vs Frequency	27
z_o	Output impedance (shutdown)	vs Frequency	28
PSRR	Power supply rejection ratio	vs Frequency	29

TYPICAL CHARACTERISTICS

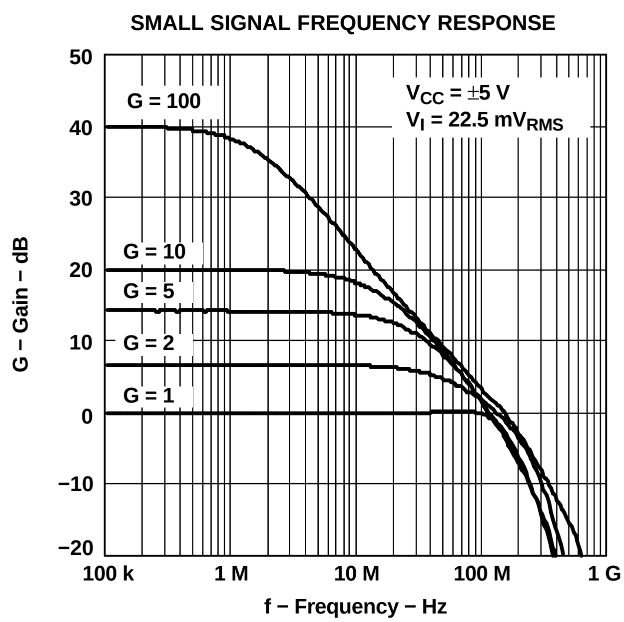


Figure 1.

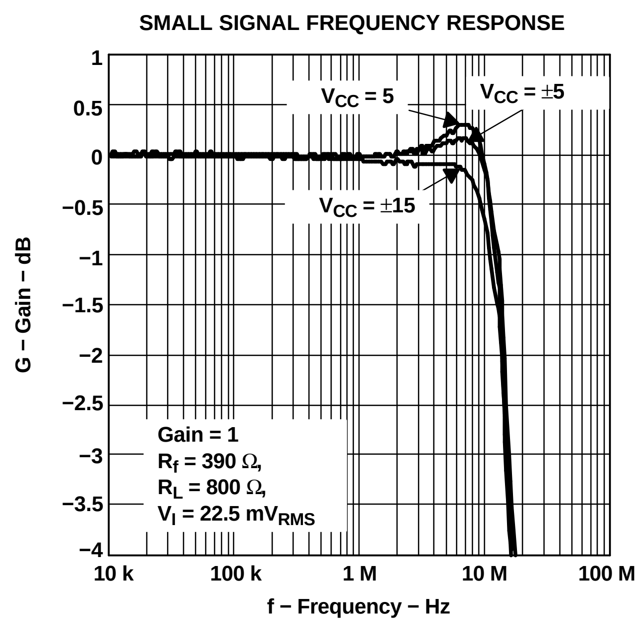


Figure 2.

TYPICAL CHARACTERISTICS (continued)

LARGE SIGNAL FREQUENCY RESPONSE

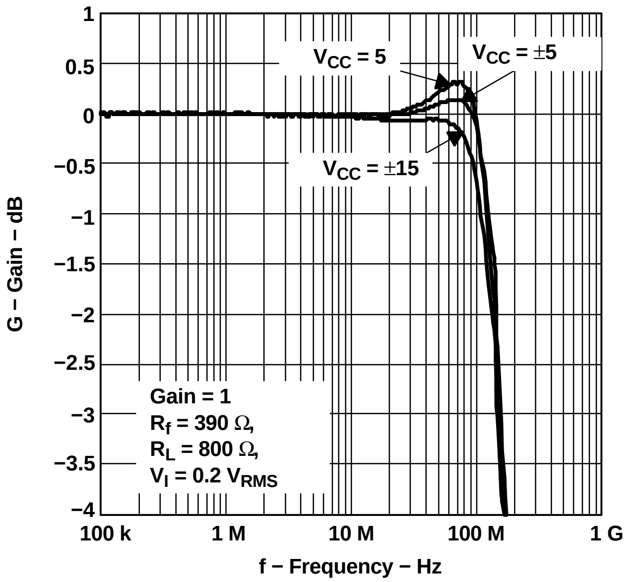


Figure 3.

SETTLING TIME

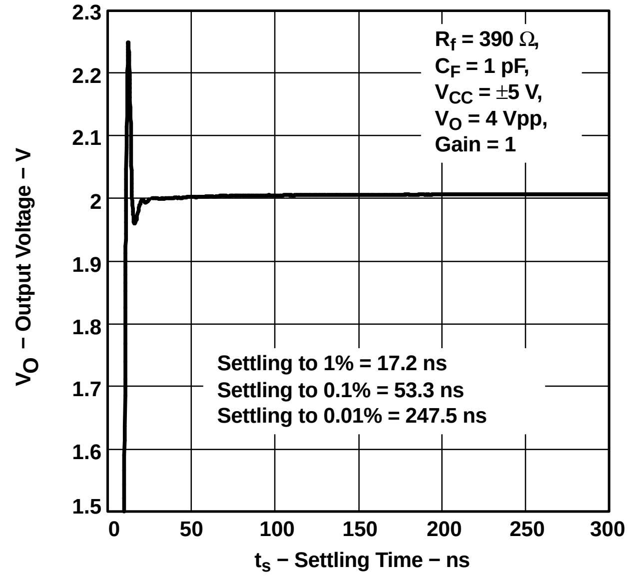


Figure 4.

SLEW RATE
vs
TEMPERATURE

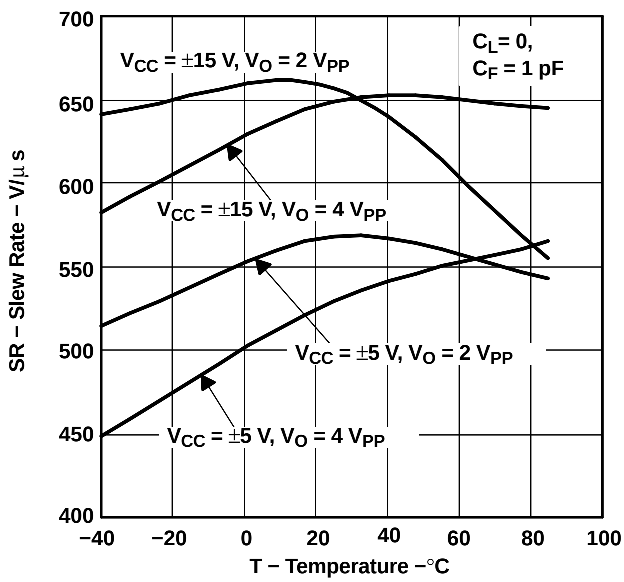


Figure 5.

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

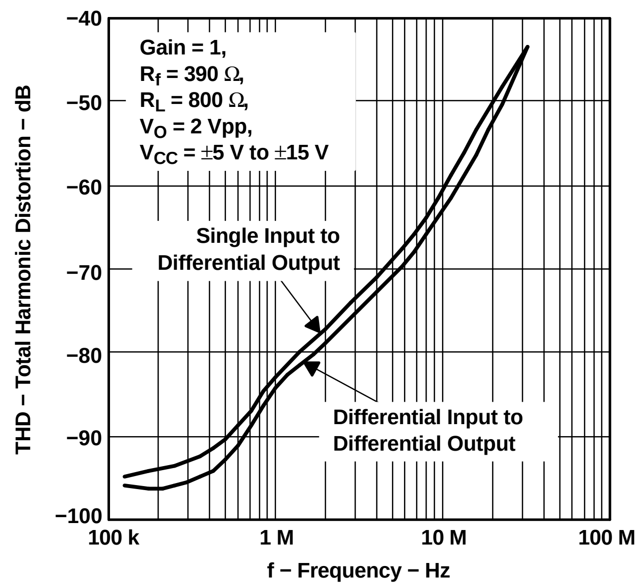


Figure 6.

TYPICAL CHARACTERISTICS (continued)

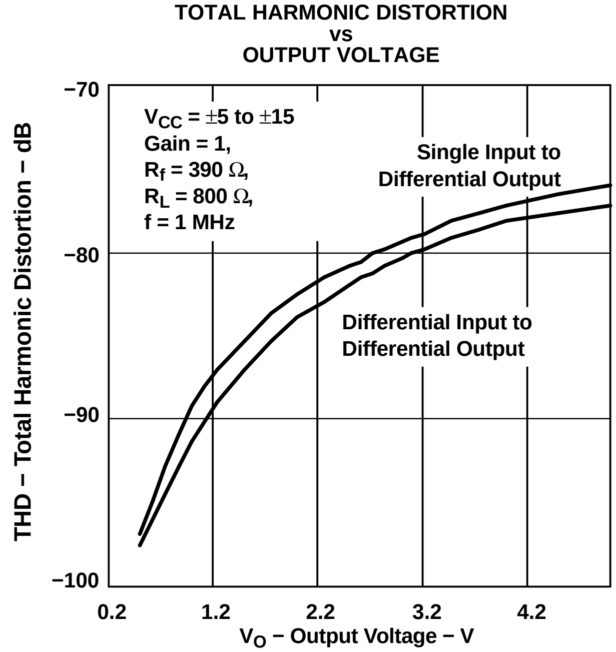


Figure 7.

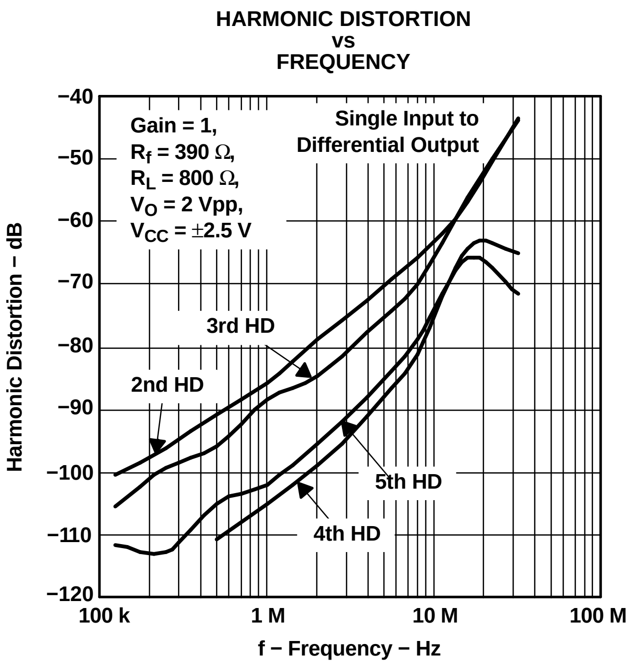


Figure 8.

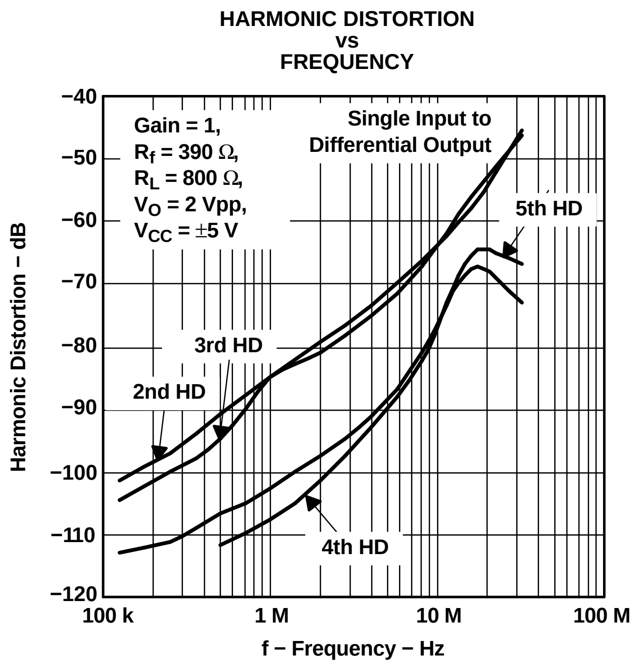


Figure 9.

TYPICAL CHARACTERISTICS (continued)

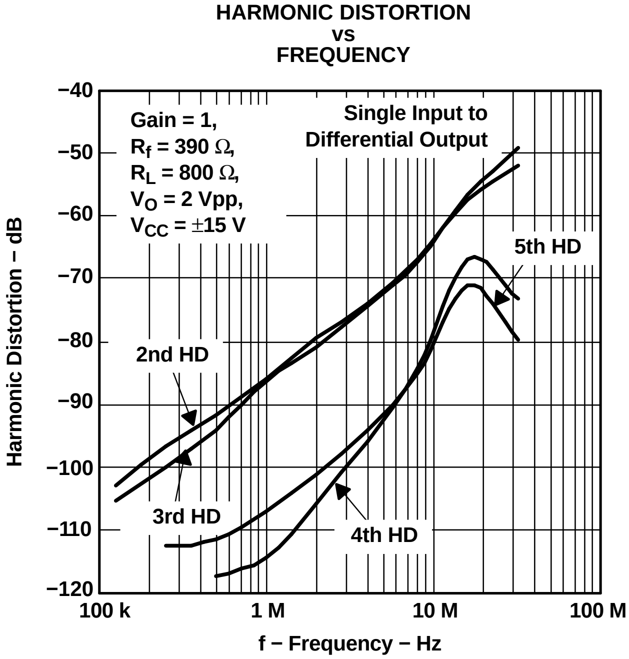


Figure 10.

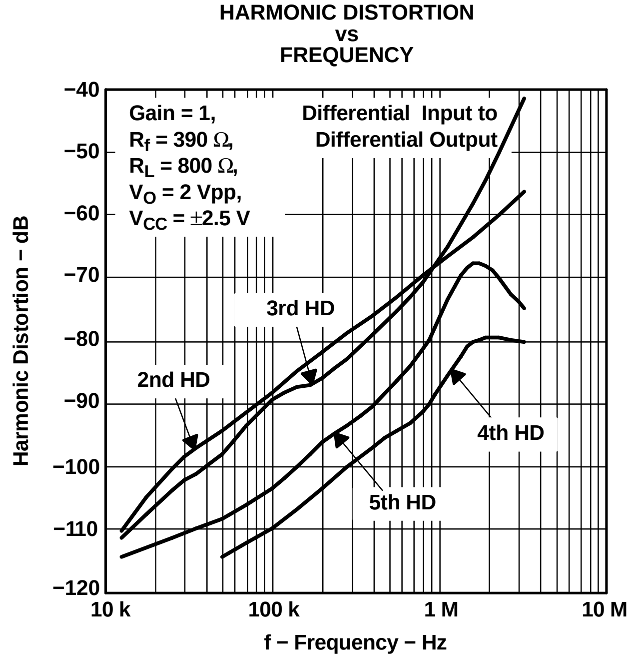


Figure 11.

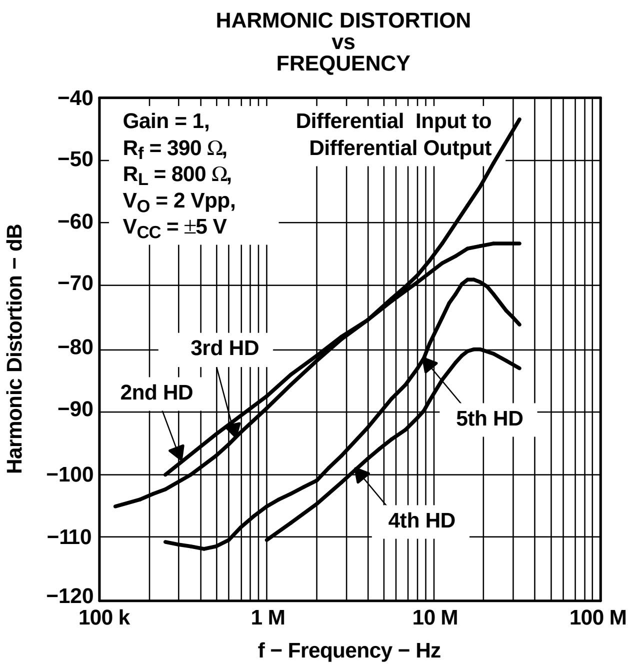


Figure 12.

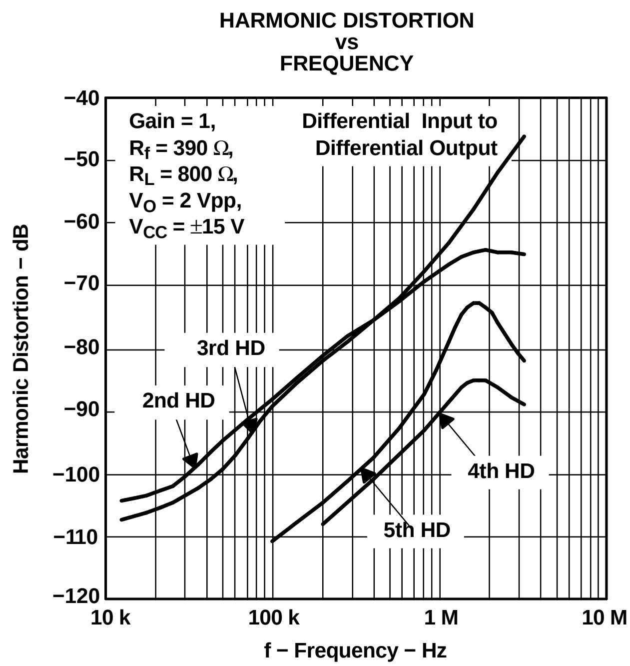


Figure 13.

TYPICAL CHARACTERISTICS (continued)

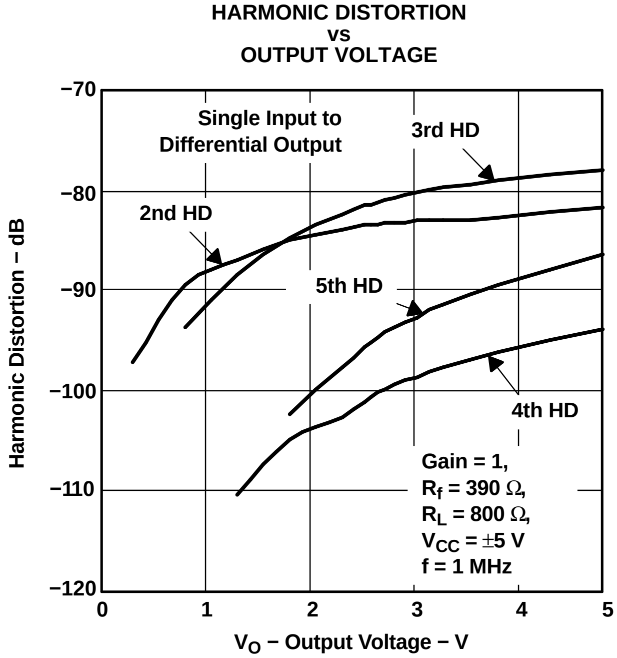


Figure 14.

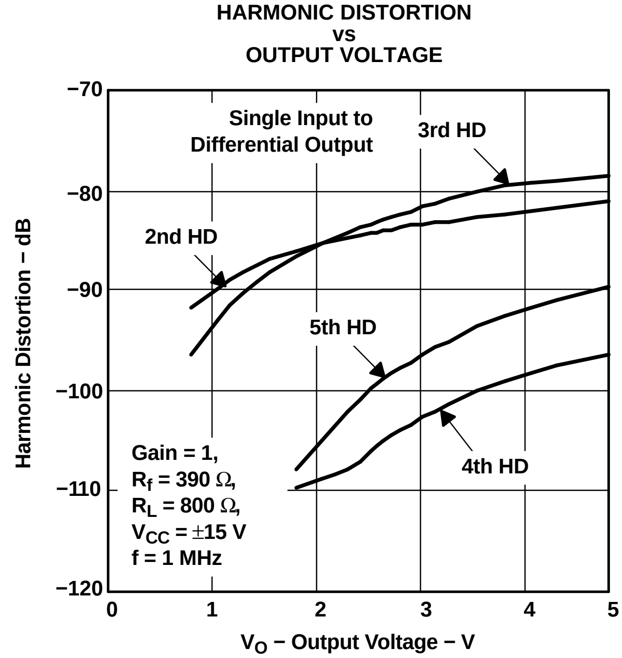


Figure 15.

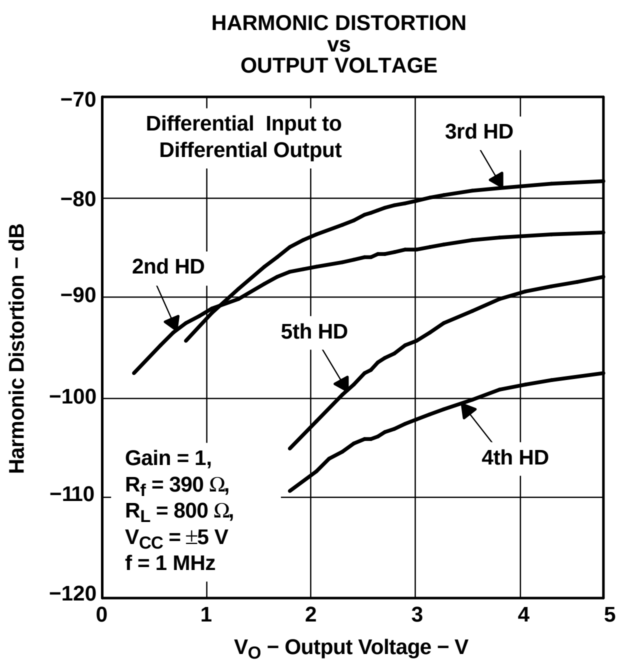


Figure 16.

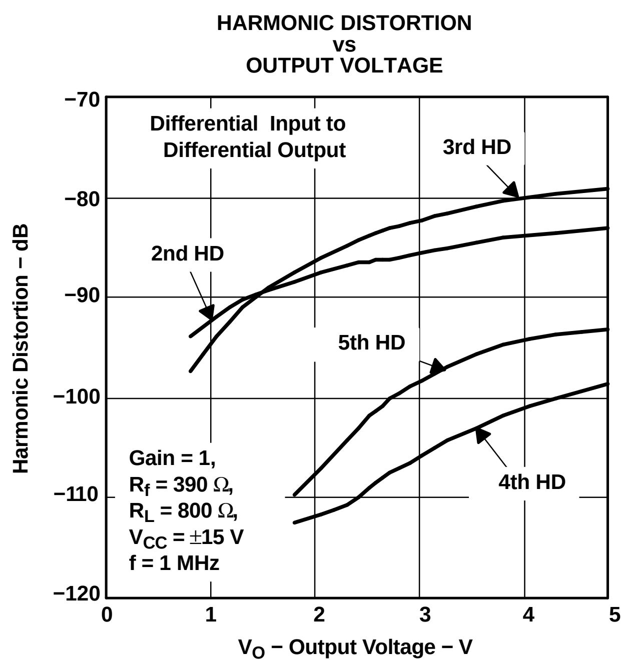


Figure 17.

TYPICAL CHARACTERISTICS (continued)

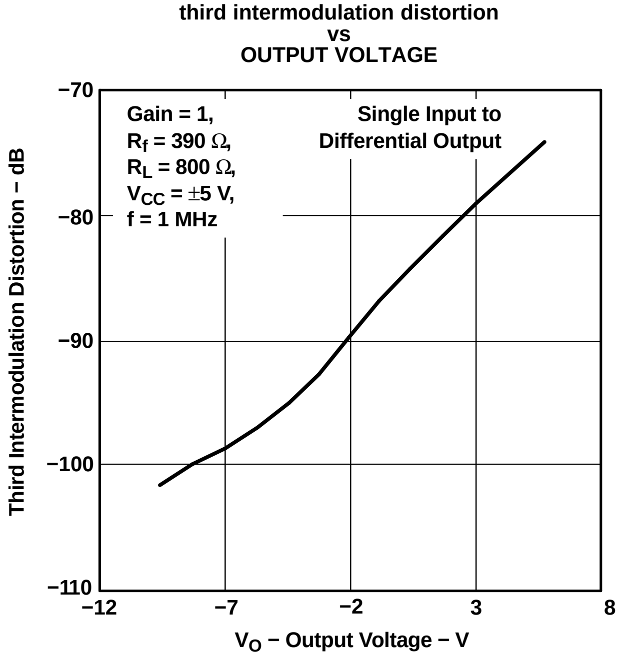


Figure 18.

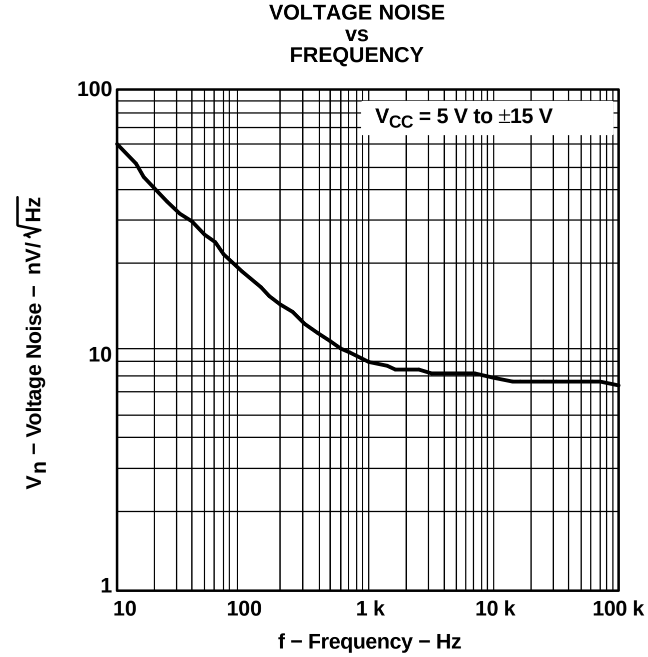


Figure 19.

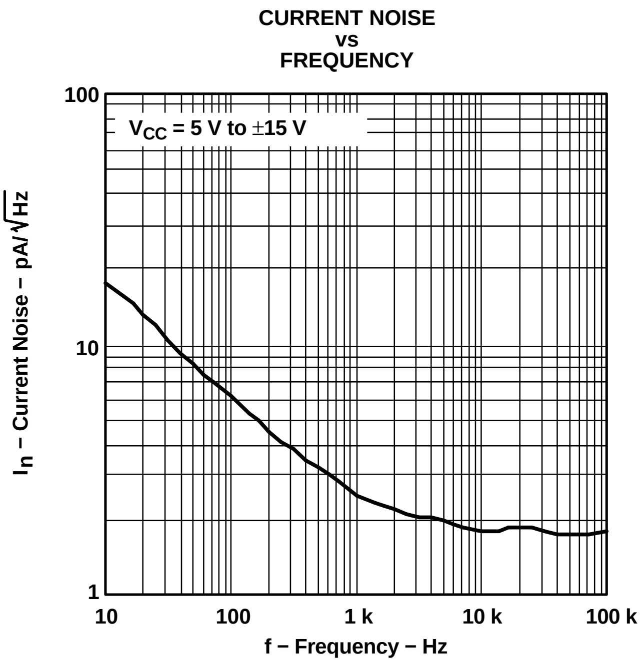


Figure 20.

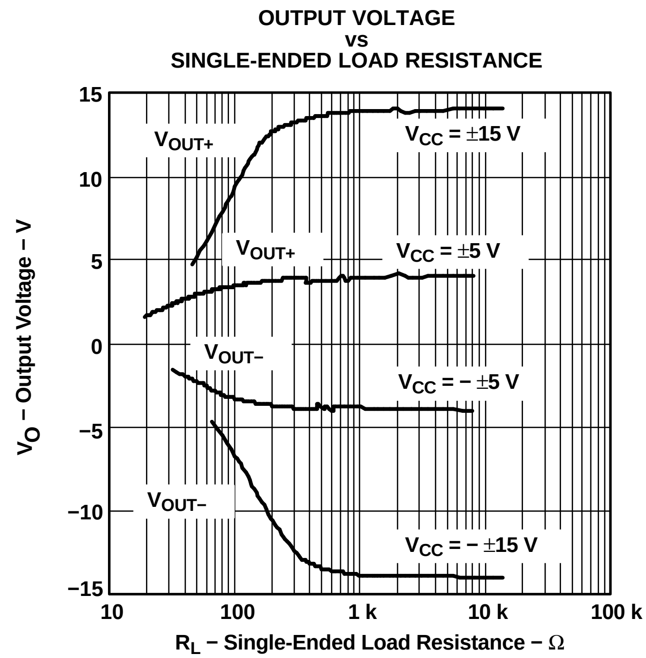


Figure 21.

TYPICAL CHARACTERISTICS (continued)

POWER SUPPLY CURRENT SHUTDOWN
vs
SUPPLY VOLTAGE

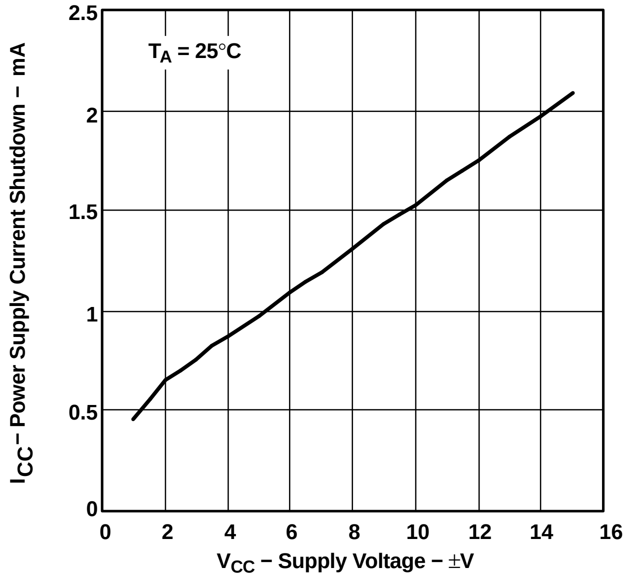


Figure 22.

OUTPUT CURRENT RANGE
vs
SUPPLY VOLTAGE

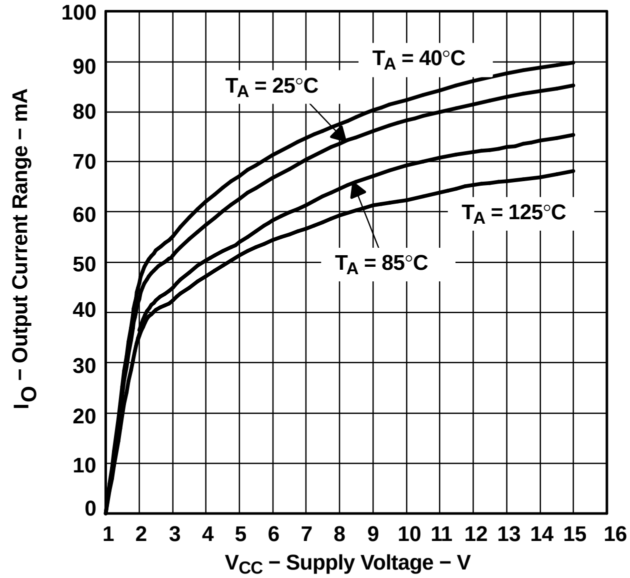


Figure 23.

SINGLE-ENDED OUTPUT OFFSET VOLTAGE
vs
COMMON-MODE OUTPUT VOLTAGE

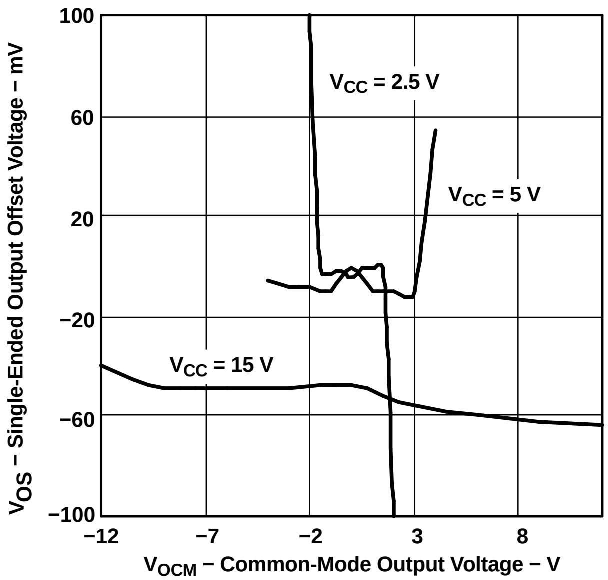


Figure 24.

COMMON MODE REJECTION RATIO
vs
FREQUENCY

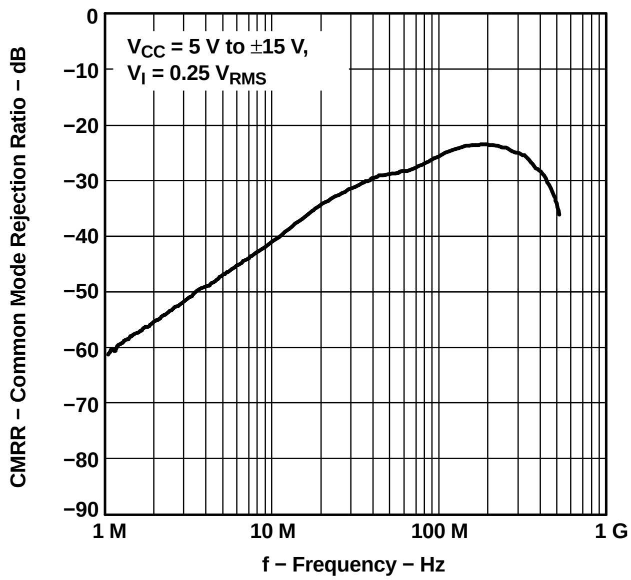


Figure 25.

TYPICAL CHARACTERISTICS (continued)

IMPEDANCE OF THE V_{OCM} TERMINAL
vs
FREQUENCY

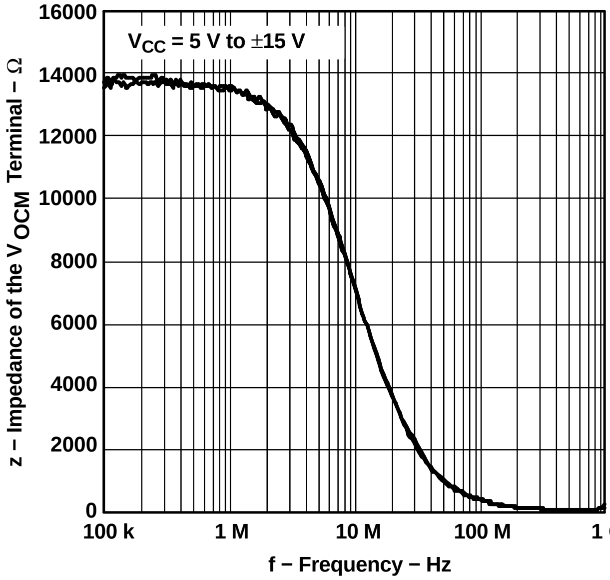


Figure 26.

OUTPUT IMPEDANCE (POWERED UP)
vs
FREQUENCY

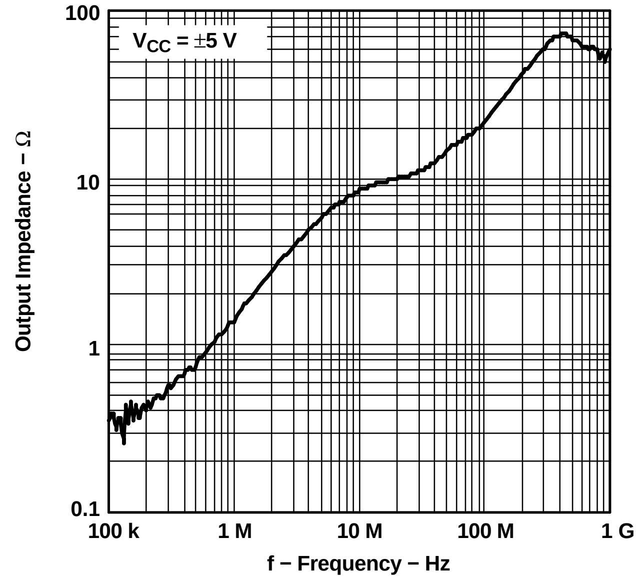


Figure 27.

OUTPUT IMPEDANCE (SHUTDOWN)
vs
FREQUENCY

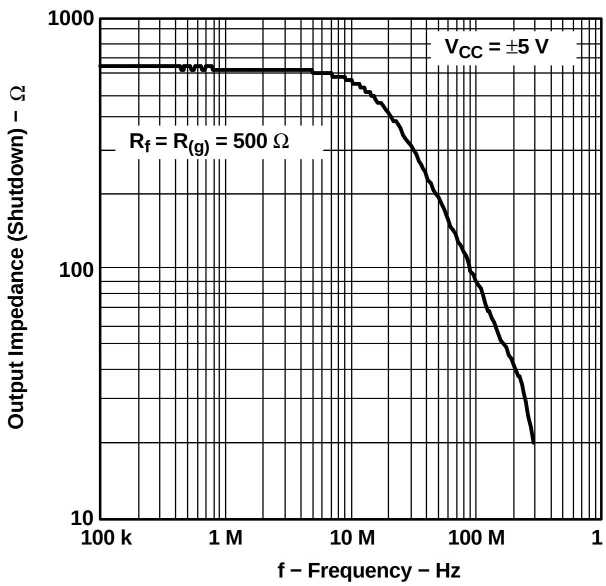


Figure 28.

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

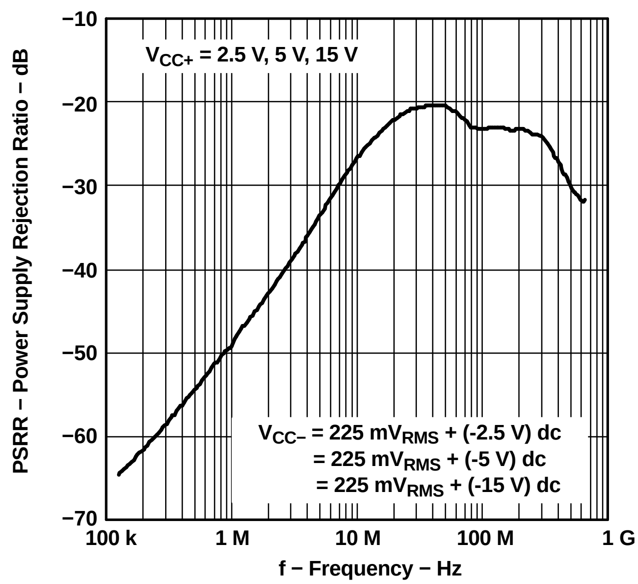


Figure 29.

APPLICATION INFORMATION

RESISTOR MATCHING

Resistor matching is important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion will diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

V_{OCM} sets the dc level of the output signals. If no voltage is applied to the V_{OCM} pin, it will be set to the midrail voltage internally defined as:

$$\frac{\left(V_{CC+}\right) + \left(V_{CC-}\right)}{2}$$

In the differential mode, the V_{OCM} on the two outputs cancel each other. Therefore, the output in the differential mode is the same as the input when gain is 1. V_{OCM} has a high bandwidth capability up to the typical operation range of the amplifier. For the prevention of noise going through the device, use a 0.1 µF capacitor on the V_{OCM} pin as a bypass capacitor. Figure 30 shows the simplified diagram of the THS415x.

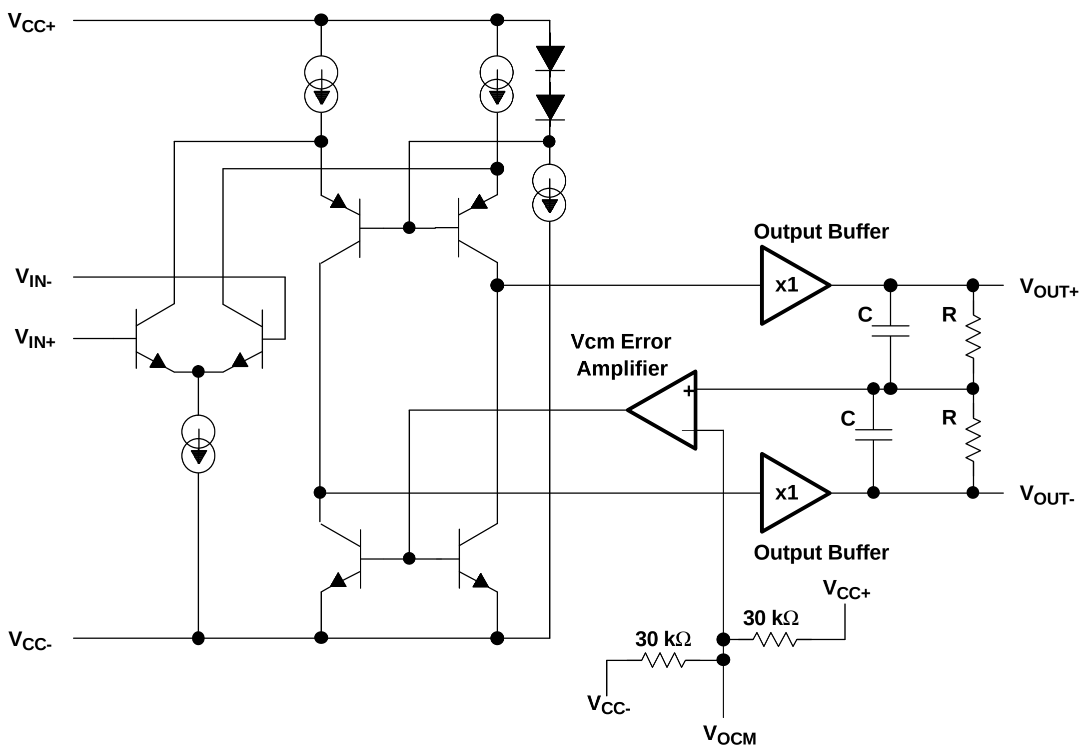


Figure 30. THS415x Simplified Diagram

APPLICATION INFORMATION (continued)

DATA CONVERTERS

Data converters are one of the most popular applications for the fully differential amplifiers. The following schematic shows a typical configuration of a fully differential amplifier attached to a differential ADC.

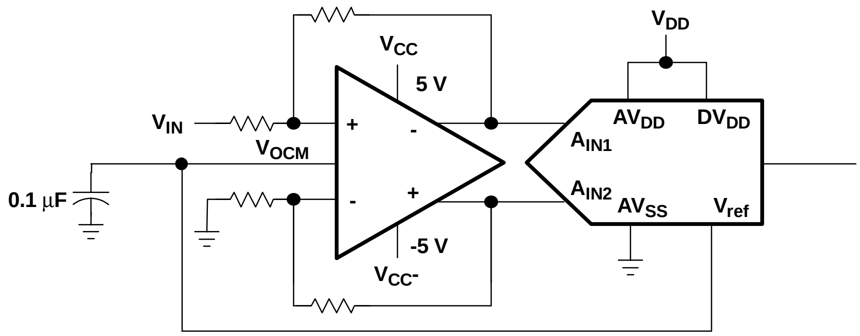


Figure 31. Fully Differential Amplifier Attached to a Differential ADC

Fully differential amplifiers can operate with a single supply. V_{OCM} defaults to the midrail voltage, $V_{CC}/2$. The differential output may be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then it is recommended to connect it directly to the V_{OCM} of the amplifier using a bypass capacitor for stability. For proper operation, the input common-mode voltage to the input terminal of the amplifier should not exceed the common-mode input voltage range.

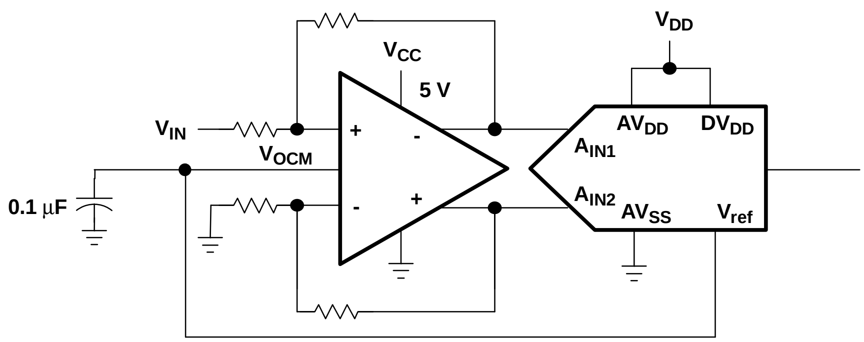


Figure 32. Fully Differential Amplifier Using a Single Supply

Some single supply applications may require the input voltage to exceed the common-mode input voltage range. In such cases, the following circuit configuration is suggested to bring the common-mode input voltage within the specifications of the amplifier.

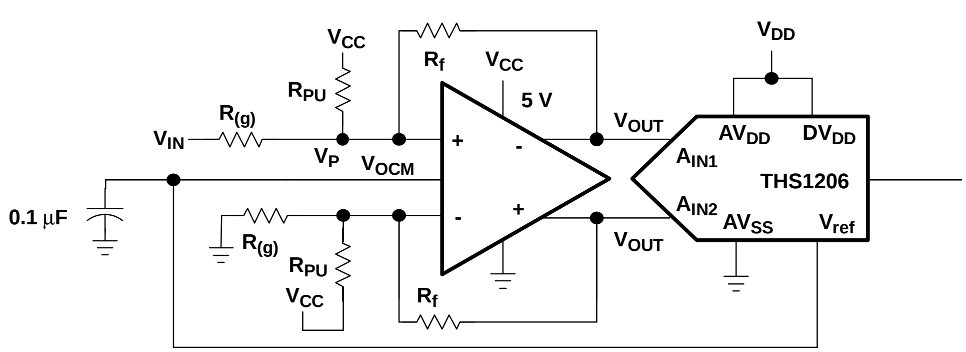


Figure 33. Circuit With Improved Common-Mode Input Voltage

APPLICATION INFORMATION (continued)

The following equation is used to calculate R_{PU}:

$$R_{PU} = \frac{V_P - V_{CC}}{\left(V_{IN} - V_P\right)\frac{1}{RG} + \left(V_{OUT} - V_P\right)\frac{1}{RF}}$$

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS415x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 34. A minimum value of 20 Ω should work well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 20 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

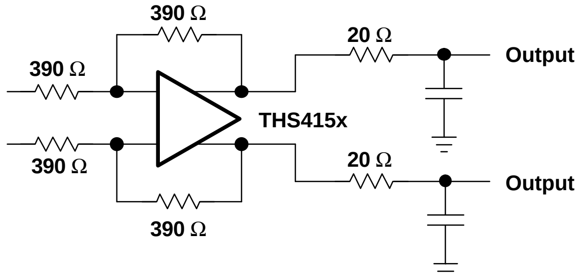


Figure 34. Driving a Capacitive Load

ACTIVE ANTIALIAS FILTERING

For signal conditioning in ADC applications, it is important to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high frequency noise with the frequency of operation. Figure 35 presents a method by which the noise may be filtered in the THS415x.

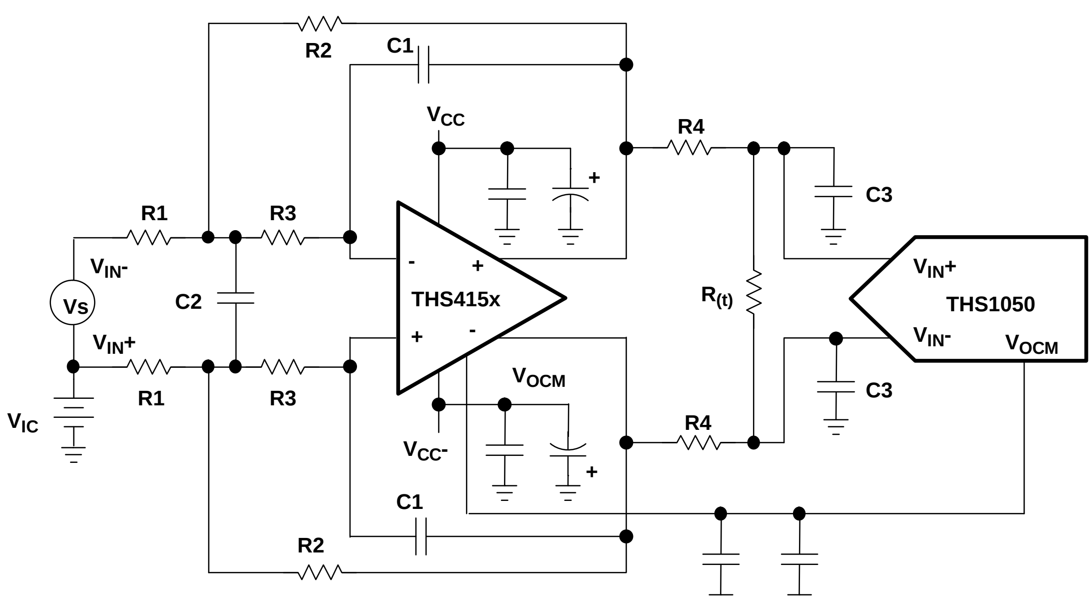


Figure 35. Antialias Filtering

APPLICATION INFORMATION (continued)

The transfer function for this filter circuit is:

$$H_d(f) = \left[\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1}\right] \times \left[\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi fR4RtC3}{2R4 + Rt}}\right] \quad \text{Where } K = \frac{R2}{R1}$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}} \quad \text{and} \quad Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1}$$

K sets the pass band gain, fc is the cutoff frequency for the filter, FSF is a frequency-scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \quad \text{and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re}$$

where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$FSF \times fc = \frac{1}{2\pi RC\sqrt{2 \times mn}} \quad \text{and } Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)}$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

PRINCIPLES OF OPERATION

THEORY OF OPERATION

The THS415x is a fully differential amplifier. Differential amplifiers are typically *differential in/single out*, whereas fully differential amplifiers are *differential in/differential out*.

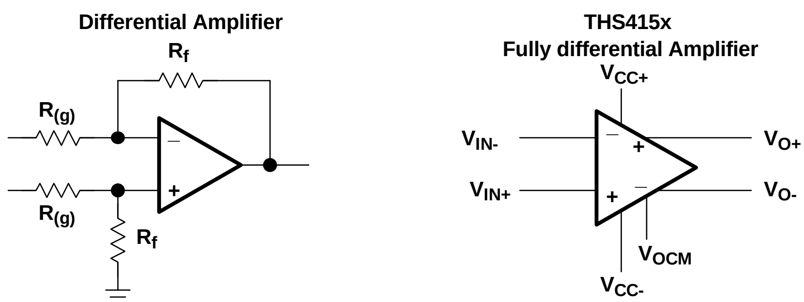


Figure 36. Differential Amplifier Versus a Fully Differential Amplifier

To understand the THS415x fully differential amplifiers, the definition for the pinouts of the amplifier are provided.

PRINCIPLES OF OPERATION (continued)

Input voltage definition $V_{ID} = \left(V_{I+}\right) - \left(V_{I-}\right) \qquad V_{IC} = \dfrac{\left(V_{I+}\right) + \left(V_{I-}\right)}{2}$

Output voltage definition $V_{OD} = \left(V_{O+}\right) - \left(V_{O-}\right) \qquad V_{OC} = \dfrac{\left(V_{O+}\right) + \left(V_{O-}\right)}{2}$

Transfer function $V_{OD} = V_{ID} \times A_{(f)}$

Output common mode voltage $V_{OC} = V_{OCM}$

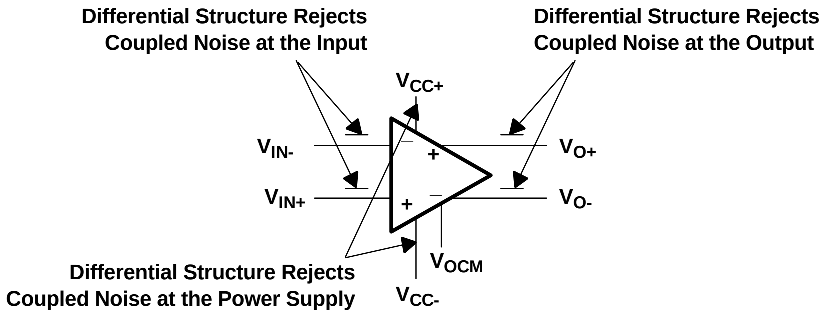
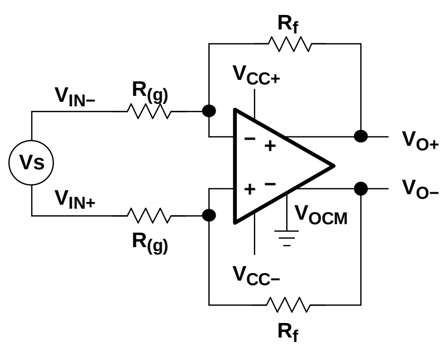


Figure 37. Definition of the Fully Differential Amplifier

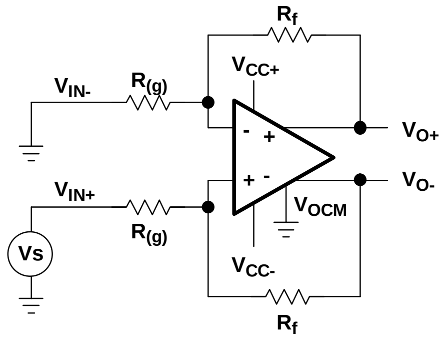
The following schematics depict the differences between the operation of the THS415x, fully differential amplifier, in two different modes. Fully differential amplifiers can work with differential input or can be implemented as single in/differential out.



Note: For proper operation, maintain symmetry by setting $R_f1 = R_f2 = R_f$ and $R_{(g)}1 = R_{(g)}2 = R_{(g)} \Rightarrow A = R_f/R_{(g)}$

Figure 38. Amplifying Differential Signals

PRINCIPLES OF OPERATION (continued)



RECOMMENDED RESISTOR VALUES

GAIN	$R_{(g)}$ Ω	R_f Ω
1	390	390
2	374	750
5	402	2010
10	402	4020

Figure 39. Single In With Differential Out

If each output is measured independently, each output is one-half of the input signal when gain is 1. The following equations express the transfer function for each output:

$$V_{O+} = \frac{V_{I+}}{2} + V_{OCM}$$

The second output is equal and opposite in sign:

$$V_{O-} = \frac{-V_{I+}}{2} + V_{OCM}$$

V_{OCM} will be set to midrails if it is not derived by any external power source.

Fully differential amplifiers may be viewed as two inverting amplifiers. In this case, the equation of an inverting amplifier holds true for gain calculations. One advantage of fully differential amplifiers is that they offer twice as much dynamic range compared to single-ended amplifiers. For example, a 1-V_{PP} ADC can only support an input signal of 1 V_{PP}. If the output of the amplifier is 2 V_{PP}, then it will not be practical to feed a 2-V_{PP} signal into the targeted ADC. Using a fully differential amplifier enables the user to break down the output into two 1-V_{PP} signals with opposite signs and feed them into the differential input nodes of the ADC. In practice, the designer has been able to feed a 2-V peak-to-peak signal into a 1-V differential ADC with the help of a fully differential amplifier. The final result indicates twice as much dynamic range.

Figure 40 illustrates the increase in dynamic range. The gain factor should be considered in this scenario. The THS415x fully differential amplifier offers an improved CMRR and PSRR due to its symmetrical input and output. Furthermore, second harmonic distortion is improved. Second harmonics tend to cancel because of the symmetrical output.

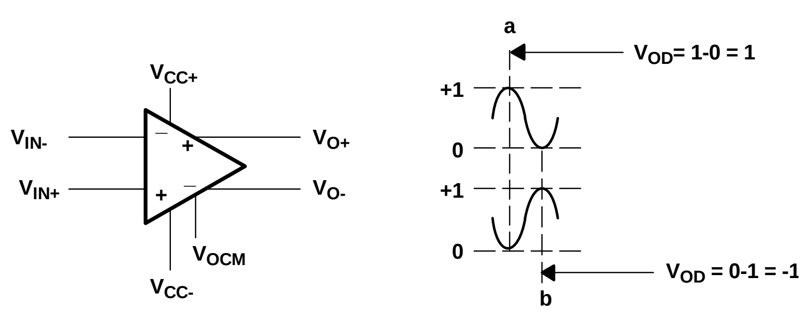


Figure 40. Fully Differential Amplifier With Two 1-V_{PP} Signals

Similar to the standard inverting amplifier configuration, input impedance of a fully differential amplifier is selected by the input resistor, $R_{(g)}$. If input impedance is a constraint in design, the designer may choose to implement the differential amplifier as an instrumentation amplifier. This configuration improves the input impedance of the fully differential amplifier. The following schematic depicts the general format of instrumentation amplifiers.

PRINCIPLES OF OPERATION (continued)

The general transfer function for this circuit is:

$$\frac{V_{OD}}{V_{IN1}-V_{IN2}} = \frac{R_f}{R_{(g)}}\left(1 + \frac{2R2}{R1}\right)$$

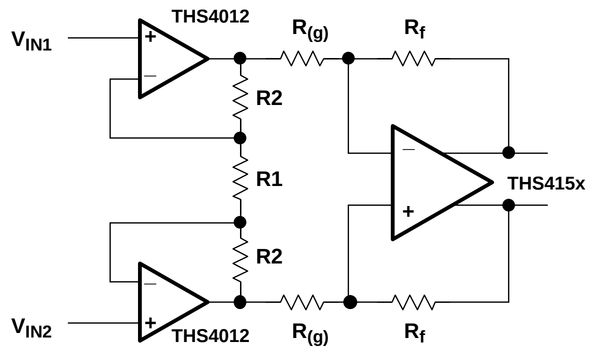


Figure 41. Fully Differential Instrumentation Amplifier

CIRCUIT LAYOUT CONSIDERATIONS

To achieve the levels of high frequency performance of the THS415x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS415x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

PRINCIPLES OF OPERATION (continued)

POWER-DOWN MODE

The power-down mode is used when power saving is required. The power-down terminal ($\overline{PD}$) found on the THS415x is an active low terminal. If it is left as a no-connect terminal, the device will always stay on due to an internal 50 kΩ resistor to V_{CC}. The threshold voltage for this terminal is approximately 1.4 V above V_{CC-}. This means that if the $\overline{PD}$ terminal is 1.4 V above V_{CC-}, the device is active. If the $\overline{PD}$ terminal is less than 1.4 V above V_{CC-}, the device is off. For example, if V_{CC-} = –5 V, then the device is on when PD reaches 3.6 V, (–5 V + 1.4 V = -3.6 V). By the same calculation, the device is off below –3.6 V. It is recommended to pull the terminal to V_{CC-} in order to turn the device off. The following graph shows the simplified version of the power-down circuit. While in the power-down state, the amplifier goes into a high-impedance state. The amplifier output impedance is typically greater than 1 MΩ in the power-down state.

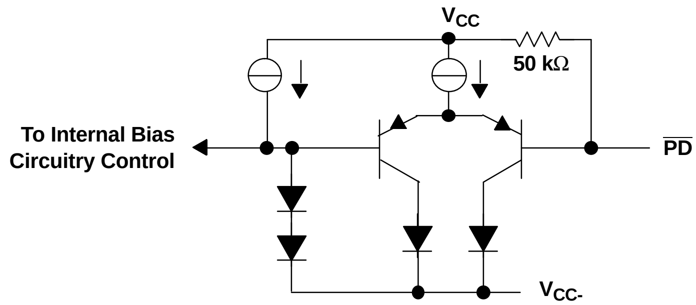


Figure 42. Simplified Power-Down Circuit

Due to the similarity of the standard inverting amplifier configuration, the output impedance appears to be very low while in the power-down state. This is because the feedback resistor (R_f) and the gain resistor ($R_{(g)}$) are still connected to the circuit. Therefore, a current path is allowed between the input of the amplifier and the output of the amplifier. An example of the closed-loop output impedance is shown in Figure 43.

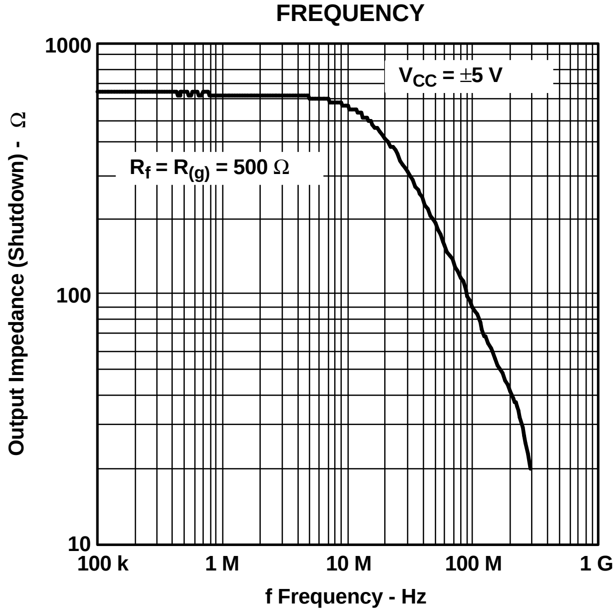


Figure 43.

PRINCIPLES OF OPERATION (continued)

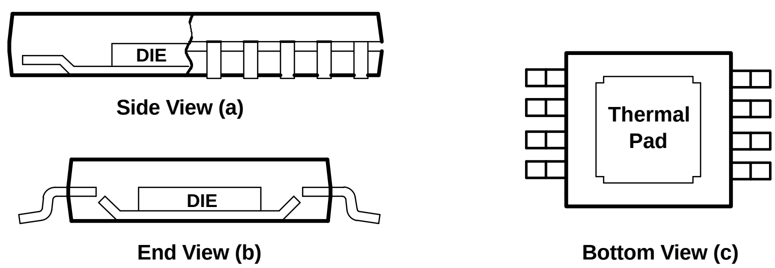
GENERAL PowerPAD DESIGN

The THS415x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 44(a) and Figure 44(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 44(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

More complete details of the PowerPAD™ installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package (SLMA002).* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 44. Views of Thermally Enhanced DGN Package

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
THS4150CD	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150CDGK	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150CDGKG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150CDGKR	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150CDGKRG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150CDGN	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150CDGNR	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150CDGNRG4	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150CDR	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150CDRG4	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150ID	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150IDGK	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150IDGKR	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150IDGKRG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150IDGN	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150IDGNG4	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150IDGNR	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150IDGNRG4	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150IDR	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4150IDRG4	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151CD	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151CDGK	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
THS4151CDGKG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151CDGKR	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151CDGKRG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151CDGN	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151CDGNG4	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151CDGNR	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151CDGNRG4	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151CDR	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151CDRG4	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151ID	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151IDGK	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151IDGKG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151IDGKR	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151IDGKRG4	ACTIVE	MSOP	DGK	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151IDGN	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151IDGNG4	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151IDGNR	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151IDGNRG4	ACTIVE	MSOP-Power PAD	DGN	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151IDR	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4151IDRG4	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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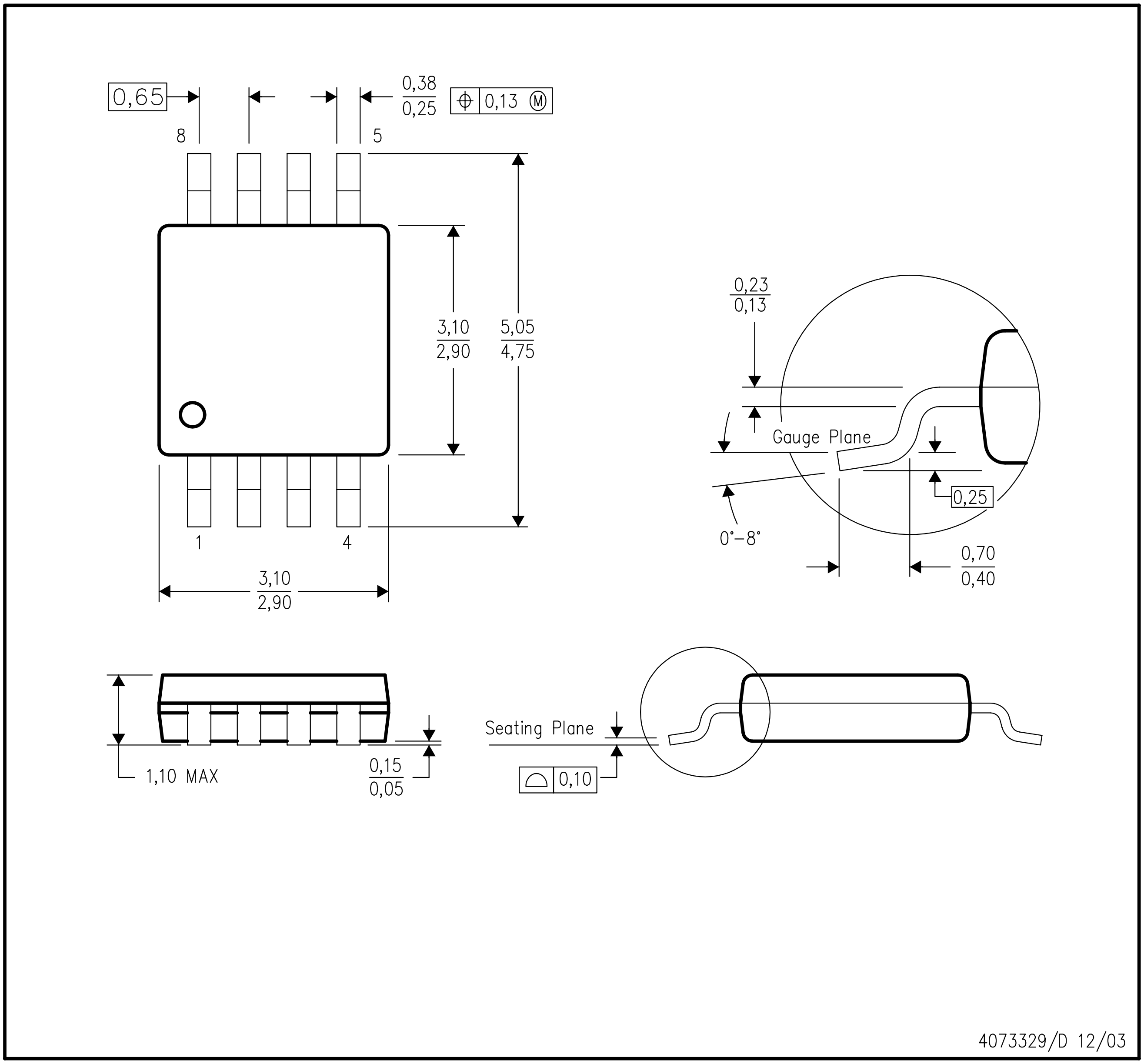
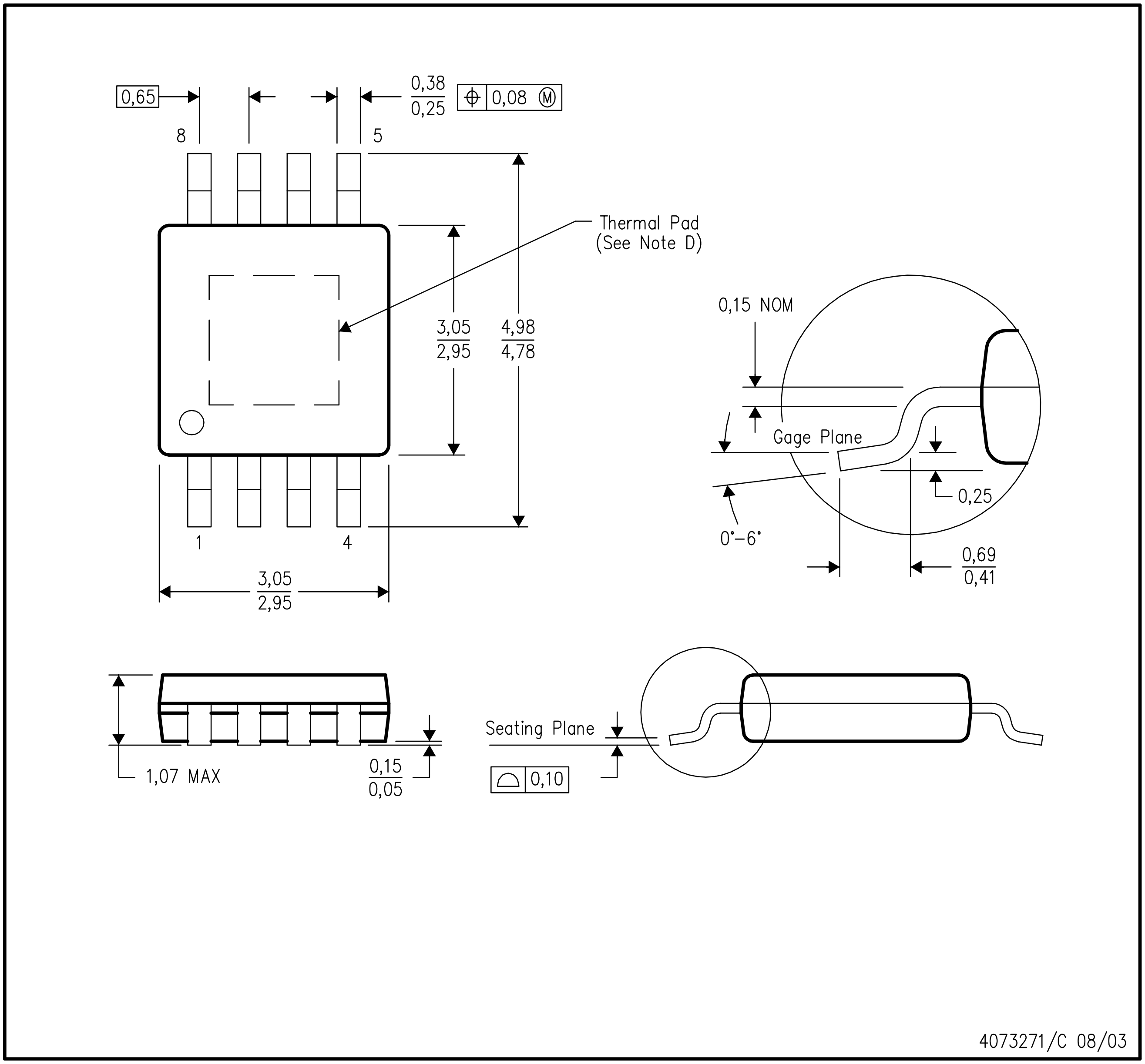
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation AA.

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



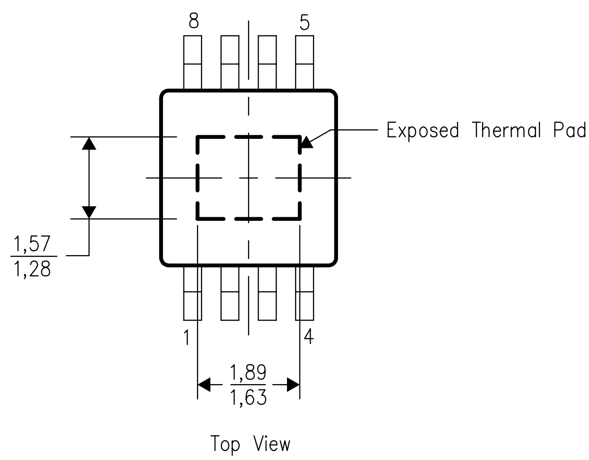
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. Falls within JEDEC MO-187

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

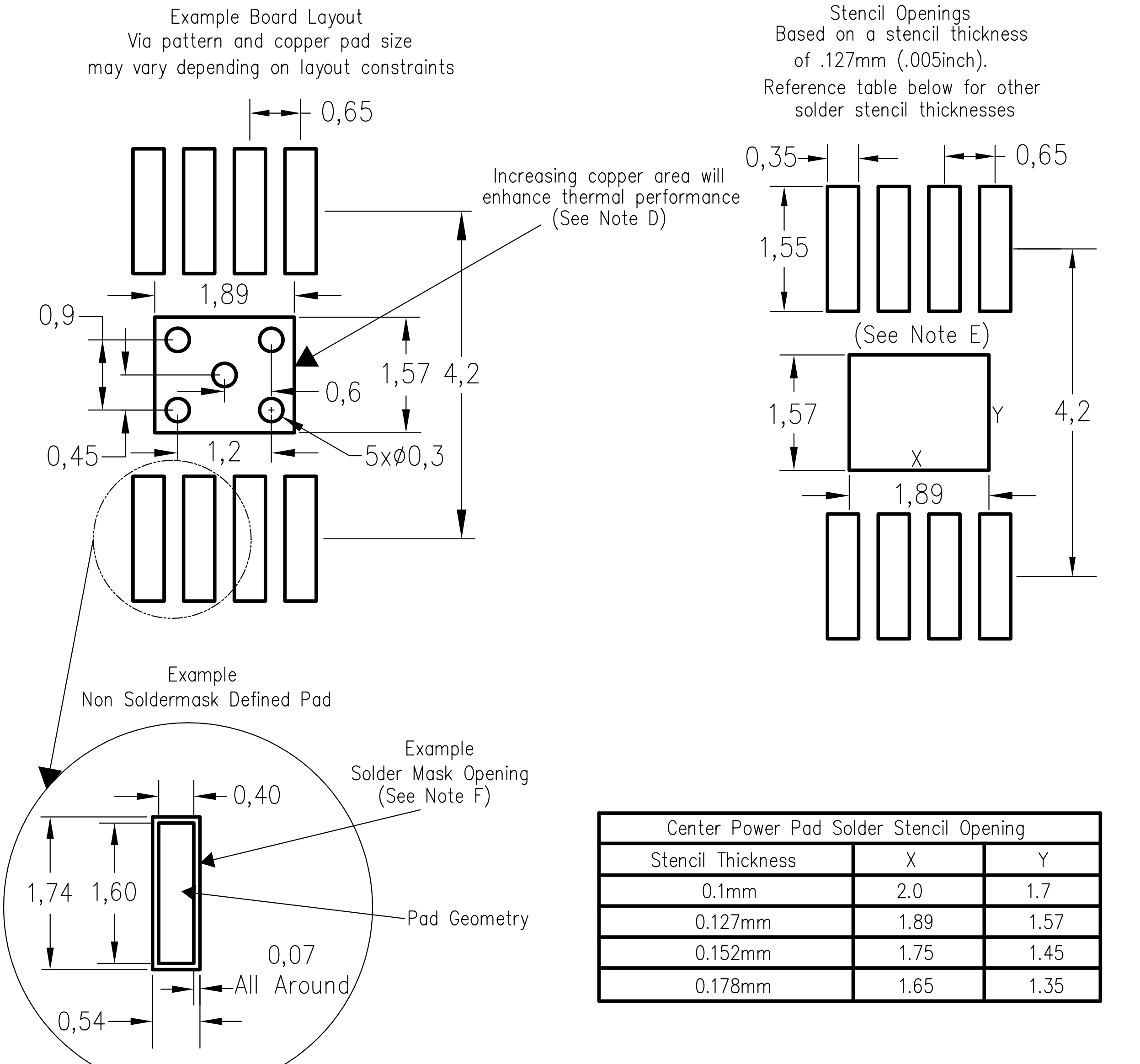
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGN (R–PDSO–G8) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

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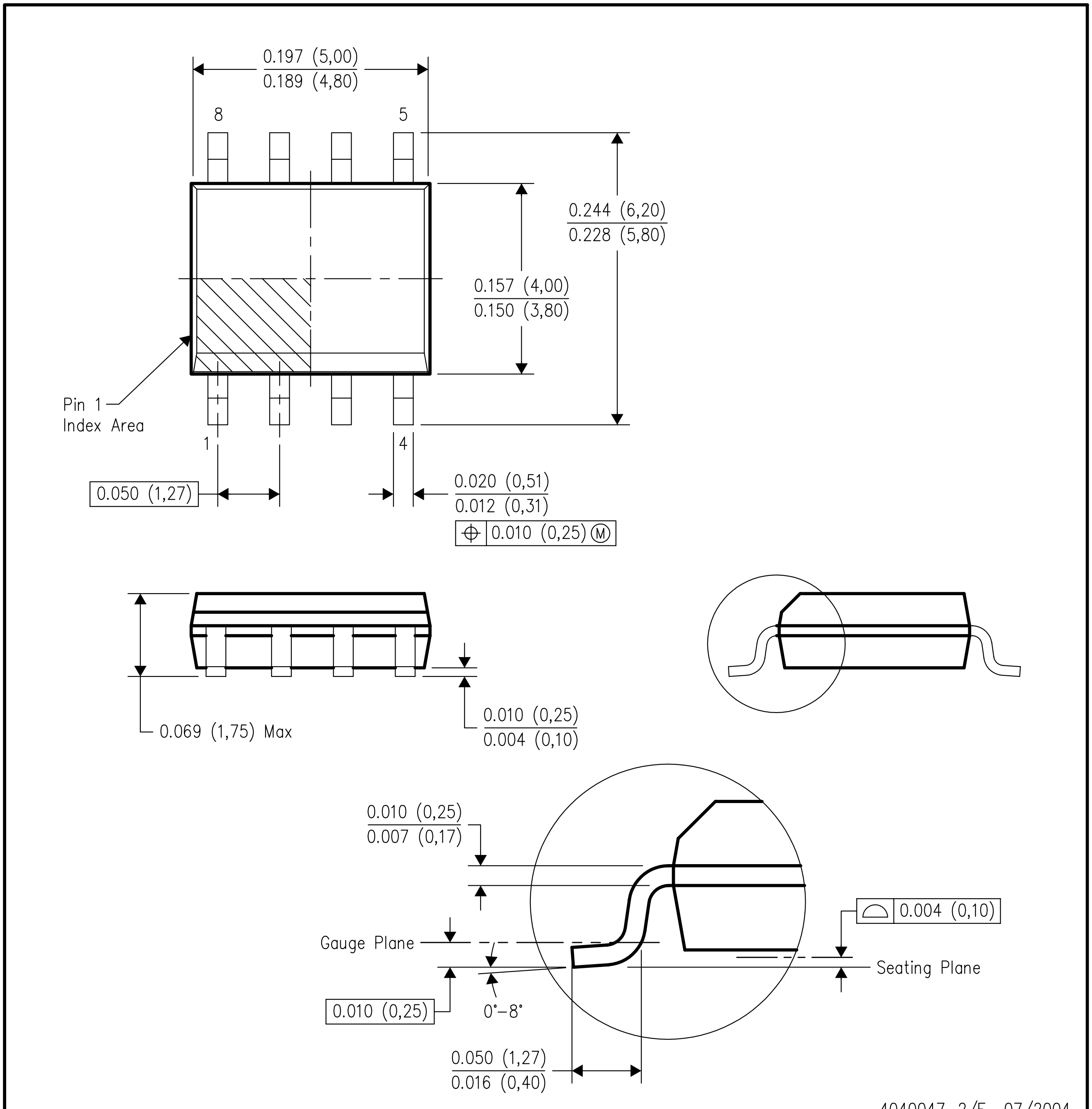
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AA.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265