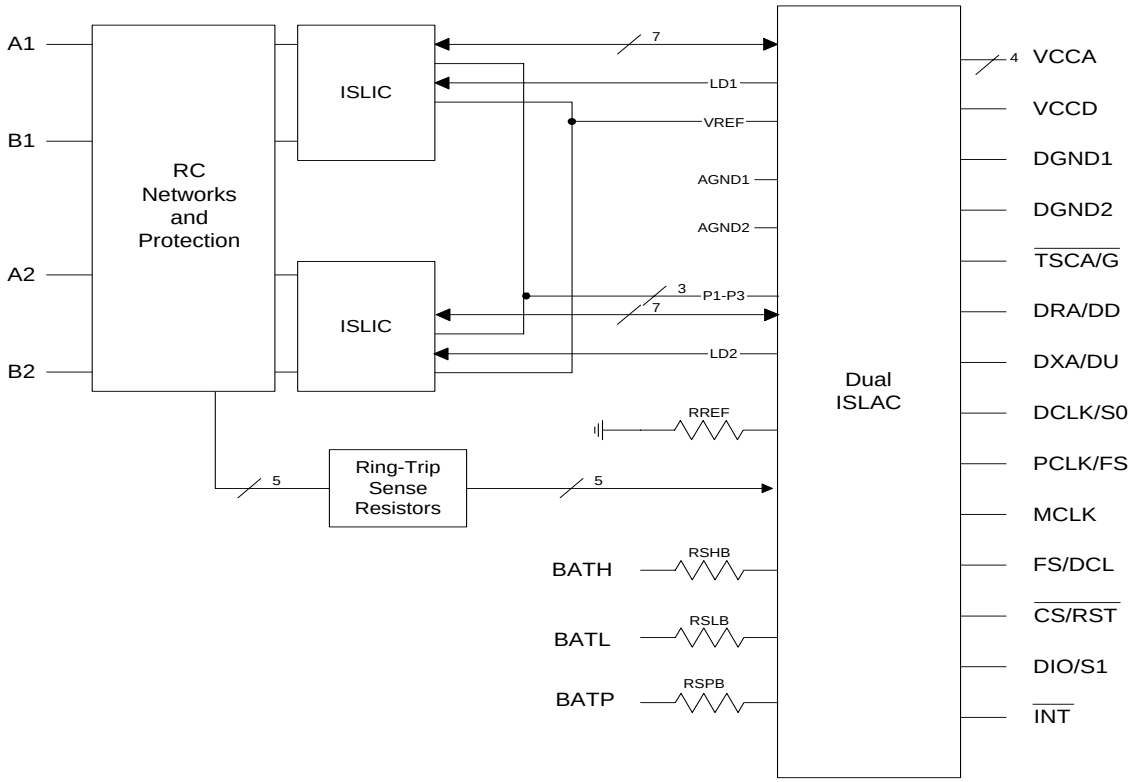
Am79D2251

Dual Intelligent Subscriber Line Audio-Processing Circuit (ISLAC™)

DISTINCTIVE CHARACTERISTICS

- **High performance digital signal processor provides programmable control of all major linecard functions**
  - — 32 and 24 kb/s ADPCM to G726, as well as A-law/μ-law and linear codec
    - — Transmit and receive gain
    - — Two-wire AC impedance
    - — Transhybrid balance
    - — Equalization
  - — DC loop feeding
    - — Smooth or abrupt polarity reversal
  - — Loop supervision
    - — Off-hook debounce circuit
    - — Ground-key and ring-trip filters
  - — Ringing generation and control
  - — Adaptive hybrid balance
  - — Line and circuit testing
  - — Tone generation
  - — Metering generation at 12 kHz and 16 kHz
    - — Envelope shaping and level control
- **Selectable PCM/MPI or GCI digital interfaces**
  - — Supports most available master clock frequencies from 512 kHz to 8.196 MHz
- **0 to 70°C commercial operation**
  - — –40°C to 85°C extended temperature range available
- **+3.3 V DC operation**
- **Exceeds LSSGR and ITU requirements**
- **Supports external ringing with on-chip ring-trip circuit**
  - — Automatic or manual ring-trip modes
- **DTMF detection according to Q.24**
- **2100 Hz modem tone detection according to V.25**

BLOCK DIAGRAM



Pub. # **22829** Rev**: C** Amendment**: /0**
Issue Date: **December 1999**

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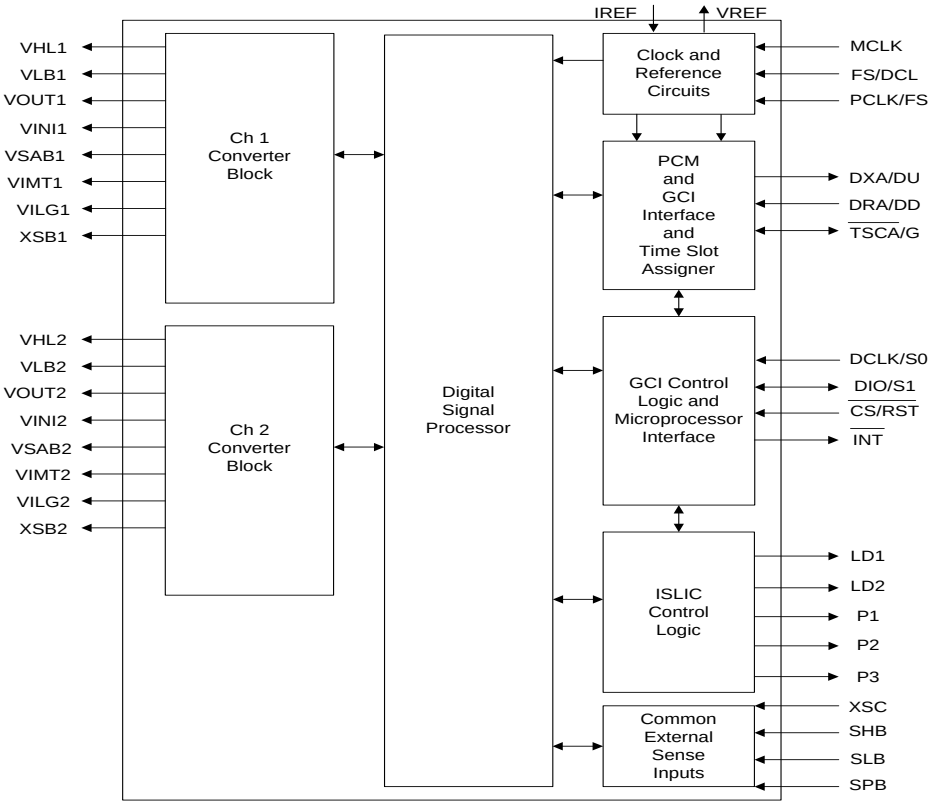
The dual ISLAC™ device, in combination with an ISLIC™ device, implements a two channel universal telephone line interface. This enables the design of a single, low cost, high performance, fully software programmable line interface for multiple country applications worldwide. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces. Additionally, the dual ISLAC device has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

DISTINCTIVE CHARACTERISTICS OF THE INTELLIGENT ACCESS™ VOICE CHIPSET

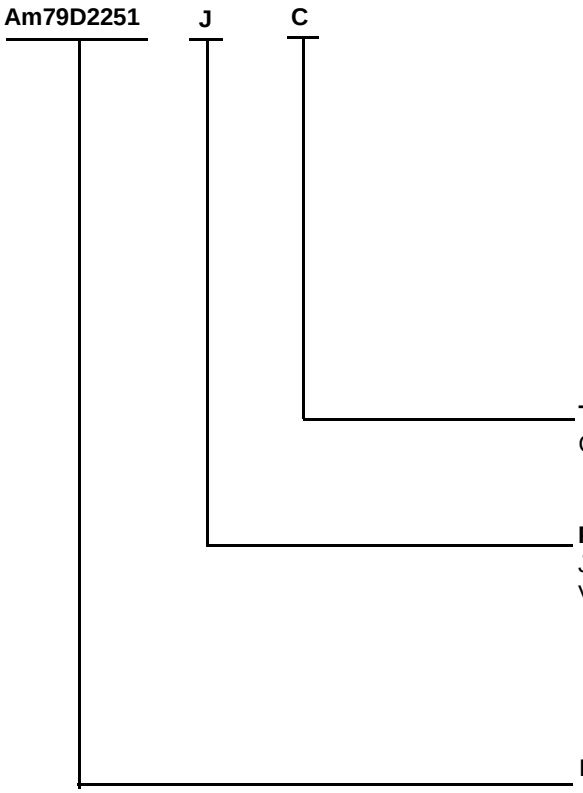
- **Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions**
- **Two chip solution supports high density, multi-channel architecture**
- **Single hardware design meets multiple country requirements through software programming of:**
  - — Ringing waveform and frequency
  - — DC loop-feed characteristics and current-limit
  - — Loop-supervision detection thresholds
    - — Off-hook debounce circuit
    - — Ground-key and ring-trip filters
  - — Off-hook detect de-bounce interval
  - — Two-wire AC impedance
  - — Transhybrid balance
  - — Transmit and receive gains
  - — Equalization
  - — Digital I/O pins
  - — A-law/μ-law and linear selection
- **Supports internal and external battery-backed ringing**
  - — Self-contained ringing generation and control
  - — Supports external ringing generator and ring relay
  - — Ring relay operation synchronized to zero crossings of ringing voltage and current
  - — Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- **Supports metering generation with envelope shaping**
- **Smooth or abrupt polarity reversal**
- **Adaptive transhybrid balance**
  - — Continuous or adapt and freeze
- **Supports both loop-start and ground-start signaling**
- **Exceeds LSSGR and CCITT central office requirements**
- **Selectable PCM or GCI interface**
  - — Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- **On-hook transmission**
- **Power/service denial mode**
- **Line-feed characteristics independent of battery voltage**
- **Only 5 V, 3.3 V and battery supplies needed**
- **Low idle-power per line**
- **Linear power-feed with intelligent power-management feature**
- **Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance**
- **Monitors two-wire interface voltages and currents for subscriber line diagnostics**
- **Built-in voice-path test modes**
- **Power-cross, fault, and foreign voltage detection**
- **Integrated line-test features**
  - — Leakage
  - — Line and ringer capacitance
  - — Loop resistance
- **Integrated self-test features**
  - — Echo gain, distortion, and noise
- **0 to 70°C commercial operation**
  - — –40°C to 85°C extended temperature range available
- **Small physical size**
- **Up to three relay drivers per ISLIC™ device**
  - — Configurable as test load switches

Figure 1. Dual ISLAC™ Block Diagram



ORDERING INFORMATION

AMD standard products are available in several packages and operating ranges. The ordering number (valid combination) is formed by a combination of the elements below. Two ISLIC devices need to be used with this part.



TEMPERATURE RANGE
C= Commercial (0°C to +70°C)

PACKAGE TYPE
J = 44-pin plastic leaded chip carrier (PL044)
V = 44-pin thin plastic quad flat pack (PQT044)

DEVICE NAME/DESCRIPTION
Am79D2251
Advanced Dual Intelligent Subscriber Line Audio-Processing Circuit

Valid Combinations	
Am79D2251	JC
Am79D2251	VC

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

CONNECTION DIAGRAMS

Figure 2. 44-Pin PLCC Connection Diagram

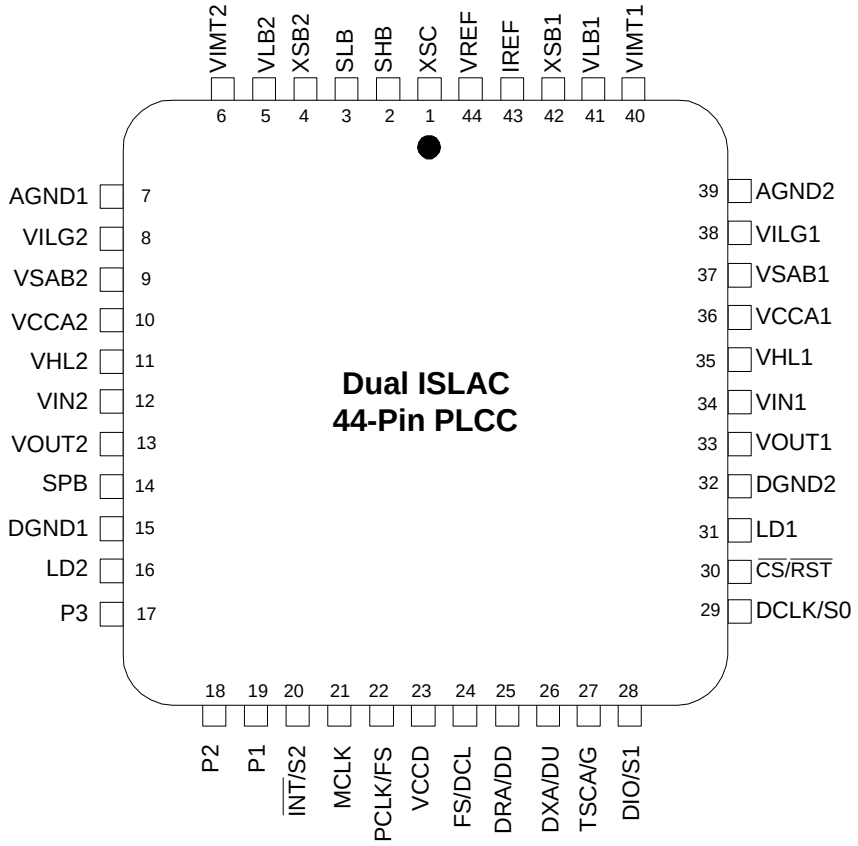
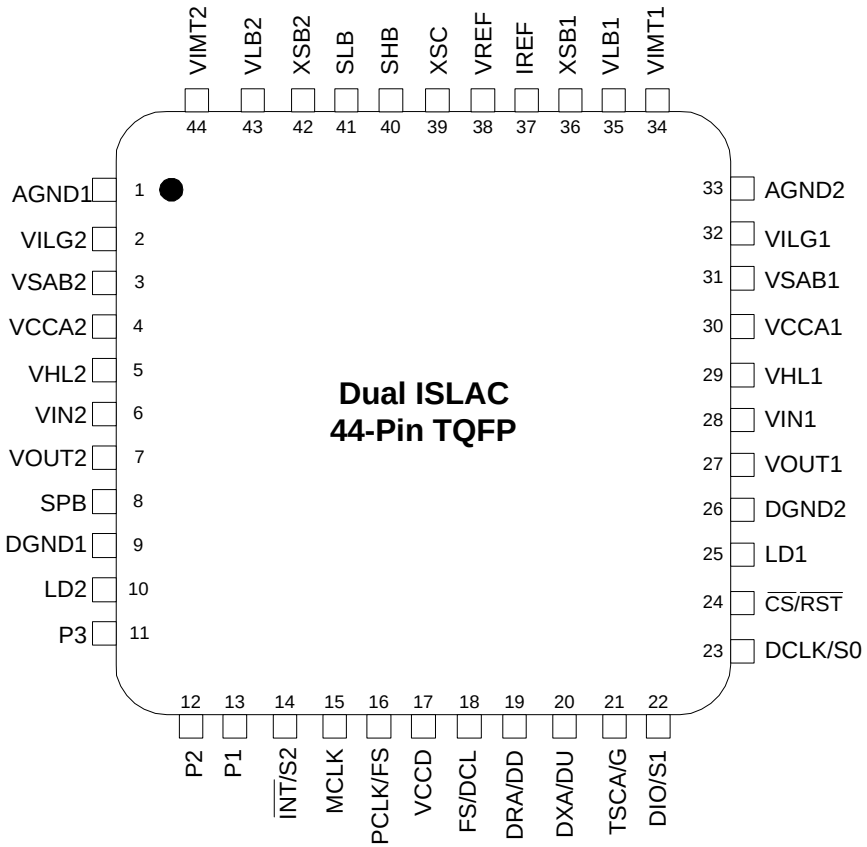


Figure 3. 44-Pin TQFP Connection Diagram



PIN DESCRIPTIONS

Pin	Pin Name	I/O	Description
AGND1, AGND2	Analog Ground	O	Analog circuitry ground returns
DCLK/S0	Data Clock/GCI Address Strap 0	I	Provides data control for MPI interface control. For GCI operation, this pin is device address bit 0. 5 V tolerant.
DGND1–DGND2	Digital Ground		Digital ground returns
DIO/S1	Data I/O/GCI Address Strap 1	I/O	For PCM backplane operation, control data is serially written into and read out of the ISLAC device via the DIO pin with the MSB first. The data clock (DCLK) determines the data rate. DIO is high impedance except when data is being transmitted from the ISLAC device under control of $\overline{CS}/\overline{RST}$. For GCI operation, this pin is device address bit 1. 5 V tolerant.
DRA/DD	RX Path A Backplane Data/ GCI data Downstream, Receive Path B backplane data	I	For the PCM highway, the receive PCM data is input serially through the DRA ports. The data input is received every 125 µs and is shifted in, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. The receive port can receive information for direct control of the ISLIC device. This mode is selected in Device Configuration Register 2 (RTSEN = 1, RTSMD = 1). When selected, this data is received in an independently programmable timeslot from the PCM data. For the GCI mode, downstream receive and control data is accepted on this pin. 5 V tolerant.
DXA/DU	TX Path A Backplane Data/GCI Data Upstream, TX Path B Backplane Data	O	For the PCM highway, the transmit PCM data is transmitted serially through the DXA port. The transmission data output is available every 125 µs and is shifted out, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. DXA is high impedance between bursts and while the device is in the inactive mode. Can also select a mode (RTSEN = 1, RTSMD = 1 or 0 in Device Configuration Register 2) that transmits the Signaling Register MSB contents first, in an independently programmable timeslot from the PCM data. This data is transmitted in all modes except disconnect. For the GCI mode, upstream transmit and signaling data is transferred on this pin. 5 V tolerant.
FS/DCL	Frame sync/GCI Downstream Clock	I	For PCM operation, pin is Frame Sync. PCM operation is selected by the presence of an 8 kHz Frame Sync signal on this pin in conjunction with the PCLK on the PCLK/FS pin (see below). This 8 kHz pulse identifies the beginning of a frame. The ISLAC device references individual timeslots with respect to this input, which must be synchronized to PCLK. GCI operation is selected by the presence of the downstream clock DCL, on this pin in conjunction with the presence of a FS on the PCLK/FS pin. In GCI mode, the rate at which data is shifted into or out of the PCM ports is a derivative of this DCL clock as selected in Device Configuration Register 1. 5 V tolerant.
$\overline{INT}/\overline{S2}$	Interrupt/GCI Address Strap 2	O	For PCM operation, when a subscriber line requires service, this pin goes to a logic 0 to interrupt a higher level processor. Several registers work together to control operation of the interrupt: Signaling and Global Interrupt Registers with their associated Mask Registers, and the Interrupt Register. See the description at configuration register 6 (Mask) for operation. Logic drive is selectable between open drain and TTL-compatible outputs. The S2 function is only available on the dual ISLAC device. For GCI operation, it is the device address bit 2.
IREF	Current Reference	I	External resistor (RREF) connected between this pin and analog ground generates an accurate, on-chip reference current for the A/D's and D/A's on the ISLAC chip.
LD1–LD2	Register Load	O	The LD pins output 3-level voltages. When LDn is a logic 0, the destination of the code on P1–P3 is the relay control latches in the ISLIC control register. When LDn is a logic 1, the destination of P1–P3 is the mode control latches. LDn is driven to VREF when the contents of the ISLIC control register must not change.
MCLK	Master Clock	I	For PCM backplane operation, a DSP master clock connects here. A signal is required only for PCM backplane operation when PCLK is not used as the master clock. MCLK can be a wide variety of frequencies. Upon initialization the MCLK input is disabled, and relevant circuitry is driven by a connection to PCLK. The MCLK connection may be re-established under user control. 5 V tolerant.
PCLK/FS	PCM Clock/Frame Sync	I	For PCM operation, this is PCM Clock. PCM operation is selected by the presence of a PCLK signal on this pin in conjunction with the FS on the FS/DCL pin (see below). For PCM backplane operation, connect a data clock, which determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK can be any multiple of the FS frequency. The minimum clock frequency for linear/ companded data plus signaling data is 256 kHz. For GCI operation, this pin is Frame Sync. The FS signal is an 8 kHz pulse that identifies the beginning of a frame. The ISLAC device references individual timeslots with respect to this input, which must be synchronized to DCL. 5 V tolerant.
P1–P3	ISLIC Control	O	Control the operating modes of the two ISLIC devices connected to the dual ISLAC device.

Pin	Pin Name	I/O	Description
$\overline{CS}/\overline{RST}$	Chip Select/Reset	I	For PCM backplane operation, a logic low on this pin for 15 or more DCLK cycles resets the sequential logic in the ISLAC device into a known mode. A logic low placed on this pin for less than 15 DCLK cycles is a chip select and enables serial data transmission into or out of the DIO port. For GCI operation, a logic low on this pin—for 1 ms or longer—resets the sequential logic into a known mode. See Table 2-4 in the Technical Reference for details. 5 V tolerant.
SHB, SLB, SPB	Battery Sense	I	Resistors that sense the high, low and positive battery voltages connect here. If only one negative battery is used, connect both resistors at the supply. If the positive battery is not used, leave the pin unconnected. These pins are current inputs whose voltage is held at VREF.
$\overline{TSCA}$/G,	Timeslot Control A/GCI Mode, Time Slot Control B	O (PCM) I (GCI)	For PCM backplane operation, $\overline{TSCA}$ is active low when PCM data is output on the DXA pin. The outputs are open-drain and are normally inactive (high impedance). Pull-up loads should be connected to VCCD. When GCI mode is selected, one of two GCI modes may be selected by connecting $\overline{TSCA}$/G to DGND or VCCD.
VSAB1–VSAB2	Loop voltage sense	I	Connect to the VSAB pins of two ISLIC devices.
VCCA1–VCCA2	Power Supply		+3.3 VDC supplies to the analog sections in each of the two channels.
VCCD	Power Supply		+3.3 VDC supply to all digital sections.
VREF	Analog Reference	O	This pin provides a 1.4 V, single-ended reference to the two ISLIC devices to which the ISLAC device is connected.
VHL1–VHL2	High Level D/A	O	High-level loop control voltages on these pins are used to control DC-feed, internal ringing, metering and polarity reversal for each ISLIC device.
VIN1–VIN2	TX Analog	I	Analog transmit signals (VTX) from each ISLIC device connect to these pins. The ISLAC device converts these signals to digital words and processes them. After processing, they are multiplexed into serial time slots and sent out of the DXA/DU pin.
VLB1–VLB2	Longitudinal Reference	O	Normally connected to VCCA internally. They supply longitudinal reference voltages to the ISLIC devices during certain test procedures. These outputs are connected internally to VCCA during ISLIC Active, Standby, Ringing, and Disconnect modes. During test modes, it can be connected to the receive D/A.
VIMT1–VIMT2, VILG1–VILG2	Sense	I	The IMT and ILG pins of two ISLIC devices connect to the VIMT1–VIMT4 and VILG1–VILG4 pins of the ISLAC chip. These pins are voltage inputs referenced to VREF. They require external resistors connected between each pin and VREF to convert IMTn and ILGn into voltages.
VOUT1–VOUT2	RX Analog	O	The ISLAC device extracts and processes voice data from time slots on DRA/DD serial data port. After processing, the ISLAC device converts the voice data to analog signals that are sent out of these pins to each respective ISLIC device.
XSB1–XSB2	External Sense	I	External resistors connect here that sense an external voltage. In a linecard with external ringing, they are used to sense the voltage at the line side of the ring-feed resistor. These pins are current inputs whose voltage is held at VREF. An internal resistor converts currents flowing in these pins into voltages to be sampled by the A/D.
XSC	Common External Sense	I	An external resistor connects here that senses a common reference for external voltages sensed by resistors connected to XSB1–XSB4. This pin is a current input whose voltage is held at VREF. An internal resistor converts current flowing in this pin into a voltage to be sampled by the A/D. This pin is intended for sensing external ringer supply voltages. However, it can also be used to sense other test points when internal ringing is used.

GENERAL DESCRIPTION

The Intelligent Access™ voice chipsets integrate all functions of the subscriber line for two subscriber lines. One or more of two chip types are used to implement the linecard; an ISLIC device and a dual ISLAC device. These provide the following basic functions:

1. The ISLIC device: A high voltage, bipolar IC that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The dual ISLAC device: A low voltage CMOS IC that provides conversion and DSP functions for 2 channels.

Complete schematics of linecards using the Intelligent Access voice chipsets for internal and external ringing are shown in Figure 4 and Figure 5.

The ISLIC device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the ISLAC device to operate in eight different modes that control power consumption and signaling modes. This enables it to have full control over the subscriber loop. The ISLIC device is customized to be used exclusively with the ISLAC device as part of a multiple-line chipset. The ISLIC device requires only +5 V power and the battery supplies for its operation.

The ISLIC device implements a linear loop-current feeding method with the enhancement of intelligent thermal management in a controlled manner. This limits the amount of power dissipated on the ISLIC chip by dissipating excess power in external resistors.

Each ISLAC device contains high-performance codec circuits that provide A/D and D/A conversion for voice (codec), DC-feed and supervision signals for two subscriber channels. The ISLAC device contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for both channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Intelligent Access voice chipset provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chipsets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide linecard requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with the WinSLAC™ software. This PC software is provided free of charge. It allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The ISLIC interface unit inside the ISLAC device processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the ISLAC device to place several key ISLIC performance parameters under software control.

The main functions that can be observed and/or controlled through the ISLAC backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- DTMF detection
- Modem tone (2100 Hz) detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth battery reversal
- Subscriber line matching
- Ringing generation
- Sophisticated line and circuit tests

To accomplish these functions, the ISLIC device collects the following information and feeds it, in analog form, to the ISLAC device:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltage

The outputs supplied by the ISLAC device to the ISLIC device are then:

- A voltage (VHLi) that provides control for the following high-level ISLIC device outputs:
  - —DC loop current
  - —Internal ringing signal
  - —12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal (VOUTi)
- A voltage that controls longitudinal offset for test purposes (VLBi)

The ISLAC device performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law, with the further option of 32 or 24 kb/s ADPCM compression.

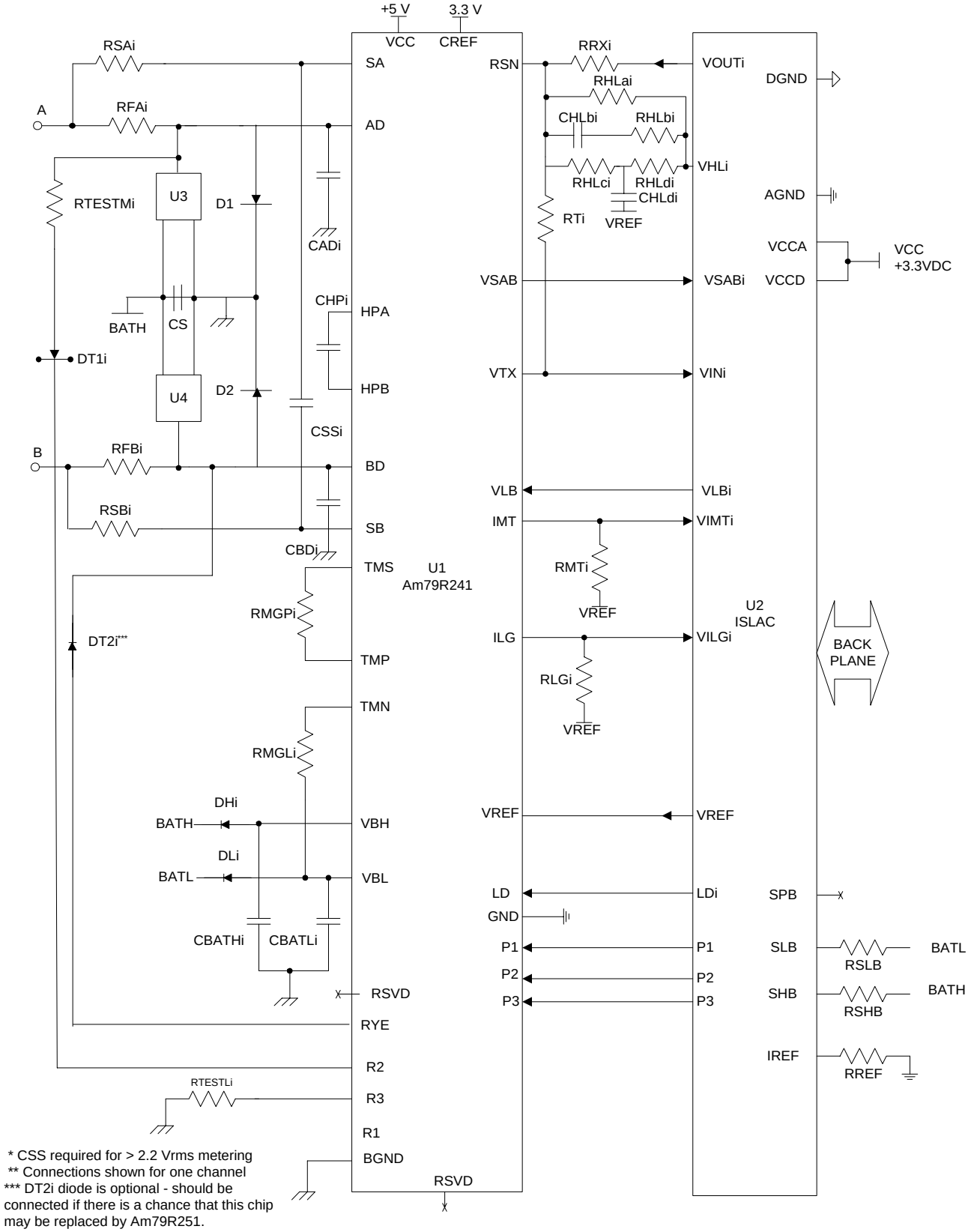
Besides the codec functions, the Intelligent Access voice chipset provides all the sensing, feedback, and clocking necessary to completely control ISLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The ISLAC device supplies complete mode control to the ISLIC device using the control bus (P1-P3) and tri-level load signal (LDi).

The Intelligent Access voice chipset provides extensive loop supervision capability including off-hook, DTMF, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

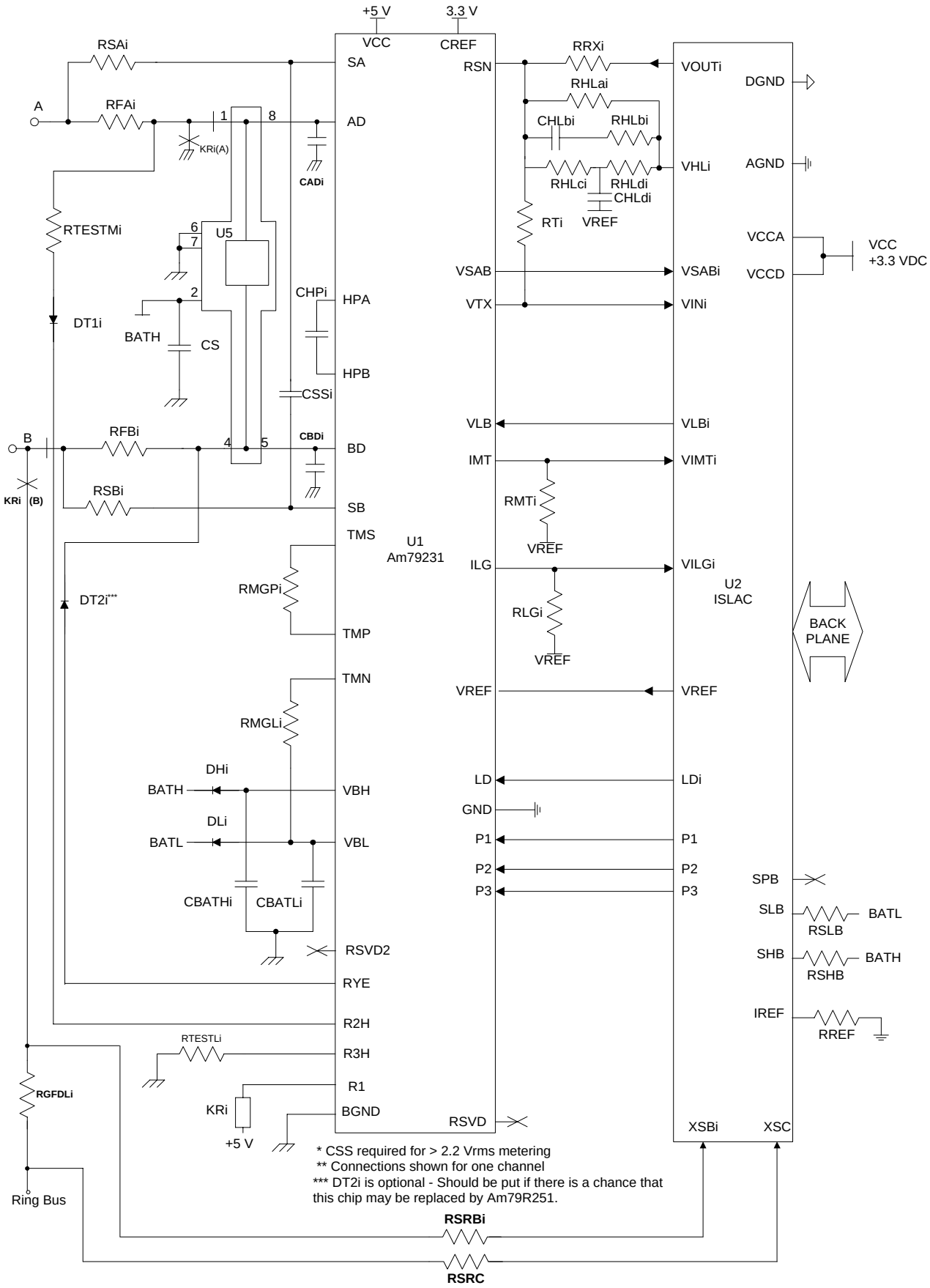
For subscriber line diagnostics, AC and DC line conditions can be monitored using built in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the actual PCM measurement data directly to a higher level processor by way of the voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

Figure 4. Internal Ringing Linecard Schematic



* CSS required for > 2.2 Vrms metering
** Connections shown for one channel
*** DT2i diode is optional - should be connected if there is a chance that this chip may be replaced by Am79R251.

Figure 5. External Ringing Linecard Schematic



LINECARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the linecard (i = 1, 2)

Item	Type	Value	Tol.	Rating	Comments
U1	Am79R241				ISLIC device
U2	Am79X22xx				ISLAC device
U3, U4	P1001SC			100 V	TECCOR Battrax protector
U5	TISP61089			80 V	Transient Voltage Suppresser, Power Innovations
D1, D2	Diode	1 A		100 V	
DHi, DLi, DT1i, DT2i[4]	Diode	100 mA		100 V	50 ns
RFAi, RFBi	Resistor	50 Ω	2%	2 W	Fusible PTC protection resistors
RSAi, RSBi	Resistor	200 kΩ	2%	1/4 W	Sense resistors
RTi	Resistor	80.6 kΩ	1%	1/8 W	
RRXi	Resistor	100 kΩ	1%	1/8 W	
RREF	Resistor	69.8 kΩ	1%	1/8 W	Current reference
RMGLi, RMGPi	Resistor	1 kΩ	5%	1 W	Thermal management resistors
RSHB, RSLB	Resistor	750 kΩ	1%	1/8 W	
RHLai	Resistor	40.2 kΩ	1%	1/10 W	
RHLbi	Resistor	4.32 kΩ	1%	1/10 W	
RHLci	Resistor	2.87 kΩ	1%	1/10 W	
RHLdi	Resistor	2.87 kΩ	1%	1/10 W	
CHLbi	Capacitor	3.3 nF	10 %	10 V	Not Polarized
CHLdi	Capacitor	0.82 µF	10 %	10 V	Ceramic
RMTi	Resistor	3.01 kΩ	1%	1/8 W	
RLGi	Resistor	6.04 kΩ	1%	1/8 W	
RTESTMi	Resistor	2 kΩ	1%	1 W	Metallic test
RTESTLi	Resistor	2 kΩ	1%	1 W	Longitudinal test
CADi, CBDi [1]	Capacitor	22 nF	10%	100 V	Ceramic, not voltage sensitive
CBATHi, CBATLi	Capacitor	100 nF	20%	100 V	Ceramic
CHPi	Capacitor	22 nF	20%	100 V	Ceramic
CSi[1]	Capacitor	100 nF	20%	100 V	Protector speed up capacitor
CSSi[3]	Capacitor	56 pF	5%	100 V	Ceramic
Components for External Ringing					
RGFDi	Resistor	510 Ω	2%	2 W	1.2 W typ
RSRBi, RSRc	Resistor	750 kΩ	2%	1/4 W	Matched to within 0.2% for initial tolerance and 0 to 70° C ambient temperature range.[2] 17 mW typ
KRi	Relay	5 V Coil			DPDT

Notes:

1. *Value can be adjusted to suit application.*
2. *Can be looser for relaxed ring-trip requirements. 1% match (each resistor ±1%) gives 1.275 mA uncertainty in ringing current sensing.*
3. *Required for metering > 2.5 Vrms, otherwise may be omitted.*
4. *DT2i is optional - Should be put if there is a chance that this chip may be replaced by Am79R251.*

ELECTRICAL CHARACTERISTICS

Power Dissipation

Description	Test Conditions	Min	Typ	Max	Unit
Dual ISLAC Power Dissipation	One channel activated		TBD	TBD	mW
	All channels active		TBD	TBD	
	All channels inactive			TBD	

Absolute Maximum Ratings

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	$-60°C \le T_A \le +125°C$
Ambient Temperature, under Bias	$-40°C \le T_A \le +85°C$
Ambient relative humidity (non condensing)	5 to 100%
V_{CCA} with respect to DGND	–0.4 V to + 3.47 V
V_{CCD} with respect to DGND	–0.4 V to + 3.47 V
V_{IN} with respect to DGND	–0.4 V to VCCA + 0.4 V
5 V tolerant pins	–0.4 to Vcc + 2.25 or 5.25 V, whichever is less
AGND	DGND ±0.4 V
Latch up immunity (any pin)	±100 mA
Any other pin with respect to DGND	–0.4 V to V_{CC}

Operating Ranges

Operating ranges define those limits over which the functionality of the device is guaranteed by 100 percent production testing. Specifications outside of the 0 to 70°C range (–40 to 85°C) are guaranteed through characterization and sample-lot testing production devices at the temperature extremes.

Intelligent Access™ Voice Chipsets Environmental Ranges

Ambient Temperature	–40 to +85°C Commercial
Ambient Relative Humidity	15 to 85%

Electrical Maximum Ranges

Analog Supply V_{CCA}	+3.3 V ± 5%
Digital Supply V_{CCD}	+3.3 V ± 5%
DGND	0 V
AGND	DGND ±50 mV

PERFORMANCE SPECIFICATIONS

The performance targets defined in this section are for the entire linecard comprised of both chips in the Intelligent Access voice chipsets unless otherwise noted. Specifications for the individual chips in the set will be published separately (see note 1). T_A = 0 to 70°C unless otherwise noted.

Intelligent Access™ Voice Chipsets System Target Specifications

Item	Condition	Min	Typ	Max	Unit	Note
Peak Ringing Voltage	Active Ringing mode, RLOAD = 1500 Ω, VBH = 80 V		70		V	
Output Impedance during internal ringing	Active Ringing mode, Dual ISLAC generating internal ringing		200		Ω	
Sinusoidal Ringing THD	Active Ringing mode, RLOAD = 1500 Ω, VBH = 80 V, ISLAC generating internal sinusoidal ringing		2		%	
PSRR (VBH, VBL)	Loop open, in anti-sat f = 50 Hz f = 200 to 3400 Hz	 2 12			dB	1, 2

Notes:

1. *Not tested or partially-tested in production.*
2. *These numbers are only valid when an ISLIC device operates with an ISLAC device, because the ISLAC generates the anti-sat feed characteristic. When the Intelligent Access voice chipsets operate in the normal feed region, the performance is controlled by the ISLIC device. See appropriate ISLIC data sheet for specific PSRR.*

DC Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Input Low Voltage, All other digital inputs		–0.05 –0.50		1.36 V 0.80 V	V	
2	Input High Voltage, All other digital inputs		2.36 2.0		Vcc+0.4 5.25		
4	Input Leakage Current All digital inputs except MCLK MCLK		–10 –120		+10 +180	µA	
5	Input hysteresis (PCLK/FS, FS/DCL, MCLK, DIO, DRA)		0.15	0.225	0.3	V	2
6	Ternary output voltages, LD1–2 High voltage Low voltage Output current	 Iout = ±200 µA Iout = 2 mA Mid level	 VCC–0.45 — –10		 — 0.4 +10	 V V µA	
7	Output Low Voltage (DXA/DU, DIO, $\overline{INT}$, $\overline{TSCA}$)	Iol = 2 mA			0.4		
8	Output Low Voltage ($\overline{INT}$, $\overline{TSCA}$)	Iol = 10 mA			1.0	V	
9	Output High Voltage (All digital outputs except $\overline{INT}$ in open drain mode and $\overline{TSCA}$)	Ioh = 400 µA	VCC–0.4				
10	Input Leakage Current (VIN1–2, VSAB1–2, VILG1–2, VIMT1–2)			TBD		µA	
11	Input Leakage Current (VSAB1–2)			TBD		µA	
12	Input voltage (VIN1–2) µ-law A-law	 3.205 dBm0 3.14 dBm0 to insertion loss in ADC	 VREF –1.02		 VREF +1.02	V	
13	Input Voltage (VSAB 1–2 or VIMT1–2 or VILG1–2)	|Vov–VREF| where Vov is input overload voltage	0.99	1.02	1.05		
14	Offset voltage allowed on VIN1–2		–50		+50	mV	9
15	VHL output offset voltage						
16	VOUT1–2 offset Voltage	DISN off DISN on	–40 –80		+40 +80		
17	Output voltage, VREF	Load current = 0 to 10 mA Source or Sink		1.4		V	
18	Capacitance load on VREF or VOUT1–2				200	pF	2
19	Output drive current, VOUT1–2 or VLB1–2	Source or Sink	–1		+1	mA	2
20	Output leakage current VOUT1–2 or VLB1–2			TBD		mA	
21	Maximum output voltage on VOUT	|VOUT–VREF| with peak digital input	0.99	1.02	1.05	V	9
22	VLB1–2 operating voltage	Source current < 250 µA or sink current < 25 µA.	VREF –1.02		VREF +1.02		
23	Maximum output voltage on VHL (KRFB)	|VHL–VREF| with peak digital input	0.97	1.00	1.03	V	9
24	Gain from VSAB to VHL	VFD = 1	4.9	5	5.1	V/V	
25	Gain from VSAB to VHL	VFD = 0	–0.0255	–0.025	–0.0245	V/V	
26	% error of VLB voltage (For VLB equation, see *Am79R2xx/ Am79D2251 Technical Reference*)		–5		+5	%	
27	Capacitance load on VLB1–2				120	pF	5

No.	Item	Condition	Min	Typ	Max	Unit	Note
28	Capacitance load on XSB1–2, XSC				400	pF	5

Transmission and Signaling Specifications

Table 1. 0 dBm0 Voltage Definitions with Unity Gain in X, R, GX, GR, AX, and AR

Signal at Digital Interface	Transmit	Receive	Unit
A-law digital mW or equivalent (0 dBm0)	0.5026	0.5026	Vrms
μ-law digital mW or equivalent (0 dBm0)	0.4987	0.4987	
±5,800 peak linear coded sine wave	0.5026	0.5025	

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Insertion Loss A-D D-A A-D + D-A A-D + D-A	Input: 1014Hz, –10dBm0 RG = AR = AX = GR = GX = 0 dB, AISN, R, X, B and Z filters disabled Temperature = 70°C Variation over temperature	 –0.25 –0.25 –0.15 –0.1	 0 0 0 0	 +0.25 +0.25 +0.015 +0.1	dB	6
2	Level set error (Error between setting and actual value)	A-D AX + GX D-A AR + GR	–0.1		0.1		
3	DR to DX gain in full digital loopback mode	DR Input: 1014 Hz, –10 dBm0 RG=AR=AX=GR=GX=0 dB, DISN, R, X, B and Z filters disabled	–0.3		+0.3		
4	Idle Channel Noise, Psophometric Weighted (A-law)	Off-hook and On-hook AX = 0dB AR = 0dB A-D (PCM output) D-A (V_{OUT})			 –69 –78	dBm0p	11
5	Idle Channel Noise, C Message weighted (μ-law)	Off-hook and On-hook AX = 0dB AR = 0dB A-D (PCM output) D-A (V_{OUT})			 +19 +12	dBrnC0	11
6	Coder Offset decision value, Xn	A-D, Input signal = 0V	–7		+7	Bits	5
7	GX step size	0 ≤ GX < 12 dB			0.1	dB	5
8	GR step size	–12 ≤ GR ≤ 0 dB			0.1		5
9	PSRR (VCC) Image frequency	Input: 4.8 to 7.8 kHz, 200 mV p-p Measure 8000 Hz-Input frequency A-D D-A	 37 37				5
10	DISN gain accuracy	Gdisn = ±0.9375 Vin = 0 dBm0 Gdisn = –0.9375 to 0.9375	–0.25		+0.25	dB	2
11	End-to-end group delay	1014 Hz; –10 dBmO B = Z = 0; X = R = 1			525	μS	13, 12, 5
12	Crosstalk TX to RX same channel RX to TX	0 dBm0 300 Hz to 3400 Hz 0 dBm0 300 Hz to 3400 Hz			–75 –75	dBm0	

No.	Item	Condition	Min	Typ	Max	Unit	Note
13	Crosstalk between channels	0 dBm0					
	TX or RX to TX	1014 Hz			–76	dBm0	
	TX or RX to RX	1014 Hz			–78		

Notes:

1. *These tests are performed with the following load impedances:*
   Frequency < 12 kHz – Longitudinal impedance = 500 Ω; metallic impedance = 300 Ω
   Frequency > 12 kHz – Longitudinal impedance = 90 Ω; metallic impedance = 135 Ω
2. *Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
3. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
4. *When the Intelligent Access voice chipset is in the anti-sat operating region, this parameter will be degraded. The exact degradation will depend on system design.*
5. *Guaranteed by design.*
6. *Overall 1.014 kHz insertion loss error of the Intelligent Access voice chipset is guaranteed to be ≤ 0.34 dB*
7. *These SBAT, PSRR specifications are valid only when the ISLIC is used with the ISLAC, which generates the anti-sat reference. Since the anti-sat reference depends upon the battery voltage sensed by the VHB, VLB, and VPB pins of the ISLAC, the PSRR of the kit depends upon the amount of battery filtering provided by CB.*
8. *Must meet at least one of these specifications.*
9. *These voltages are referred to VREF*
10. *These limits refer to the 2-wire output of an ideal ISLIC but reflect only the capabilities the ISLAC.*
11. *When relative levels (dBm0) are used, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR + RG) from 0 to –12 dB.*
12. *Group delay spec valid only when Channels 1–2 occupy consecutive slots in the frame. Programming channels in non-consecutive timeslots adds 1 frame delay in the Group delay measurements.*
13. *The Group delay specification is defined as the sum of the minimum values of the group delays for transmit and the receive paths when the B, X, R, and Z filters are disabled with null coefficients. See Figure 15-3 for Group Delay Distortion.*
14. *These limits reflect only the capabilities of the dual ISLAC device.*

Transmit and Receive Paths

In this section, the transmit path is defined as the analog input to the ISLAC device (VINn) to the PCM voice output of the ISLAC A-law/µ law speech compressor (See Figure 7-1 in the *Am79R2xx/ Am79D2251x Technical Reference*). The receive path is defined as the PCM voice input to the ISLAC speech expander to the analog output of the ISLAC device (VOUTn). All limits defined in this section are tested with B = 0, Z = 0 and X = R = RG = 1.

When RG is enabled, a gain of –6.02 dB is added to the digital section of the receive path.

When AR is enabled, a nominal gain of –6.02 dB is added to the analog section of the receive path.

When AX is enabled, a nominal gain of +6.02 dB is added to the analog section of the transmit path.

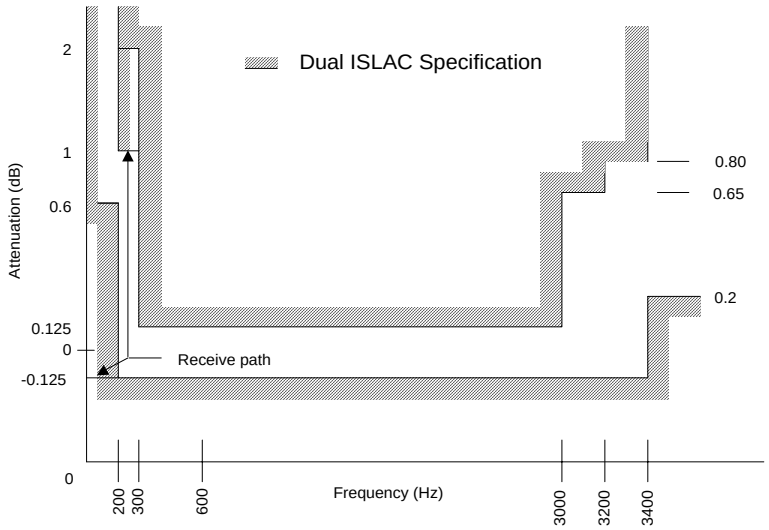
When relative levels (dBm0) are used in any of the following transmission characteristics, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to –12 dB.

These transmission characteristics are valid for 0 to 70°C.

Attenuation Distortion

The attenuation of the signal in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 6. The reference frequency is 1014 Hz and the signal level is –10 dBm0.

Figure 6. Transmit and Receive Path Attenuation vs. Frequency

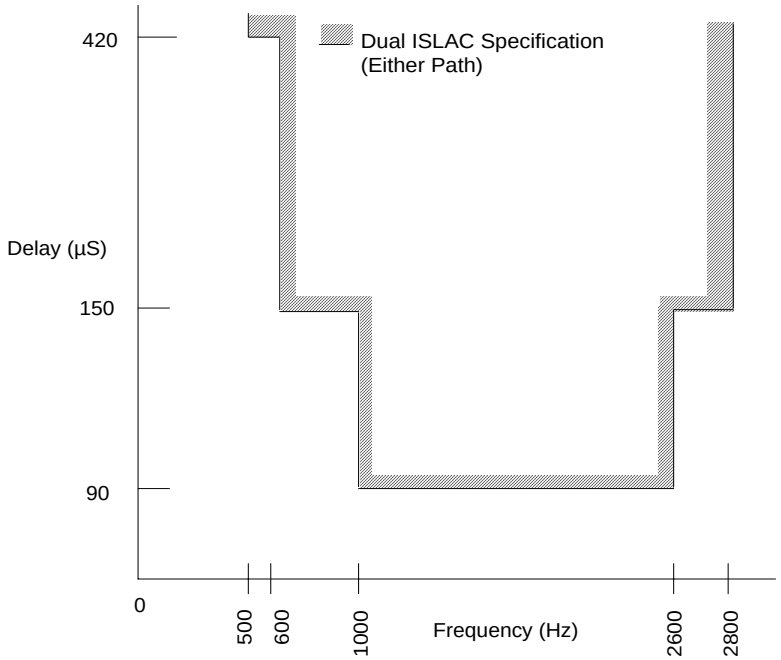


Minimum transmit attenuation at 60 Hz is 24 dB

Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 7. The minimum value of the group delay is taken as the reference. The signal level should be –10 dBm0.

Figure 7. Group Delay Distortion



Single Frequency Distortion

The output signal level, at any single frequency in the range of 300 to 3400 Hz, other than that due to an applied 0 dBm0 sine wave signal with frequency f in the same frequency range, is less than –46 dBm0. With f swept between 0 to 300 Hz and 3.4 to 12 kHz, any generated output signals other than f are less than –28 dBm0. This specification is valid for either transmission path.

Intermodulation Distortion

Two sine wave signals of different frequencies, f_1 and f_2 (not harmonically related) in the range 300 to 3400 Hz and of equal levels in the range –4 to –21 dBm0, do not produce $2 \bullet f_1 – f_2$ products having a level greater than –42 dB, relative to the level of the two input signals.

A sine wave signal in the frequency band 300 to 3400 Hz with input level –9 dBm0 and a 50 Hz signal with input level –23 dBm0 does not produce intermodulation products exceeding a level of –56 dBm0. These specifications are valid for either transmission path.

Gain Linearity

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 8 (A-law) and Figure 9 (μ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

Figure 8. A-law Gain Linearity with Tone Input (Both Paths)

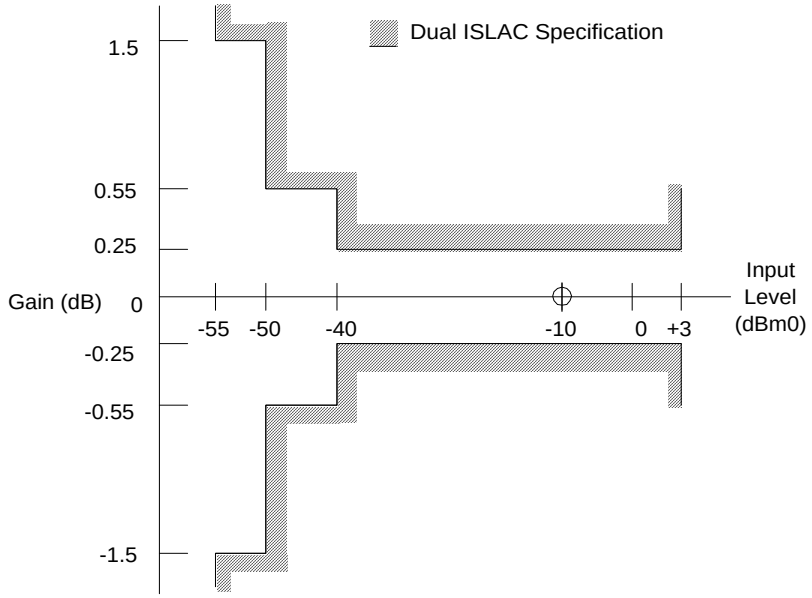
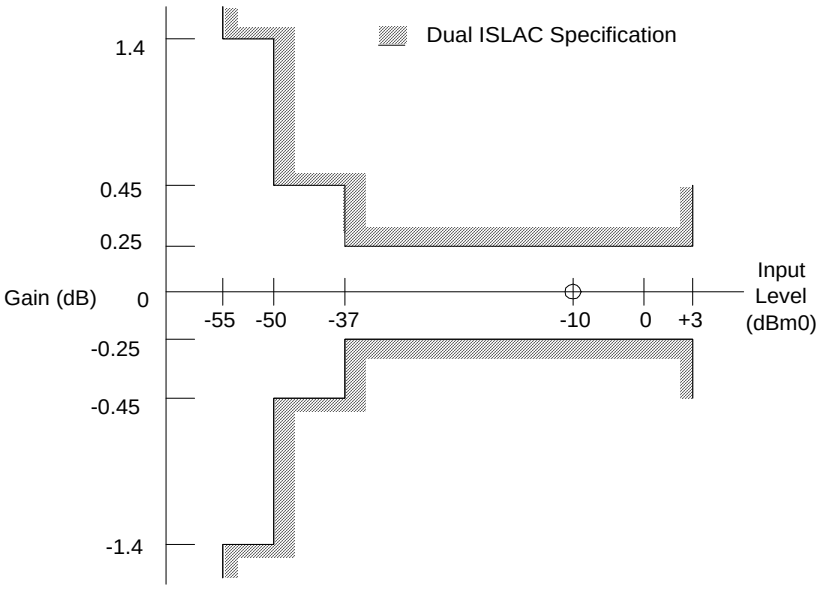


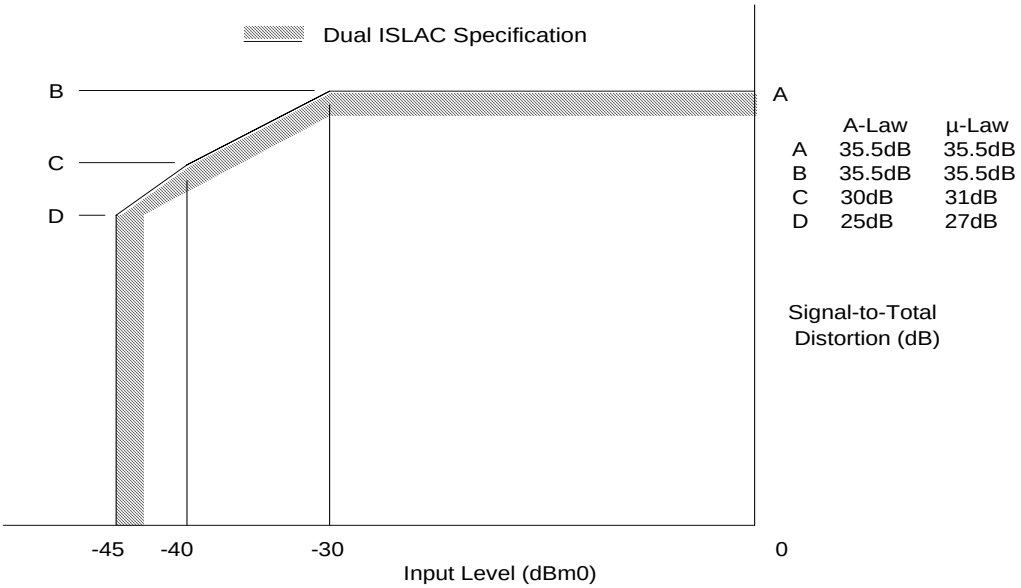
Figure 9. μ-law Gain Linearity with Tone Input (Both Paths)



Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in Figure 10 for either path when the input signal is a sine wave signal of frequency 1014 Hz.

Figure 10. Total Distortion with Tone Input, Both Paths

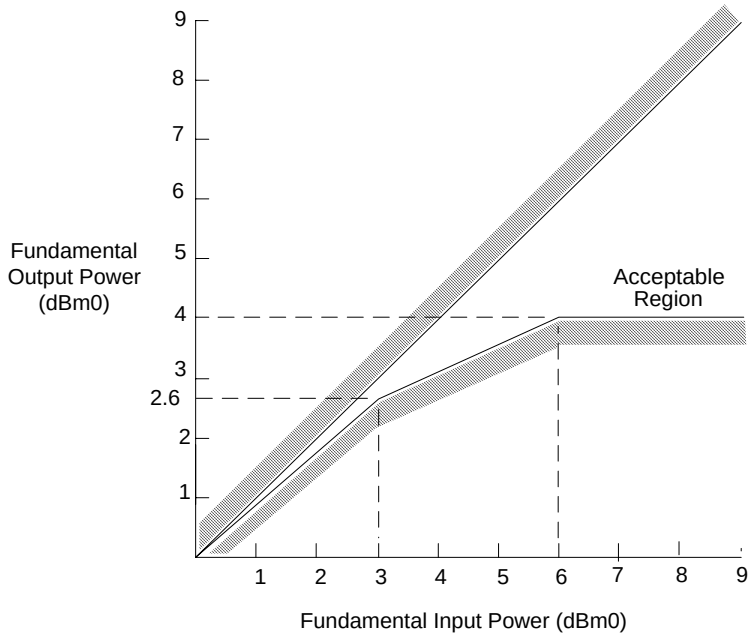


Overload Compression

Figure 11 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

(1) 1 dB < GX ≤ +12 dB; (2) –12 dB ≤ GR < –1 dB; (3) Digital voice output connected to digital voice input; and (4) measurement analog to analog.

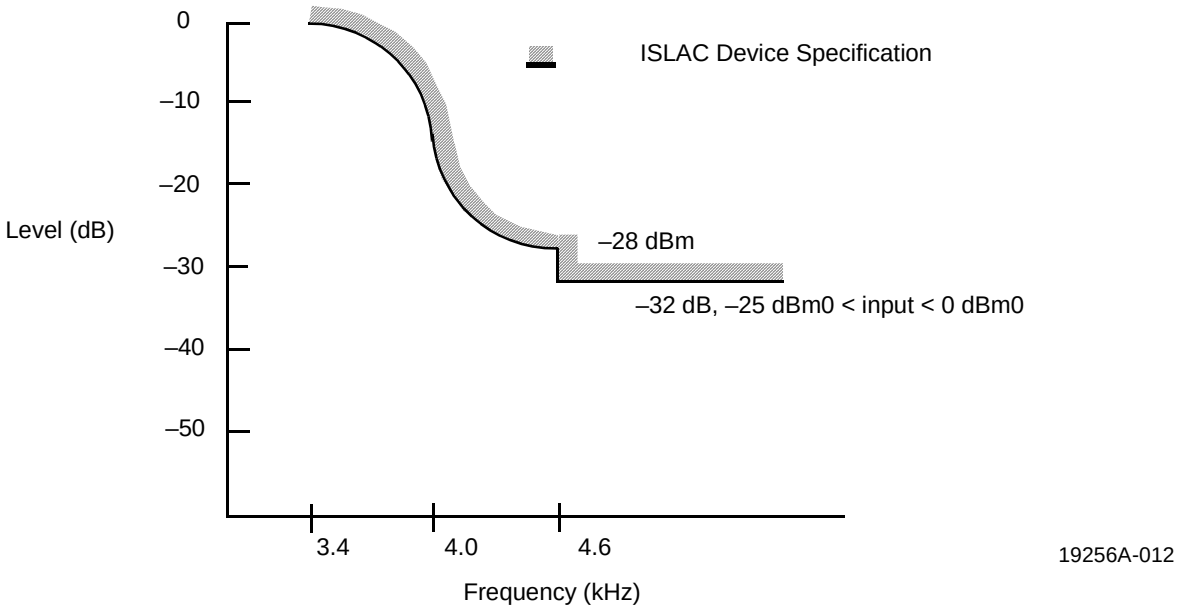
Figure 11. A/A Overload Compression



Discrimination against Out-of-Band Input Signals

When an out-of-band sine wave signal with frequency and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the following table.

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	–25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	–25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	–25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	–25 dBm0 < A ≤ 0 dBm0	see Figure 12
4600 Hz < f < 100 kHz	–25 dBm0 < A ≤ 0 dBm0	32 dB



Note:

The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Attenuation (db)} = 14 - 14\sin\frac{\pi(4000 - f)}{1200}$$

Figure 12. Discrimination Against Out-of-Band Signals

Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 13. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$A = -14 - 14\sin\frac{\pi(f-4000)}{1200}\,\mathrm{dBm0}$$

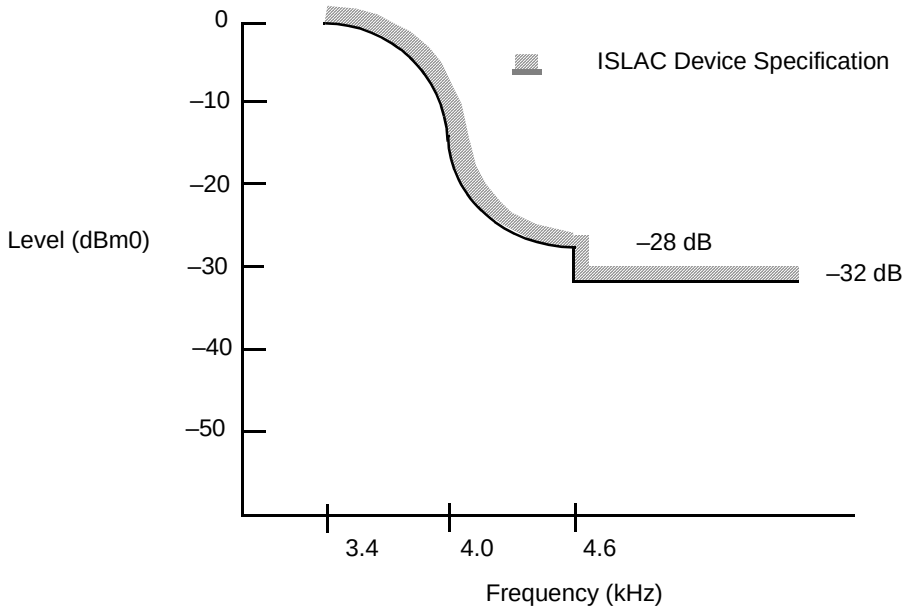


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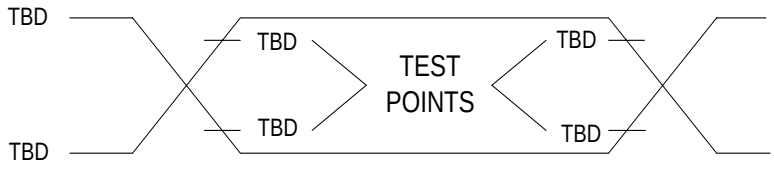
Figure 13. Spurious Out-of-Band Signals

Figure 14. PCM Switching Characteristics

VCC = 3.3 V ±5%, AGND = DGND = 0 V



Microprocessor Interface

Min and max values are valid for all digital outputs with a 100 pF load, except DIO,DXA, INTL, and TSCA which are valid with 150 pF loads.

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Data clock period	122				
2	t_{DCH}	Data clock HIGH pulse width	48				1
3	t_{DCL}	Data clock LOW pulse width	48				1
4	t_{DCR}	Rise time of clock			15		
5	t_{DCF}	Fall time of clock			15		
6	t_{ICSS}	Chip select setup time, Input mode	30		t_{DCY}–10	ns	
7	t_{ICSH}	Chip select hold time, Input mode	0		t_{DCH}–20		
8	t_{ICSL}	Chip select pulse width, Input mode		$8t_{DCY}$			
9	t_{ICSO}	Chip select off time, Input mode					1, 6
10	t_{IDS}	Input data setup time	25				5
11	t_{IDH}	Input data hold time	30				
12							
13	t_{OCSS}	Chip select setup time, Output mode	30		t_{DCY}–10		
14	t_{OCSH}	Chip select hold time, Output mode			t_{DCH}–20		
15	t_{OCSL}	Chip select pulse width, Output mode		$8t_{DCY}$			
16	t_{OCSO}	Chip select off time, output Mode				ns	1, 6
17	t_{ODD}	Output data turn on delay			50		
18	t_{ODH}	Output data hold time	3				
19	t_{ODOF}	Output data turn off delay			50		
20	t_{ODC}	Output data valid	0		50		
21	t_{RST}	Reset pulse width	50			µs	

PCM Interface

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
22	t_{PCY}	PCM clock period	0.122		7.8125	µs	2
23	t_{PCH}	PCM clock HIGH pulse width	48			ns	
24	t_{PCL}	PCM clock LOW pulse width	48				
25	t_{PCF}	Fall time of clock			15		
26	t_{PCR}	Rise time of clock			15		
27	t_{FSS}	FS setup time	30		t_{PCY}–30		
28	t_{FSH}	FS hold time	50				
29	t_{TSD}	Delay to $\overline{TSCA}$ valid	5		80		3
30	t_{TSO}	Delay to $\overline{TSCA}$ off	5				4
31	t_{DXD}	PCM data output delay	5		70		
32	t_{DXH}	PCM data output hold time	5		70		
33	t_{DXZ}	PCM data output delay to high-Z	10		70		
34	t_{DRS}	PCM data input setup time	25				
35	t_{DRH}	PCM data input hold time	5				
36	t_{FST}	PCM or frame sync jitter time	–97		97		

Master Clock

For 2.048 MHz ±100 PPM, 4.096 MHz ±100 PPM, or 8.192 MHz ±100 PPM operation:

No.	Symbol	Parameter	Min	Typ	Max	Unit	No
37	t_{MCY}	Period: 2.048 MHz Period: 4.096 MHz Period: 8.192 MHz	488.23 244.11 122.05	488.28 244.14 122.07	488.33 244.17 122.09		2
38	t_{MCR}	Rise time of clock			15	ns	
39	t_{MCF}	Fall time of clock			15		
40	t_{MCH}	MCLK HIGH pulse width	48				
41	t_{MCL}	MCLK LOW pulse width	48				

Notes:

1. *DCLK may be stopped in the HIGH or LOW state indefinitely without loss of information. When $\overline{CS}$ makes a transition to the High state, the last byte received will be interpreted by the Microprocessor Interface logic.*
2. *The PCM clock (PCLK or MCLK) frequency must be an integer multiple of the frame sync (FS) frequency with an accuracy of 100 PPM. This allowance includes any jitter that may occur between the PCM signals (FS, PCLK) and MCLK. The actual PCLK rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 128 kHz. A PCLK of 1.544 MHz may be used for standard U.S. transmission systems.*
3. *$\overline{TSCA}$ is delayed from FS by a typical value of* N • t_{PCY}*, where N is the value stored in the time/clock slot register.*
4. *t_{TSO} is defined as the time at which the output driver turns off. The actual delay time is dependent on the load circuitry. The maximum load capacitance on $\overline{TSCA}$ is 150 pF and the minimum pull-up resistance is 360 Ω.*
5. *The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*
6. *The ISLAC device requires 2.0 µs between SIO operations. If the MPI is being accessed while the MCLK (or PCLK if combined with MCLK) input is not active, a Chip Select Off time of 20 µs is required when accessing coefficient RAM.*

PCM Switching Waveforms

Figure 15. Master Clock Timing

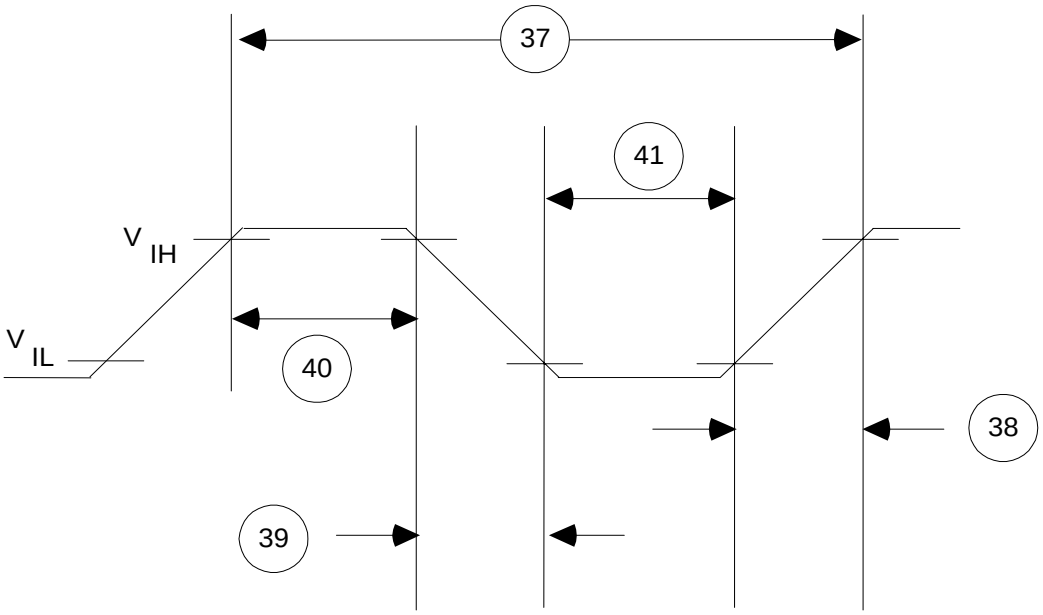


Figure 16. Microprocessor Interface (Input Mode)

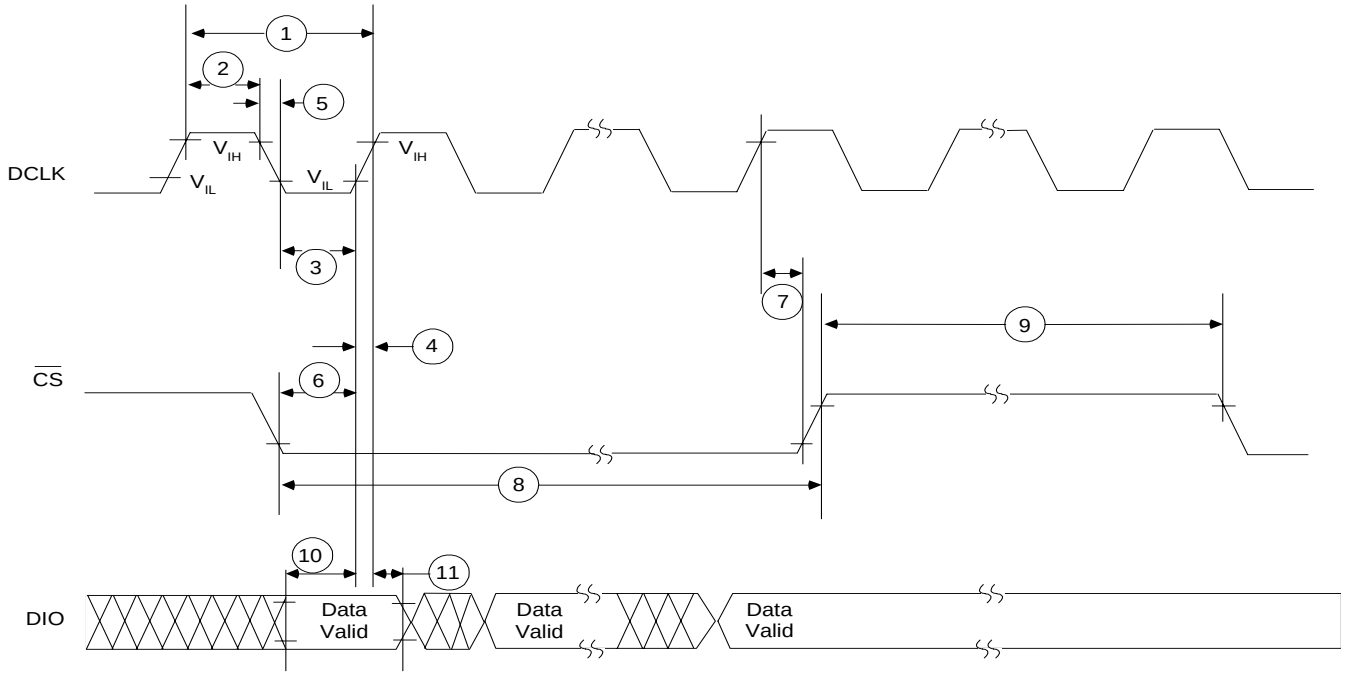


Figure 17. Microprocessor Interface (Output Mode)

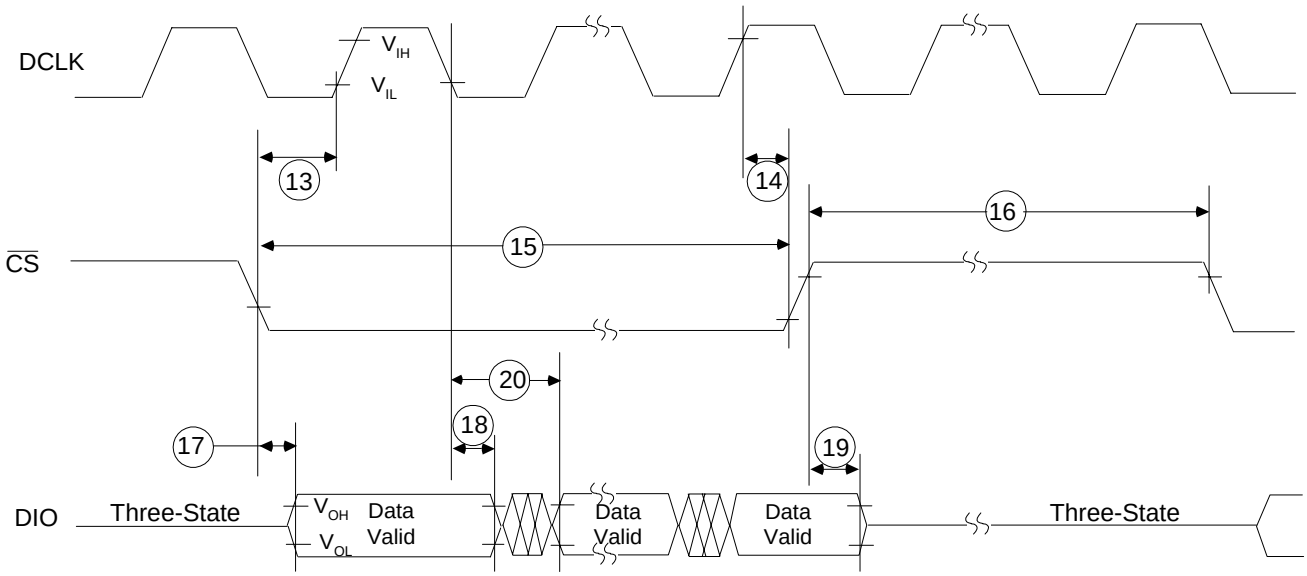


Figure 18. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge))

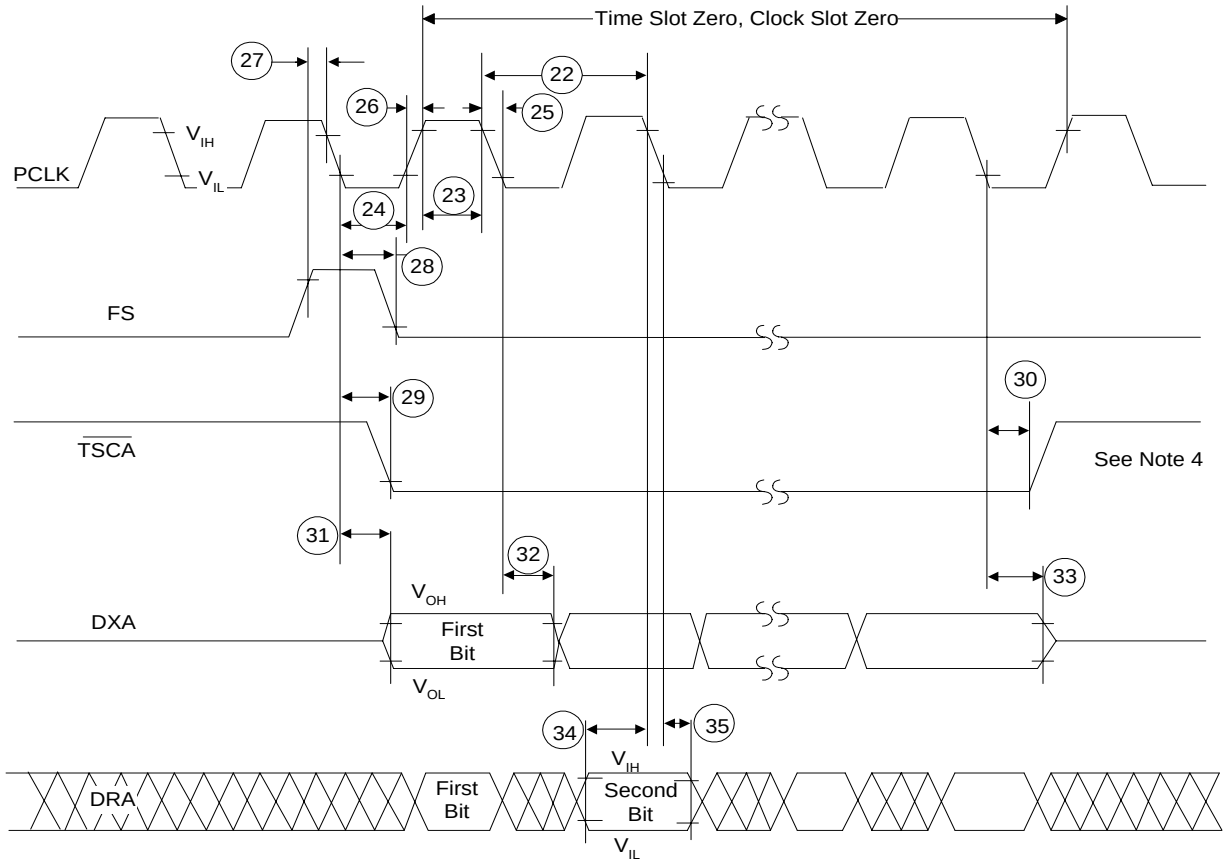
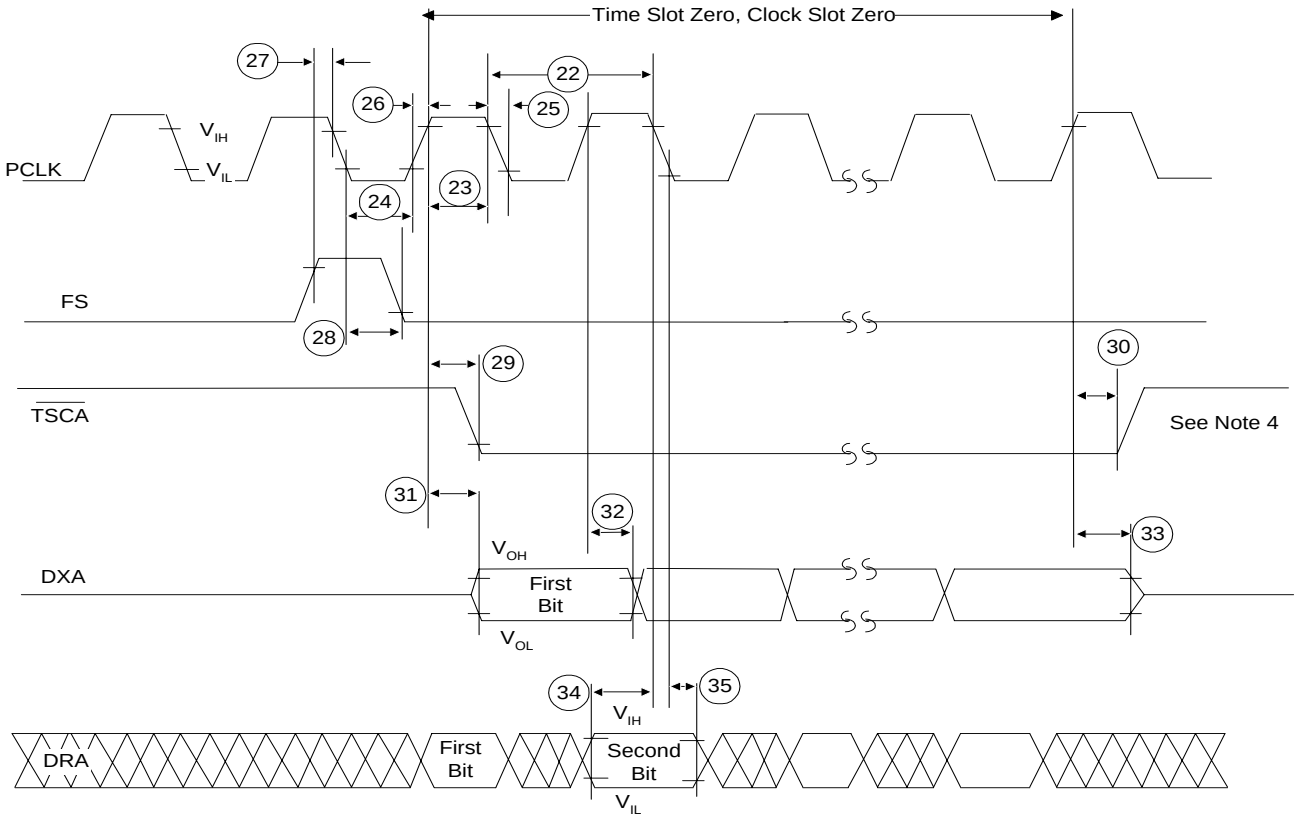


Figure 19. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)



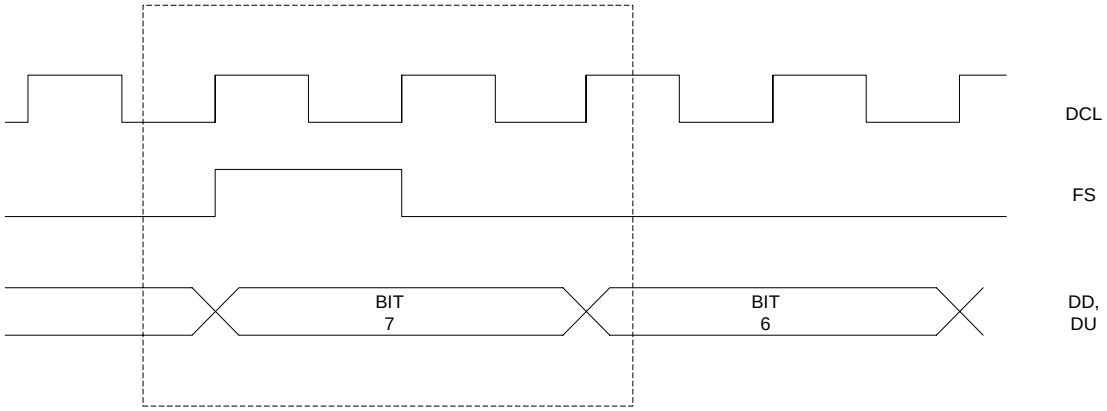
GCI Timing Specifications

Symbol	Signal	Parameter	Min	Typ	Max	Unit
t_R, t_F	DCL	Rise/fall time			60	ns
t_{DCL}	DCL	Period, F_{DCL} = 2048 kHz F_{DCL} = 4096 kHz	478 239		498 249	
t_{WH}, t_{WL}	DCL	Pulse width	90			
t_R, t_F	FS	Rise/fall time			60	
t_{SF}	FS	Setup time	70		t_{DCL}–50	
t_{HF}	FS	Hold time	50			
t_{WFH}	FS	High pulse width	130			
t_{DDC}	DU	Delay from DCL edge			100	
t_{DDF}	DU	Delay from FS edge			150	
t_{SD}	DD	Data setup	twH+20			
t_{HD}	DD	Data hold	50			

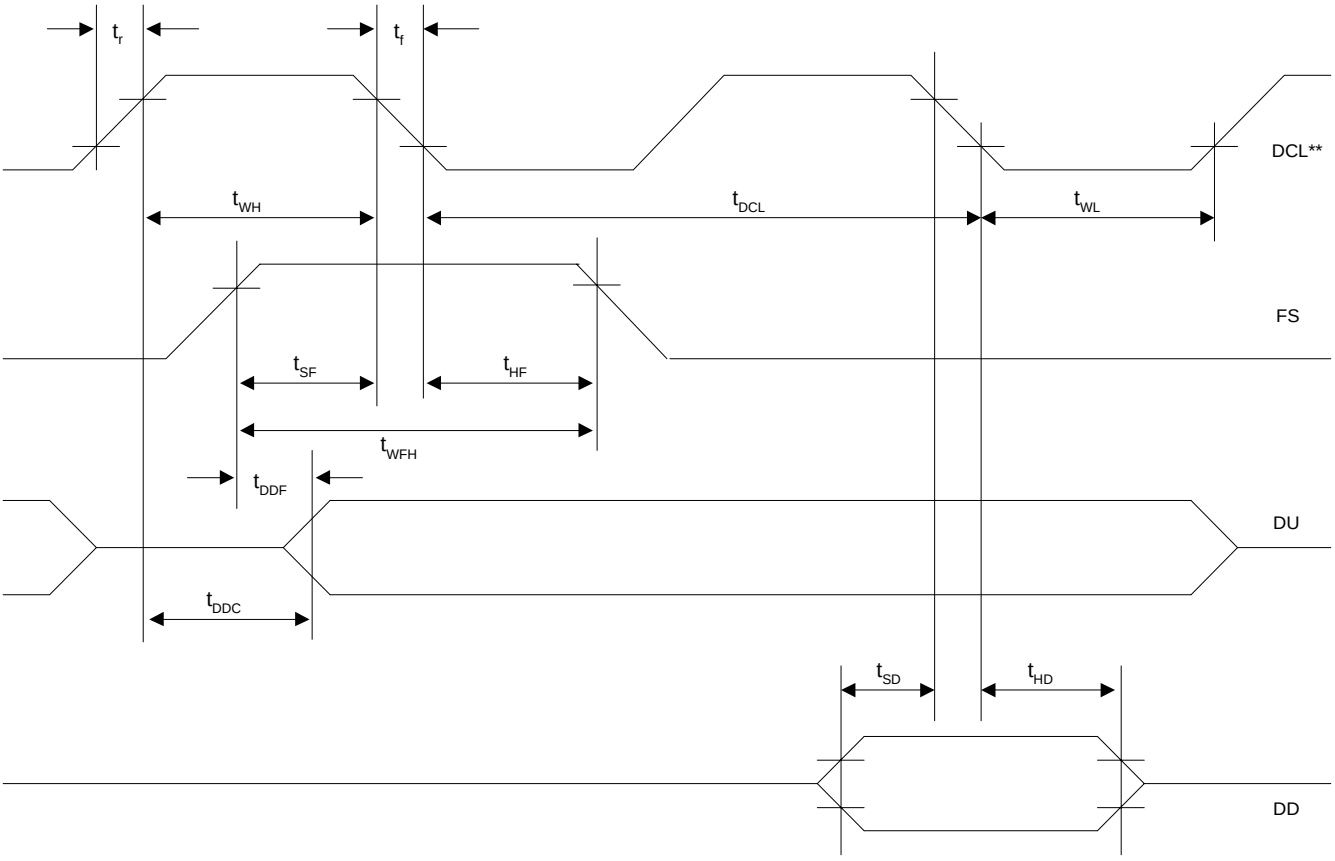
Notes:

1. *The Data Clock (DCL) can be stopped in the high or low state without loss of information.*
2. *A temporary stoppage of DCL must not put the ISLAC into a state in which it does not respond to a software reset command.*
3. *All frequency-dependent specifications are guaranteed for clock frequencies within ±100 PPM from nominal.*

GCI Waveforms



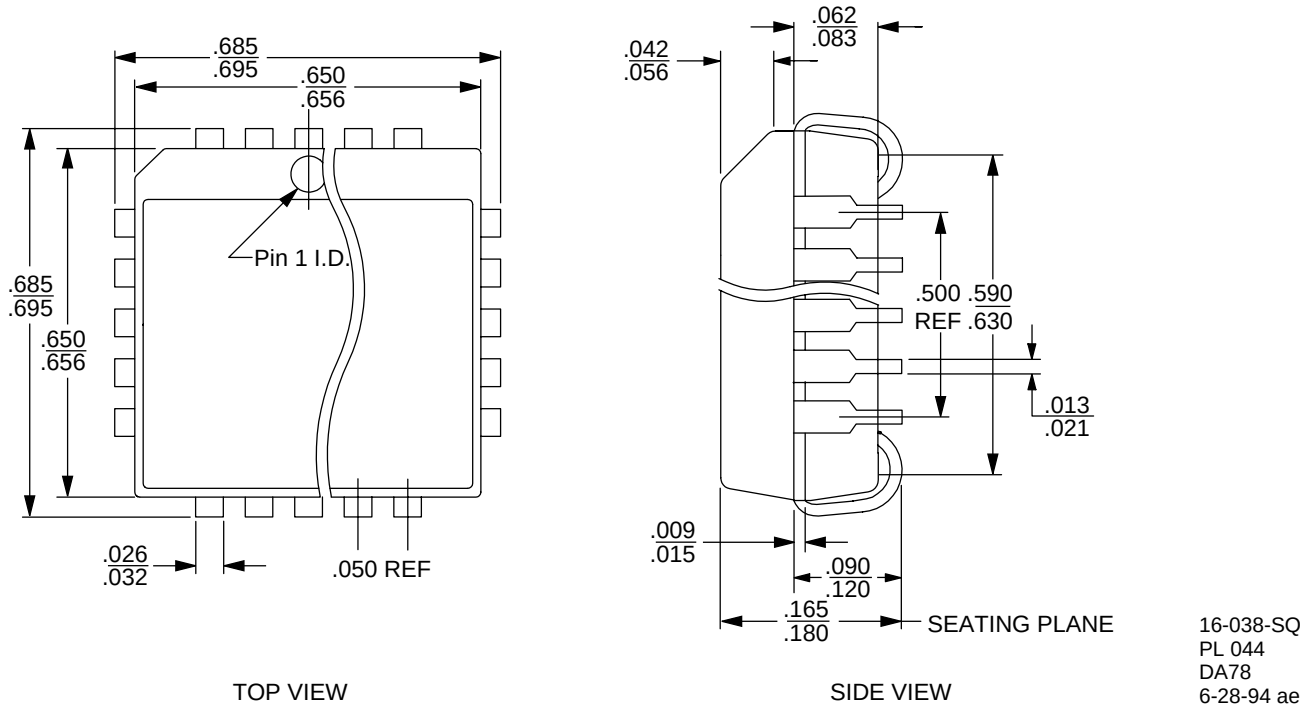
DETAIL A



** Timing diagram valid for
F_{DCL} = 2048 or 4096 KHz

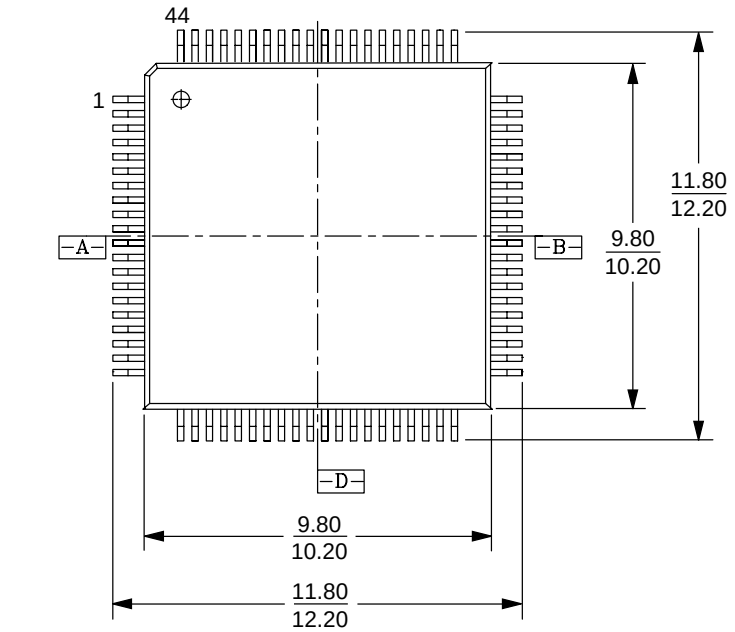
PHYSICAL DIMENSIONS

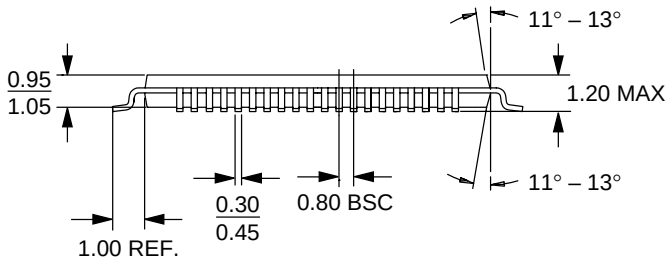
44-Pin PLCC



16-038-SQ
PL 044
DA78
6-28-94 ae

44-Pin TQFP





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REVISION SUMMARY

Revision A to Revision B

- Revision A was a condensed version of the datasheet while Revision B contains the full version.

Revision B to Revision C

- Page 13, Linecard Parts List, Rows CHLbi and CHLdi: switched the numbers in the “Values” column.