

Product Description

The PE43703 is a HaRP™-enhanced, high linearity, 7-bit RF Digital Step Attenuator (DSA). This highly versatile DSA covers a 31.75 dB attenuation range in 0.25 dB, 0.5 dB, or 1.0 dB steps. The customer can choose which step size and associated specifications are best suited for their application. The Peregrine 50Ω RF DSA provides multiple CMOS control interfaces and an optional external Vss feature. It maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss and low power consumption. Performance does not change with V_{DD} due to on-board regulator. This next generation Peregrine DSA is available in a 5x5 mm 32-lead QFN footprint.

The PE43703 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Package Type

32-lead 5x5x0.85 mm QFN Package

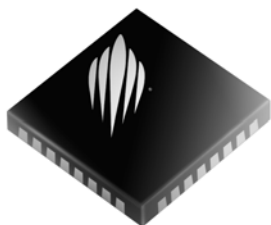
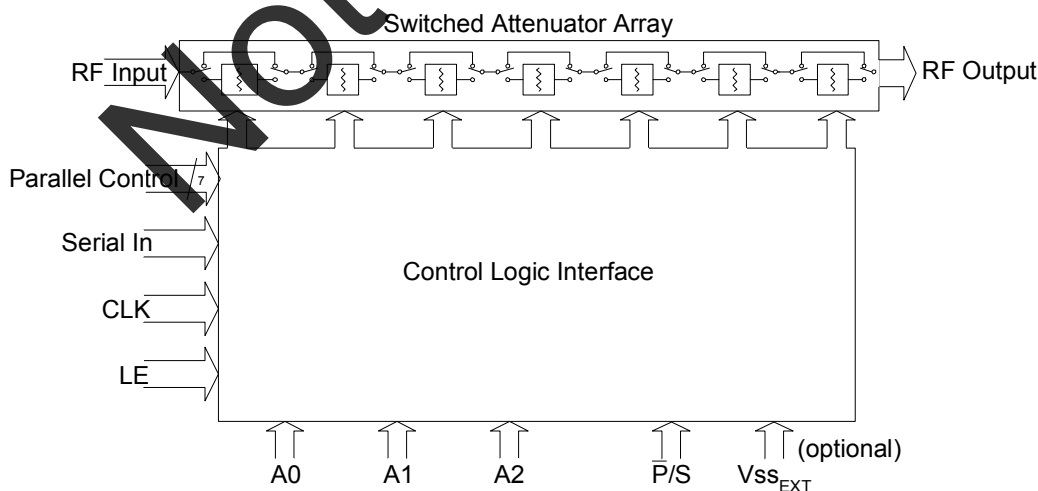


Figure 2. Functional Schematic Diagram



50 Ω RF Digital Attenuator

7-bit, 31.75 dB, 9 kHz - 6000 MHz

V_{ssEXT} option

Features

- HaRP™-enhanced UltraCMOS™ device
- Attenuation options: 0.25 dB, 0.5 dB, or 1.0 dB steps to 31.75 dB
 - 0.25 dB monotonicity for ≤ 4.0 GHz
 - 0.5 dB monotonicity for ≤ 5.0 GHz
 - 1 dB monotonicity for ≤ 6.0 GHz
- High Linearity: Typical +59 dBm IIP3
 - Excellent low-frequency performance
- Optional External Vss Control (V_{ssEXT})
- 3.3 V or 5.0 V Power Supply Voltage
- Fast switch settling time
- Programming Modes:
 - Direct Parallel
 - Latched Parallel
 - Serial-Addressable: Program up to eight addresses 000 - 111
- High-attenuation state @ power-up (PUP)
- CMOS Compatible
- No DC blocking capacitors required

Table 1. Electrical Specifications: 0.25 dB steps @ +25°C, $V_{DD} = 3.3\text{ V}$ or 5.0 V , $V_{SS_{EXT}} = -2.7\text{ V}$ or GND

| Parameter | Test Conditions | Frequency | Min | Typical | Max | Units |
|-------------------------------------|--|--------------------|-------|-----------|-------------------|---------|
| Frequency Range | | | 9 kHz | | 4000 MHz | |
| Attenuation Range | 0.25 dB Step | | | 0 – 31.75 | | dB |
| Insertion Loss | | 9 kHz \leq 4 GHz | | 1.9 | 2.4 | dB |
| Attenuation Error | 0 dB - 7.75 dB Attenuation settings | 9 kHz < 3 GHz | | | $\pm(0.2+1.5\%)$ | dB |
| | 8 dB - 31.75 dB Attenuation settings | 9 kHz < 3 GHz | | | $\pm(0.15+4\%)$ | dB |
| | 0 dB - 31.75 dB Attenuation settings | 3 GHz < 4 GHz | | | $\pm(0.25+4.5\%)$ | dB |
| Return Loss | | 9 kHz - 4 GHz | | 18 | | dB |
| Relative Phase | All States | 9 kHz - 4 GHz | | 33 | | deg |
| P1dB (note 1) | Input | 20 MHz - 4 GHz | 30 | 32 | | dBm |
| IIP3 | Two tones at +18 dBm, 20 MHz spacing | 20 MHz - 4 GHz | | 59 | | dBm |
| Typical Spurious Value ² | $V_{SS_{EXT}}$ grounded | 1 MHz | | 10 | | dBm |
| Video Feed Through | | | | 10 | | mVpp |
| Switching Time | 50% DC CTRL to 10% / 90% RF | | | 650 | | ns |
| RF Trise/Tfall | 10% / 90% RF | | | 400 | | ns |
| Settling Time | RF settled to within 0.05 dB of final value. RBW = 5 MHz, Averaging ON. | | | 4 | 25 | μ s |

Notes: 1. Please note Maximum Operating Pin (50 Ω) of +23dBm as shown in Table 5.
2. To prevent negative voltage generator spurs, supply -2.7 volts to $V_{SS_{EXT}}$.

Performance Plots, 0.25 dB step

Figure 3. 0.25 dB Step Attenuation*

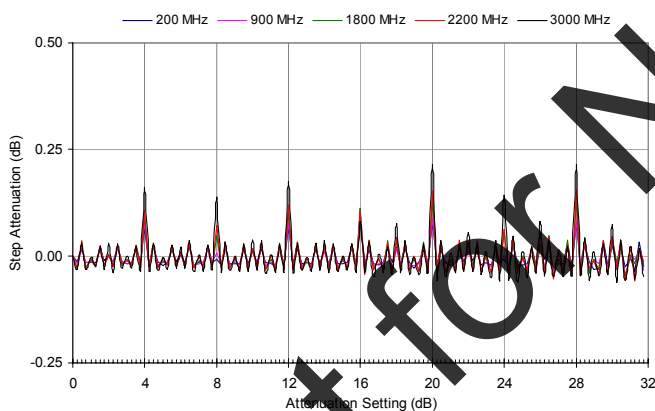
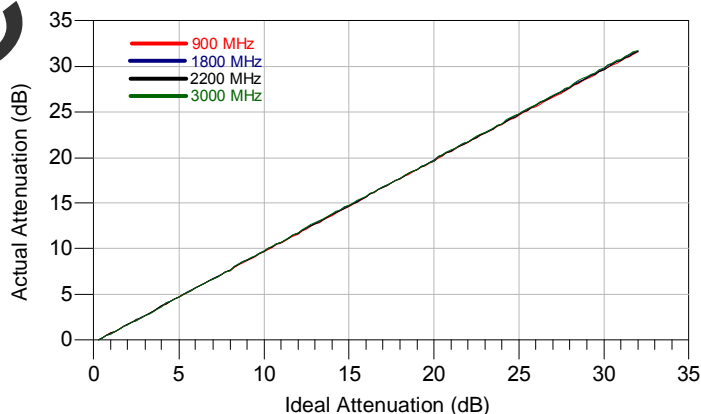


Figure 4. 0.25 dB Step, Actual vs. Ideal Attenuation



*Monotonicity is held so long as Step Attenuation does not cross below -0.25

Figure 5. 0.25 dB Major State Bit Error

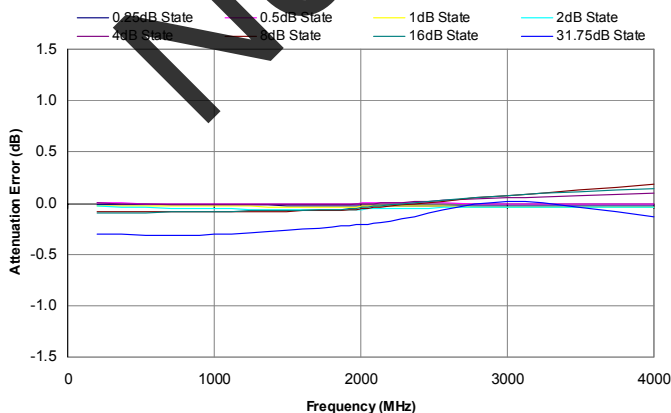


Figure 6. 0.25 dB Attenuation Error

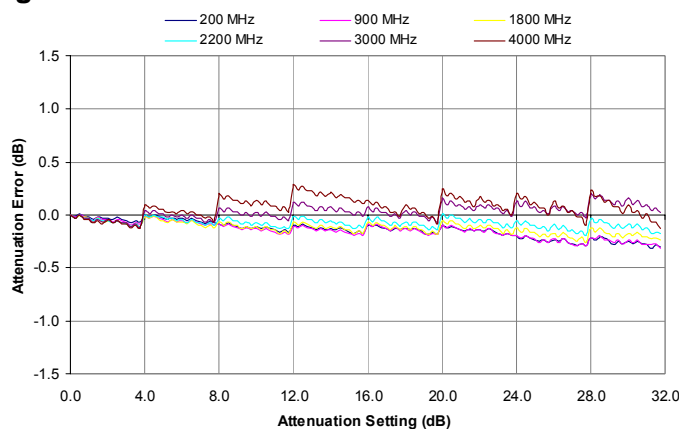


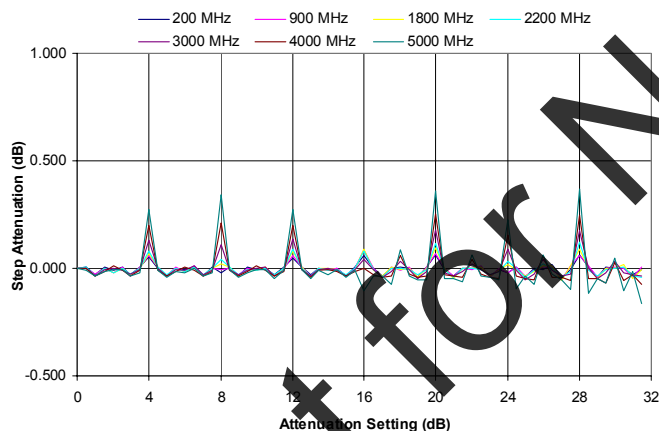
Table 2. Electrical Specifications: 0.5 dB steps @ +25°C, $V_{DD} = 3.3\text{ V}$ or 5.0 V , $V_{SS_{EXT}} = -2.7\text{ V}$ or GND

| Parameter | Test Conditions | Frequency | Min | Typical | Max | Units |
|-------------------------------------|--|----------------|-------|----------|--------------|-------|
| Frequency Range | | | 9 kHz | | 5000 MHz | |
| Attenuation Range | 0.5 dB Step | | | 0 – 31.5 | | dB |
| Insertion Loss | | 9 kHz ≤ 5 GHz | | 2.0 | 2.6 | dB |
| Attenuation Error | 0 dB - 31.5 dB Attenuation settings 0 dB - 16.5 dB Attenuation settings 17 dB - 31.5 dB Attenuation settings | 9 kHz < 4 GHz | | | ±(0.25+4.5%) | dB |
| | | 4 ≤ 5 GHz | | | ±(0.3+5%) | dB |
| | | 4 ≤ 5 GHz | | | ±(1.3+0%) | dB |
| Return Loss | | 9 kHz - 5 GHz | | 18 | | dB |
| Relative Phase | All States | 9 kHz - 5 GHz | | 56 | | deg |
| P1dB (note 1) | Input | 20 MHz - 5 GHz | 30 | 32 | | dBm |
| IIP3 | Two tones at +18 dBm, 20 MHz spacing | 20 MHz - 5 GHz | | 57 | | dBm |
| Typical Spurious Value ² | $V_{SS_{EXT}}$ grounded | 1 MHz | | 110 | | dBm |
| Video Feed Through | | | | 10 | | mVpp |
| Switching Time | 50% DC CTRL to 10% / 90% RF | | | 650 | | ns |
| RF Trise/Tfall | 10% / 90% RF | | | 400 | | ns |
| Settling Time | RF settled to within 0.05 dB of final value. RBW = 5 MHz, Averaging ON. | | | 4 | 25 | μs |

Notes: 1. Please note Maximum Operating Pin (50Ω) of +23dBm as shown in Table 5.
2. To prevent negative voltage generator spurs, supply -2.7 volts to $V_{SS_{EXT}}$.

Performance Plots, 0.5 dB step

Figure 7. 0.5 dB Step Attenuation*



*Monotonicity is held so long as Step Attenuation does not cross below -0.5

Figure 9. 0.5 dB Major State Bit Error

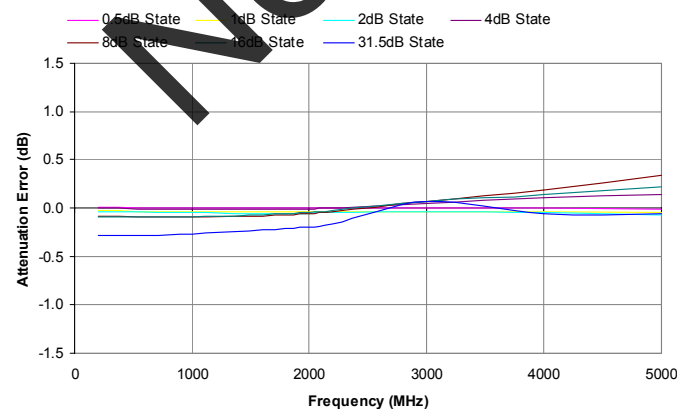


Figure 8. 0.5 dB Step, Actual vs. Ideal Attenuation

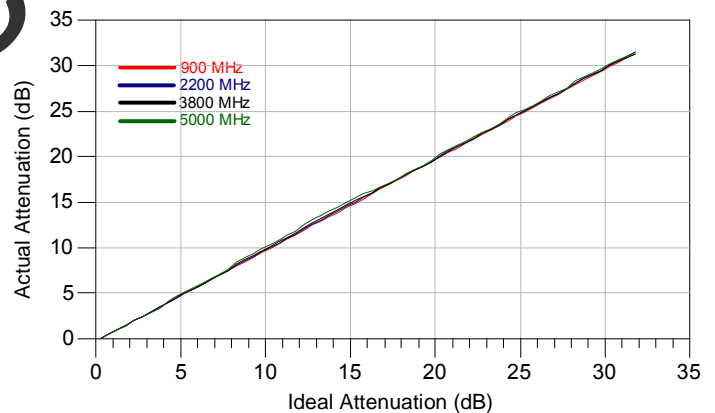


Figure 10. 0.5 dB Attenuation Error

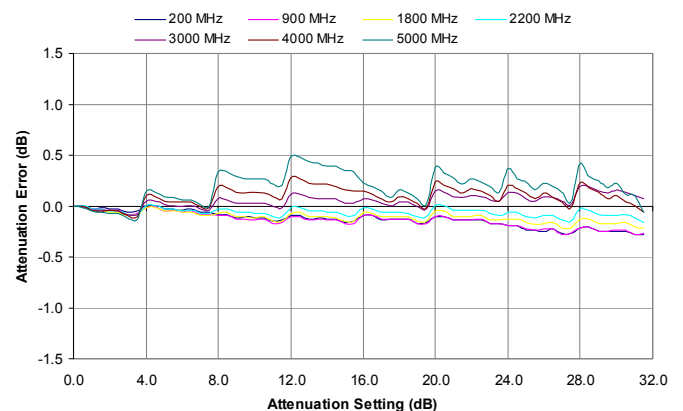


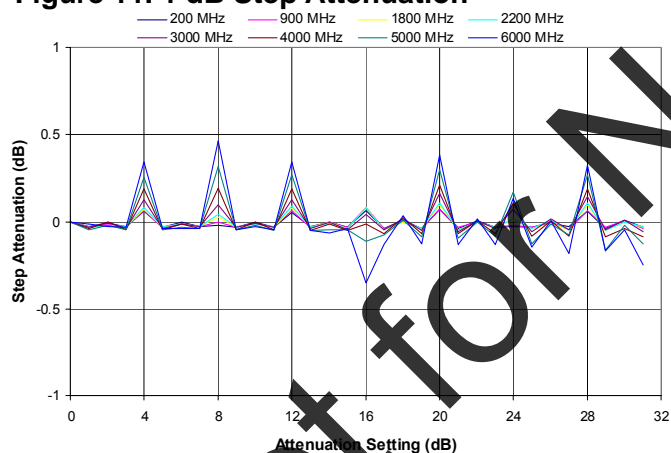
Table 3. Electrical Specifications: 1 dB steps @ +25°C, $V_{DD} = 3.3\text{ V}$ or 5.0 V , $V_{SS_{EXT}} = -2.7\text{ V}$ or GND

| Parameter | Test Conditions | Frequency | Min | Typical | Max | Units |
|-------------------------------------|--|--------------------|-------|---------|-------------------|---------|
| Frequency range | | | 9 kHz | | 6000 MHz | |
| Attenuation Range | 1 dB Step | | | 0 - 31 | | dB |
| Insertion Loss | | 9 kHz \leq 6 GHz | | 2.3 | 2.8 | dB |
| Attenuation Error | 0 dB - 31 dB Attenuation settings | 9 kHz - 4 GHz | | | $\pm(0.25+4.5\%)$ | dB |
| | 0 dB - 12 dB Attenuation settings | 4 GHz \leq 6 GHz | | | +0.4+8% | dB |
| | 13 dB - 31 dB Attenuation setting | 4 GHz \leq 6 GHz | | | +1.4+0% | dB |
| | 0 dB - 31 dB Attenuation settings | 4 GHz \leq 6 GHz | | | -0.2-3% | dB |
| Return Loss | | 9 kHz - 6 GHz | | 18 | | dB |
| Relative Phase | All States | 9 kHz - 6 GHz | | 74 | | deg |
| P1dB (note 1) | Input | 20 MHz - 6 GHz | 30 | 32 | | dBm |
| IIP3 | Two tones at +18 dBm, 20 MHz spacing | 20 MHz - 6 GHz | | 50 | | dBm |
| Typical Spurious Value ² | $V_{SS_{EXT}}$ grounded | 1 MHz | | -110 | | dBm |
| Video Feed Through | | | | 16 | | mVpp |
| Switching Time | 50% DC CTRL to 10% / 90% RF | | | 650 | | ns |
| RF Trise/Tfall | 10% / 90% RF | | | 400 | | ns |
| Settling Time | RF settled to within 0.05 dB of final value. RBW = 5 MHz, Averaging ON. | | | 4 | 25 | μ s |

Notes: 1. Please note Maximum Operating Pin (50Q) of +23dBm as shown in Table 5.
2. To prevent negative voltage generator spurs, supply -2.7 volts to $V_{SS_{EXT}}$.

Performance Plots, 1 dB step

Figure 11. 1 dB Step Attenuation



*Monotonicity is held so long as Step Attenuation not cross below -1

Figure 13. 1 dB Major State Bit Error

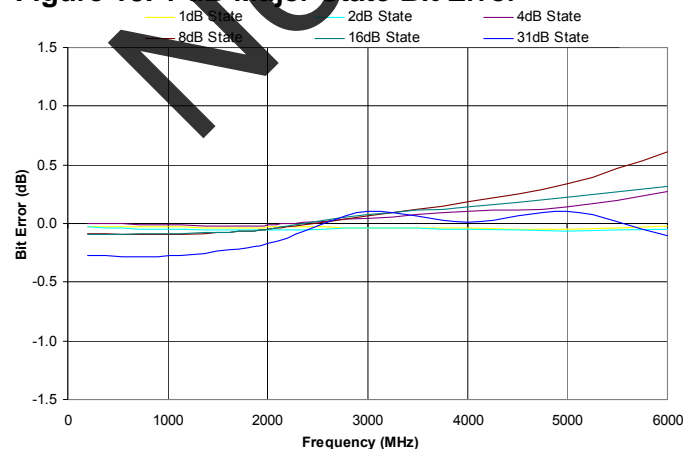


Figure 12. 1 dB Step, Actual vs. Ideal Attenuation

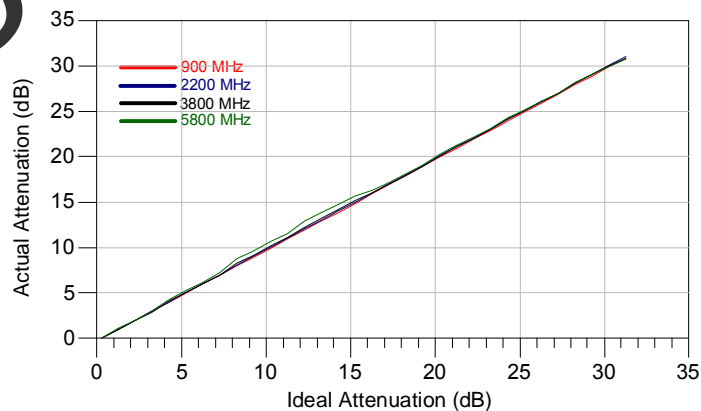
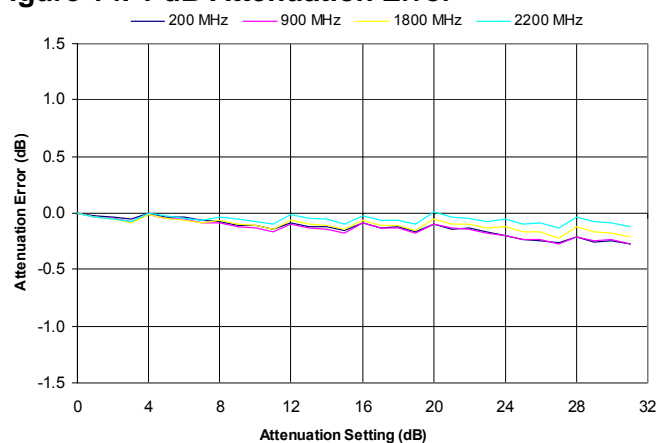


Figure 14. 1 dB Attenuation Error



Performance Plots, 1 dB step (continued)

Figure 15. 1 dB Attenuation Error (continued)

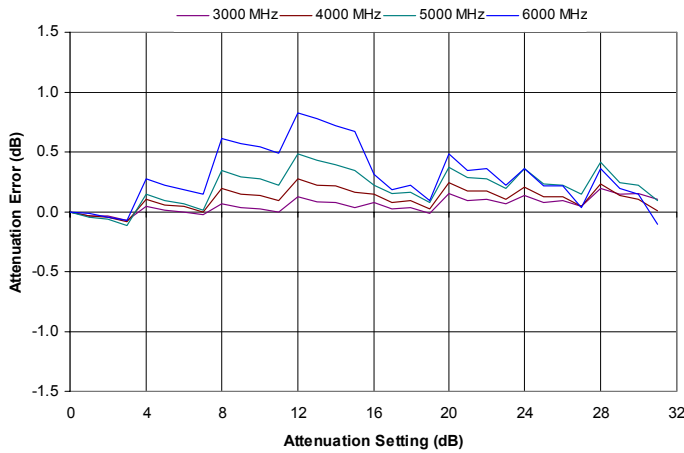


Figure 16. Insertion Loss @ Temperature

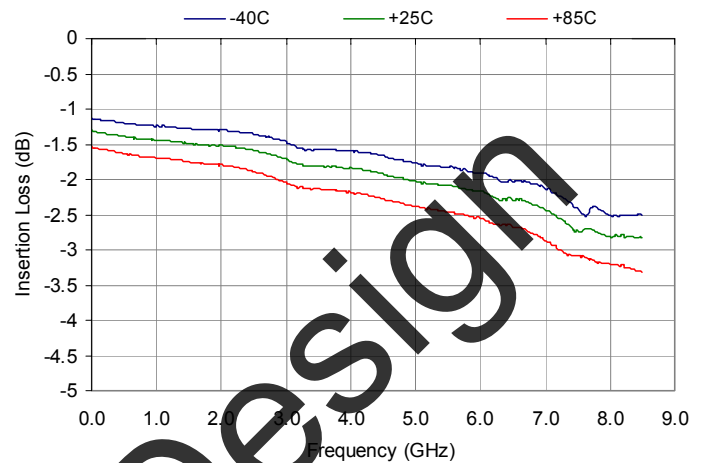


Figure 17. Input Return Loss (+25C)

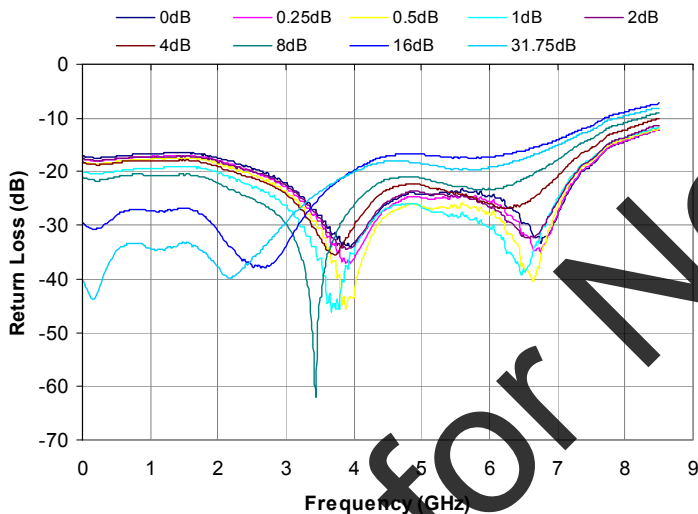


Figure 18. Output Return Loss (+25C)

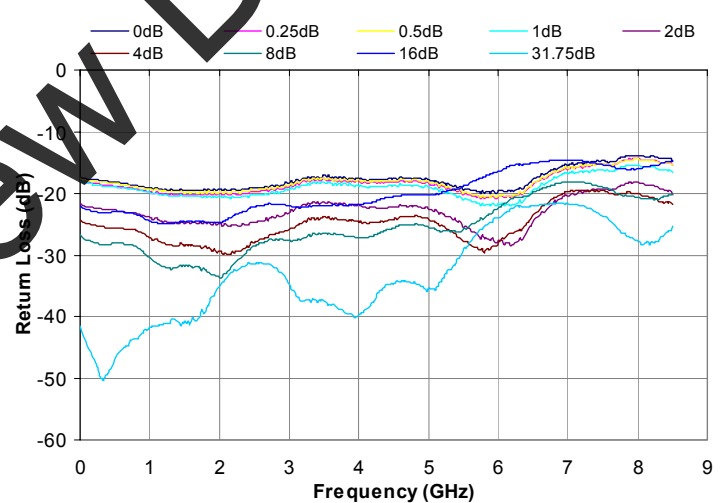


Figure 19. Input Return Loss @ Temperature for 16 dB State

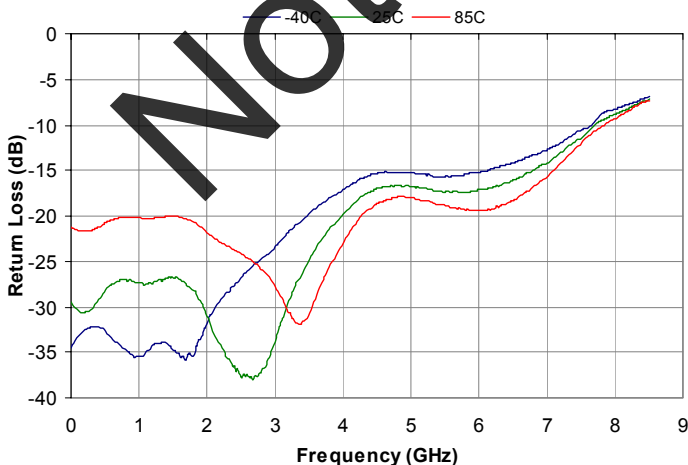
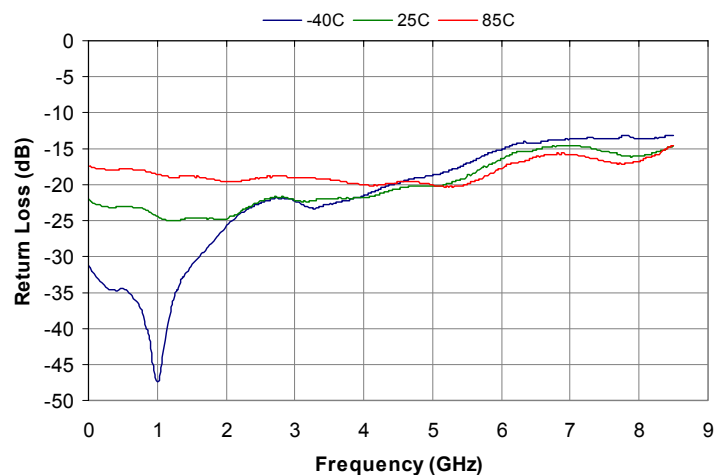


Figure 20. Output Return Loss @ Temperature for 16 dB State



Performance Plots (continued)

Figure 21. Relative Phase Error

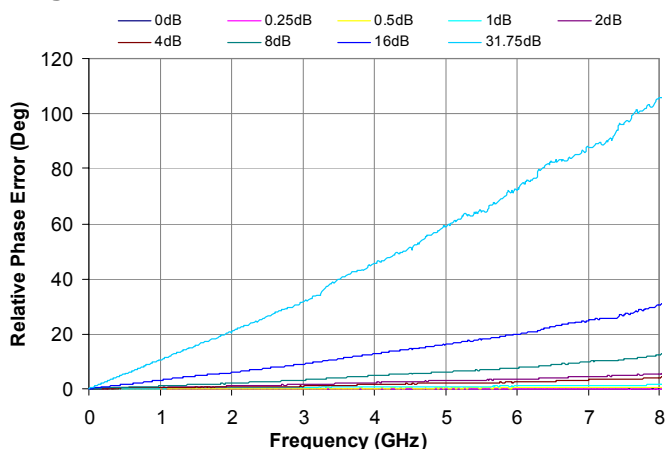


Figure 22. Relative Phase Error vs. Temperature for 31.75 dB State

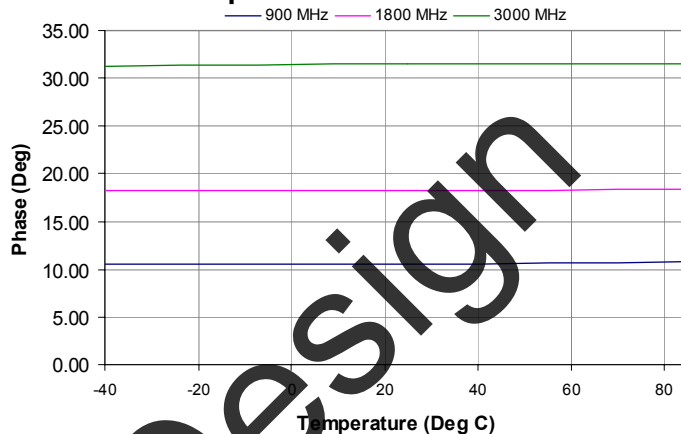


Figure 23. Attenuation Error @ 900 MHz

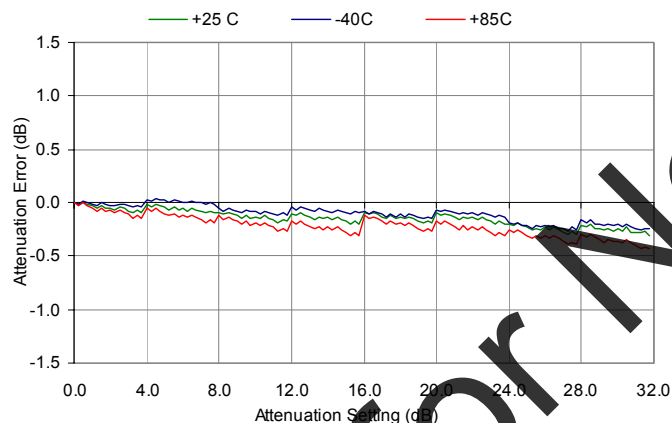


Figure 24. Attenuation Error @ 1800 MHz

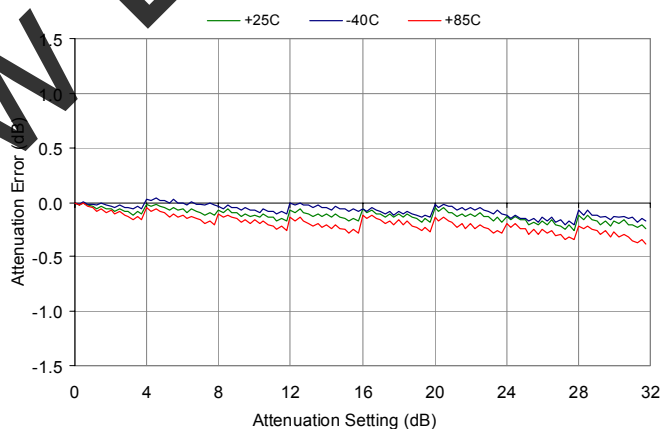


Figure 25. Attenuation Error @ 3000 MHz

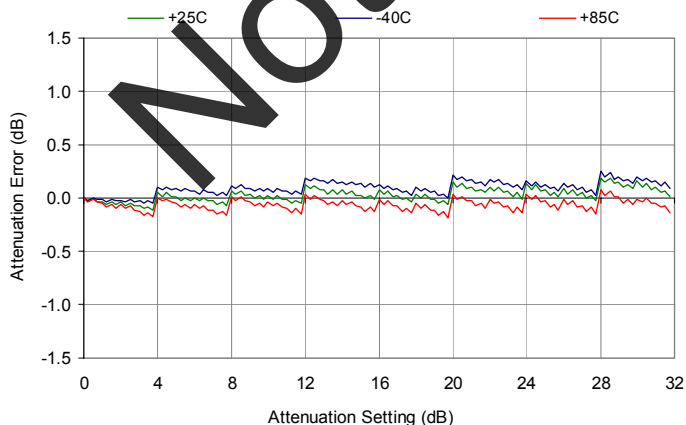


Figure 26. Input IP3 vs. Frequency

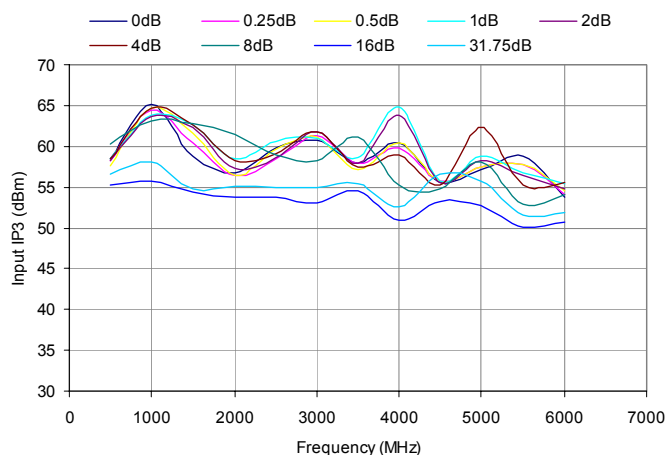


Figure 27. Pin Configuration (Top View)

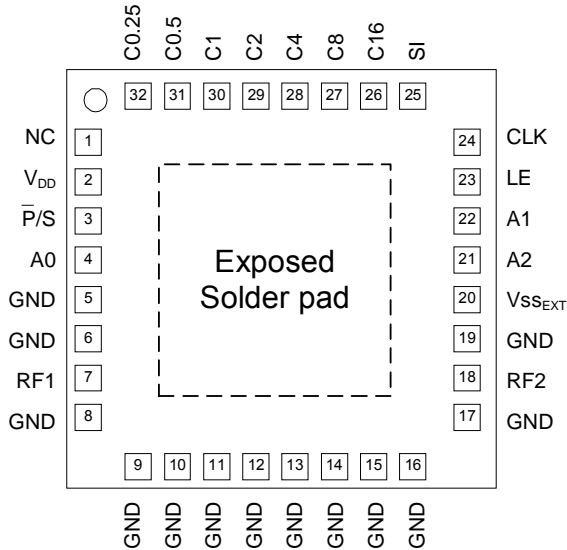


Table 4. Pin Descriptions

| Pin No. | Pin Name | Description |
|---------|--------------------|-------------------------------------|
| 1 | N/C | No Connect |
| 2 | V _{DD} | Power supply pin |
| 3 | P/S | Serial/Parallel mode select |
| 4 | A0 | Address Bit A0 connection |
| 5 | GND | Ground |
| 6 | GND | Ground |
| 7 | RF1 | RF1 port |
| 8 - 17 | GND | Ground |
| 18 | RF2 | RF2 port |
| 19 | GND | Ground |
| 20 | V _{ssEXT} | External V _{ss} Control |
| 21 | A2 | Address Bit A2 connection |
| 22 | A1 | Address Bit A1 connection |
| 23 | LE | Serial interface Latch Enable input |
| 24 | CLK | Serial interface Clock input |
| 25 | SI | Serial interface Data input |
| 26 | C16 (D6) | Parallel control bit, 16 dB |
| 27 | C8 (D5) | Parallel control bit, 8 dB |
| 28 | C4 (D4) | Parallel control bit, 4 dB |
| 29 | C2 (D3) | Parallel control bit, 2 dB |
| 30 | C1 (D2) | Parallel control bit, 1 dB |
| 31 | C0.5 (D1) | Parallel control bit, 0.5 dB |
| 32 | C0.25 (D0) | Parallel control bit, 0.25 dB |
| Paddle | GND | Ground for proper operation |

Note: Ground C0.25, C0.5, C1 C2, C4, C8, C16 if not in use.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Optional External V_{ss} Control (V_{ssEXT})

For proper operation, the V_{ssEXT} control must be grounded or at the V_{ss} voltage specified in the Operating Ranges table. When the V_{ssEXT} control pin on the package is grounded the switch FET's are biased with an internal low spur negative voltage generator. For applications that require the lowest possible spur performance, V_{ssEXT} can be applied to bypass the internal negative voltage generator to eliminate the spurs.

Switching Frequency

The PE43703 has a maximum 25 kHz switching rate when V_{ssEXT} is grounded. Switching rate is defined to be the speed at which the DSA can be toggled across attenuation states.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE43703 in the 5x5 QFN package is MSL1.

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Table 5. Operating Ranges

| Parameter | Min | Typ | Max | Units |
|---|------|------|--------------------|------------|
| V _{DD} 3.3 V Power Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| V _{DD} 5.0 V Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{SS} _{EXT} Negative Power Supply Voltage ¹ | -3.0 | -2.7 | -2.4 | V |
| I _{DD} Power Supply Current | | 70 | 350 | μA |
| Digital Input High | 2.6 | | 5.5 | V |
| P _{IN} Input power (50Ω): 9 kHz ≤ 20 MHz 20 MHz ≤ 6 GHz | | | See fig. 28 +23 | dBm dBm |
| T _{OP} Operating temperature range | -40 | 25 | 85 | °C |
| Digital Input Low | 0 | | 1 | V |
| Digital Input Leakage | | | 15 | μA |

Note: 1. Applied only when external VSS power supply used. Pin 20 must be grounded when using internal Vss supply

Table 6. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|--------------------------------|---|------|--------------------|------------|
| V _{DD} | Power supply voltage | -0.3 | 6.0 | V |
| V _{SS} _{EXT} | Vss External Negative Power Supply Voltage (optional) | -4.0 | 0.3 | V |
| V _I | Voltage on any Digital input | -0.3 | 5.8 | V |
| P _{IN} | Input power (50Ω) 9 kHz ≤ 20 MHz 20 MHz ≤ 6 GHz | | See fig. 28 +23 | dBm dBm |
| T _{ST} | Storage temperature range | -65 | 150 | °C |
| V _{ESD} | ESD voltage (HBM) ESD voltage (Machine Model) | | 500 100 | V V |

Note: 1. Human Body Model (HBM, MIL-STD 883 Method 3015.7)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Figure 28. Maximum Power Handling Capability: Z₀ = 50 Ω

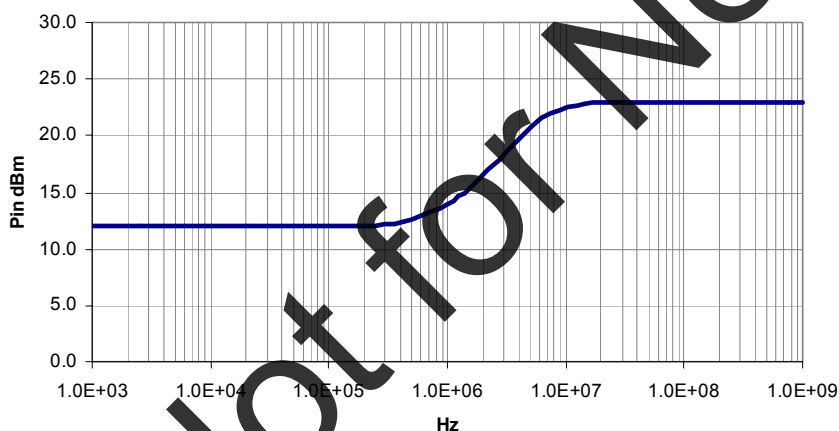


Table 7. Control Voltage

| State | Bias Condition |
|-------|------------------------------------|
| Low | 0 to +1.0 Vdc at 2 μ A (typ) |
| High | +2.6 to +5 Vdc at 10 μ A (typ) |

Table 8. Latch and Clock Specifications

| Latch Enable | Shift Clock | Function |
|--------------|-------------|---|
| 0 | \uparrow | Shift Register Clocked |
| \uparrow | X | Contents of shift register transferred to attenuator core |

Table 9. Parallel Truth Table

| Parallel Control Setting | | | | | | | Attenuation Setting RF1-RF2 |
|--------------------------|----|----|----|----|----|----|-----------------------------|
| D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| L | L | L | L | L | L | L | Reference I.L. |
| L | L | L | L | L | L | H | 0.25 dB |
| L | L | L | L | L | H | L | 0.5 dB |
| L | L | L | L | H | L | L | 1 dB |
| L | L | L | H | L | L | L | 2 dB |
| L | L | H | L | L | L | L | 4 dB |
| L | H | L | L | L | L | L | 8 dB |
| H | L | L | L | L | L | L | 16 dB |
| H | H | H | H | H | H | H | 31.75 dB |

Table 10. Serial Address Word Truth Table

| Address Word | | | | | | | | Address Setting |
|--------------|----|----|----|----|----|----|----|-----------------|
| A7 (MSB) | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| X | X | X | X | X | L | L | L | 000 |
| X | X | X | X | X | L | L | H | 001 |
| X | X | X | X | X | L | H | L | 010 |
| X | X | X | X | X | L | H | H | 011 |
| X | X | X | X | X | H | L | L | 100 |
| X | X | X | X | X | H | L | H | 101 |
| X | X | X | X | X | H | H | L | 110 |
| X | X | X | X | X | H | H | H | 111 |

Table 11. Serial Attenuation Word Truth Table

| Attenuation Word | | | | | | | | Attenuation Setting RF1-RF2 |
|------------------|----|----|----|----|----|----|----------|-----------------------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) | |
| L | L | L | L | L | L | L | L | Reference I.L. |
| L | L | L | L | L | L | L | H | 0.25 dB |
| L | L | L | L | L | L | H | L | 0.5 dB |
| L | L | L | L | L | H | L | L | 1 dB |
| L | L | L | L | H | L | L | L | 2 dB |
| L | L | L | H | L | L | L | L | 4 dB |
| L | L | H | L | L | L | L | L | 8 dB |
| L | H | L | L | L | L | L | L | 16 dB |
| L | H | H | H | H | H | H | H | 31.75 dB |

Table 12. Serial-Addressable Register Map

| | | | | | | | | | | | | | | | |
|--|-----|-----|-----|-----|-----|----|----|------------------|----|----|----|----|----|----|----|
| <div style="display: flex; justify-content: space-between; align-items: center;"> <div> <p>MSB (last in) \downarrow</p> </div> <div> <p>Bits can either be set to logic high or logic low</p> <p>D7 must be set to logic low</p> </div> <div> <p>LSB (first in) \downarrow</p> </div> </div> | | | | | | | | | | | | | | | |
| Q15 | Q14 | Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 |
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Address Word | | | | | | | | Attenuation Word | | | | | | | |

Attenuation Word is derived directly from the attenuation value. For example, to program the 18.25 dB state at address 3:

Address word: XXXXX011

Attenuation Word: Multiply by 4 and convert to binary $\rightarrow 4 * 18.25 \text{ dB} \rightarrow 73 \rightarrow 01001001$

Serial Input: XXXXX01101001001

Programming Options

Parallel/Serial Selection

Either a parallel or serial-addressable interface can be used to control the PE43703. The \bar{P}/S bit provides this selection, with $\bar{P}/S=LOW$ selecting the parallel interface and $\bar{P}/S=HIGH$ selecting the serial-addressable interface.

Parallel Mode Interface

The parallel interface consists of seven CMOS-compatible control lines that select the desired attenuation state, as shown in *Table 9*.

The parallel interface timing requirements are defined by *Fig. 30* (Parallel Interface Timing Diagram), *Table 9* (Parallel Interface AC Characteristics), and switching speed (*Table 1*).

For *latched*-parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per *Fig. 30*) to latch new attenuation state into device.

For *direct* parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardware, switches, or jumpers).

Serial-Addressable Interface

The serial-addressable interface is a 16-bit serial-in, parallel-out shift register buffered by a transparent latch. The 16-bits make up two words comprised of 8-bits each. The first word is the Attenuation Word, which controls the state of the DSA. The second word is the Address Word, which is compared to the static (or programmed) logical states of the A0, A1 and A2 digital inputs. If there is an address match, the DSA changes state; otherwise its current state will remain unchanged. *Fig. 29* illustrates an example timing diagram for programming a state. It is required that all parallel control inputs be grounded when the DSA is used in serial-addressable mode.

The serial-addressable interface is controlled using three CMOS-compatible signals: Serial-In (SI), Clock (CLK), and Latch Enable (LE). The SI and CLK inputs allow data to be serially entered into the

shift register. Serial data is clocked in LSB first, beginning with the Attenuation Word.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. Address Word and Attenuation Word truth tables are listed in *Table 10* & *Table 11*, respectively. A programming example of the serial-addressable register is illustrated in *Table 12*. The serial-addressable timing diagram is illustrated in *Fig. 29*.

Power-up Control Settings

The PE43703 will always initialize to the maximum attenuation setting (31.75 dB) on power-up for both the serial-addressable and latched-parallel modes of operation and will remain in this setting until the user latches in the next programming word. In direct-parallel mode, the DSA can be preset to any state within the 31.75 dB range by pre-setting the parallel control pins prior to power-up. In this mode, there is a 400- μ s delay between the time the DSA is powered-up to the time the desired state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (31.75 dB) before defaulting to the user defined state. If the control pins are left floating in this mode during power-up, the device will default to the minimum attenuation setting (insertion loss state).

Dynamic operation between serial-addressable and parallel programming modes is possible.

If the DSA powers up in serial-addressable mode ($\bar{P}/S = HIGH$), all the parallel control inputs DI[6:0] must be set to logic low. Prior to toggling to parallel mode, the DSA *must* be programmed serially to ensure D[7] is set to logic low.

If the DSA powers up in either latched or direct-parallel mode, all parallel pins DI[6:0] must be set to logic low prior to toggling to serial-addressable mode ($\bar{P}/S = HIGH$), and *held* low until the DSA has been programmed serially to ensure bit D[7] is set to logic low.

The sequencing is only required once on power-up. Once completed, the DSA may be toggled between serial-addressable and parallel programming modes at will.

Figure 29. Serial-Addressable Timing Diagram

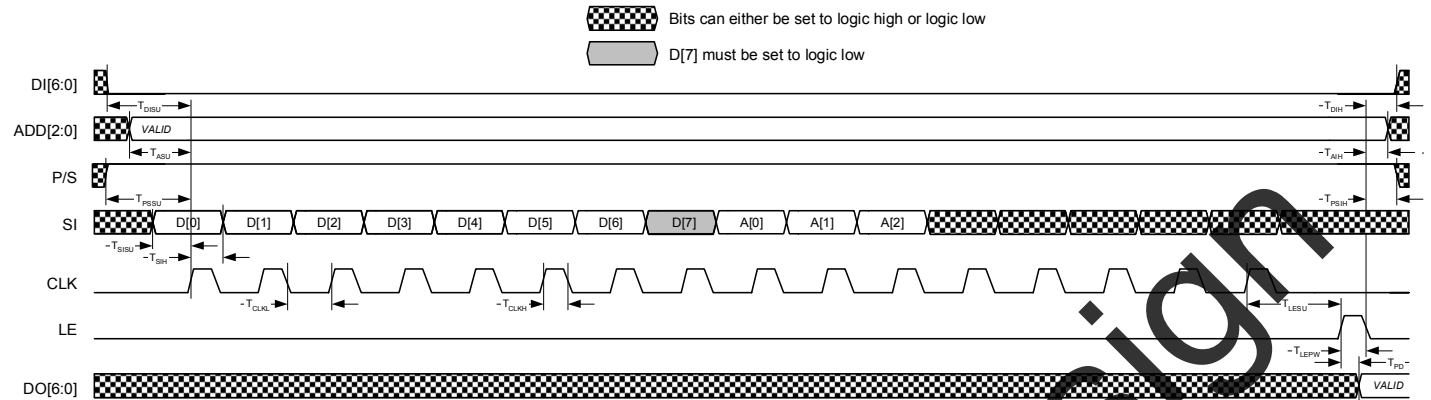


Figure 30. Latched-Parallel/Direct-Parallel Timing Diagram

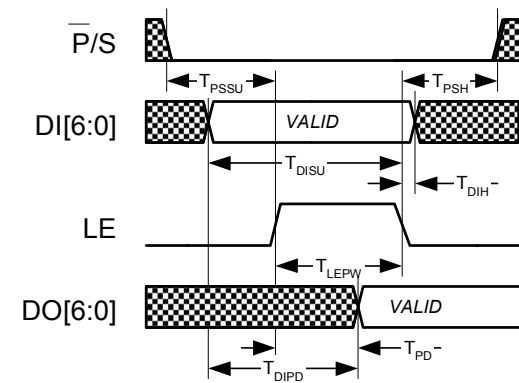


Table 13. Serial-Addressable Interface AC Characteristics

$V_{DD} = 3.3$ or 5.0 V, $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$, unless otherwise specified

| Symbol | Parameter | Min | Max | Unit |
|------------|--|-----|-----|------|
| F_{CLK} | Serial clock frequency | - | 10 | MHz |
| T_{CLKH} | Serial clock HIGH time | 30 | - | ns |
| T_{CLKL} | Serial clock LOW time | 30 | - | ns |
| T_{LESU} | Last serial clock rising edge setup time to Latch Enable rising edge | 10 | - | ns |
| T_{LEPW} | Latch Enable min. pulse width | 30 | - | ns |
| T_{SISU} | Serial data setup time | 10 | - | ns |
| T_{SIH} | Serial data hold time | 10 | - | ns |
| T_{DISU} | Parallel data setup time | 100 | - | ns |
| T_{DIH} | Parallel data hold time | 100 | - | ns |
| T_{ASU} | Address setup time | 100 | - | ns |
| T_{AH} | Address hold time | 100 | - | ns |
| T_{PSSU} | Parallel/Serial setup time | 100 | - | ns |
| T_{PSH} | Parallel/Serial hold time | 100 | - | ns |
| T_{PD} | Digital register delay (internal) | - | 10 | ns |

Table 14. Parallel and Direct Interface AC Characteristics

$V_{DD} = 3.3$ or 5.0 V, $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$, unless otherwise specified

| Symbol | Parameter | Min | Max | Unit |
|------------|---|-----|-----|------|
| T_{LEPW} | Latch Enable minimum pulse width | 30 | - | ns |
| T_{DISU} | Parallel data setup time | 100 | - | ns |
| T_{DIH} | Parallel data hold time | 100 | - | ns |
| T_{PSSU} | Parallel/Serial setup time | 100 | - | ns |
| T_{PSIH} | Parallel/Serial hold time | 100 | - | ns |
| T_{PD} | Digital register delay (internal) | - | 10 | ns |
| T_{DIPD} | Digital register delay (internal, direct mode only) | - | 5 | ns |

Evaluation Kit

The Digital Attenuator Evaluation Kit board was designed to ease customer evaluation of the PE43703 Digital Step Attenuator.

Direct-Parallel Programming Procedure

For automated direct-parallel programming, connect the test harness provided with the EVK from the parallel port of the PC to the J1 & Serial header pin and set the D0-D6 SP3T switches to the 'MIDDLE' toggle position. Position the Parallel/Serial (\bar{P}/S) select switch to the Parallel (or left) position. The evaluation software is written to operate the DSA in either Parallel or Serial-Addressable Mode. Ensure that the software is set to program in *Direct-Parallel* mode. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

For manual direct-parallel programming, disconnect the test harness provided with the EVK from the J1 and Serial header pins. Position the Parallel/Serial (\bar{P}/S) select switch to the Parallel (or left) position. The LE pin on the Serial header must be tied to V_{DD} . Switches D0-D6 are SP3T switches which enable the user to manually program the parallel bits. When any input D0-D6 is toggled 'UP', logic high is presented to the parallel input. When toggled 'DOWN', logic low is presented to the parallel input. Setting D0-D6 to the 'MIDDLE' toggle position presents an OPEN, which forces an on-chip logic low. Table 9 depicts the parallel programming truth table and Fig. 30 illustrates the parallel programming timing diagram.

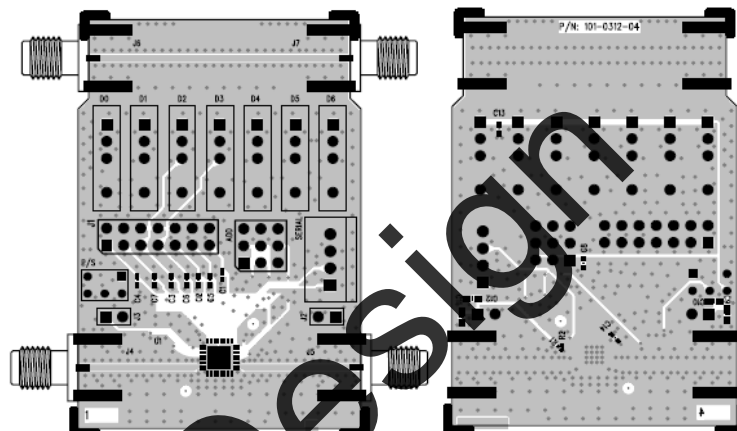
Latched-Parallel Programming Procedure

For automated latched-parallel programming, the procedure is identical to the direct-parallel method. The user only must ensure that *Latched-Parallel* is selected in the software.

For manual latched-parallel programming, the procedure is identical to direct-parallel except now the LE pin on the Serial header must be logic low as the parallel bits are applied. The user must then pulse LE from 0V to V_{DD} and back to 0V to latch the programming word into the DSA. LE must be logic low prior to programming the next word.

Figure 31. Evaluation Board Layout

Peregrine Specification 101-0312



Note: Reference Fig. 32 for Evaluation Board Schematic

Serial-Addressable Programming Procedure

Position the Parallel/Serial (\bar{P}/S) select switch to the Serial (or right) position. Prior to programming, the user must define an address setting using the ADD header pin. Jump the middle pins on the ADD header A0-A2 (or lower) row of pins to set logic high, or jump the middle pins to the upper row of pins to set logic low. If the ADD pins are left open, then 000 become the default address. The evaluation software is written to operate the DSA in either Parallel or Serial-Addressable Mode. Ensure that the software is set to program in *Serial-Addressable* mode. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

Figure 32. Evaluation Board Schematic
Peregrine Specification 102-0381

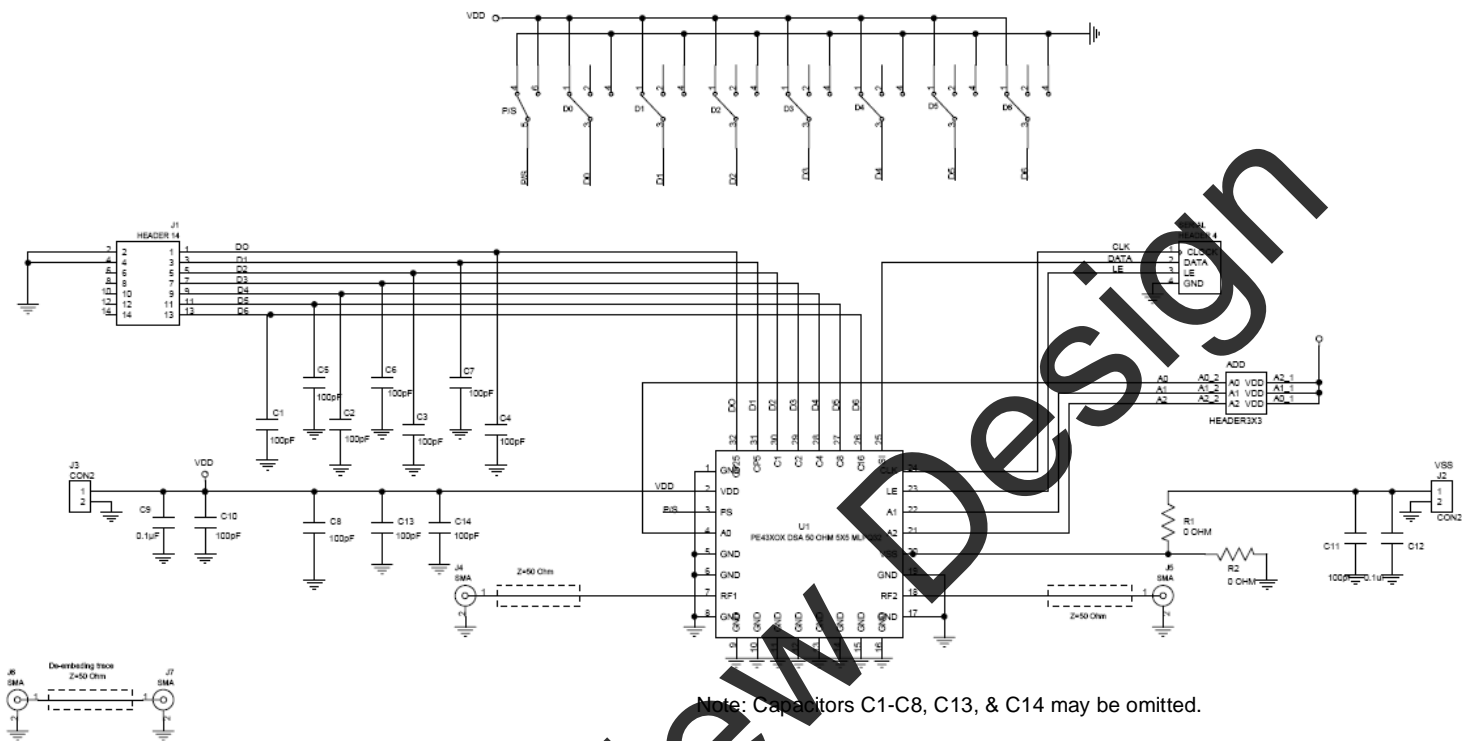
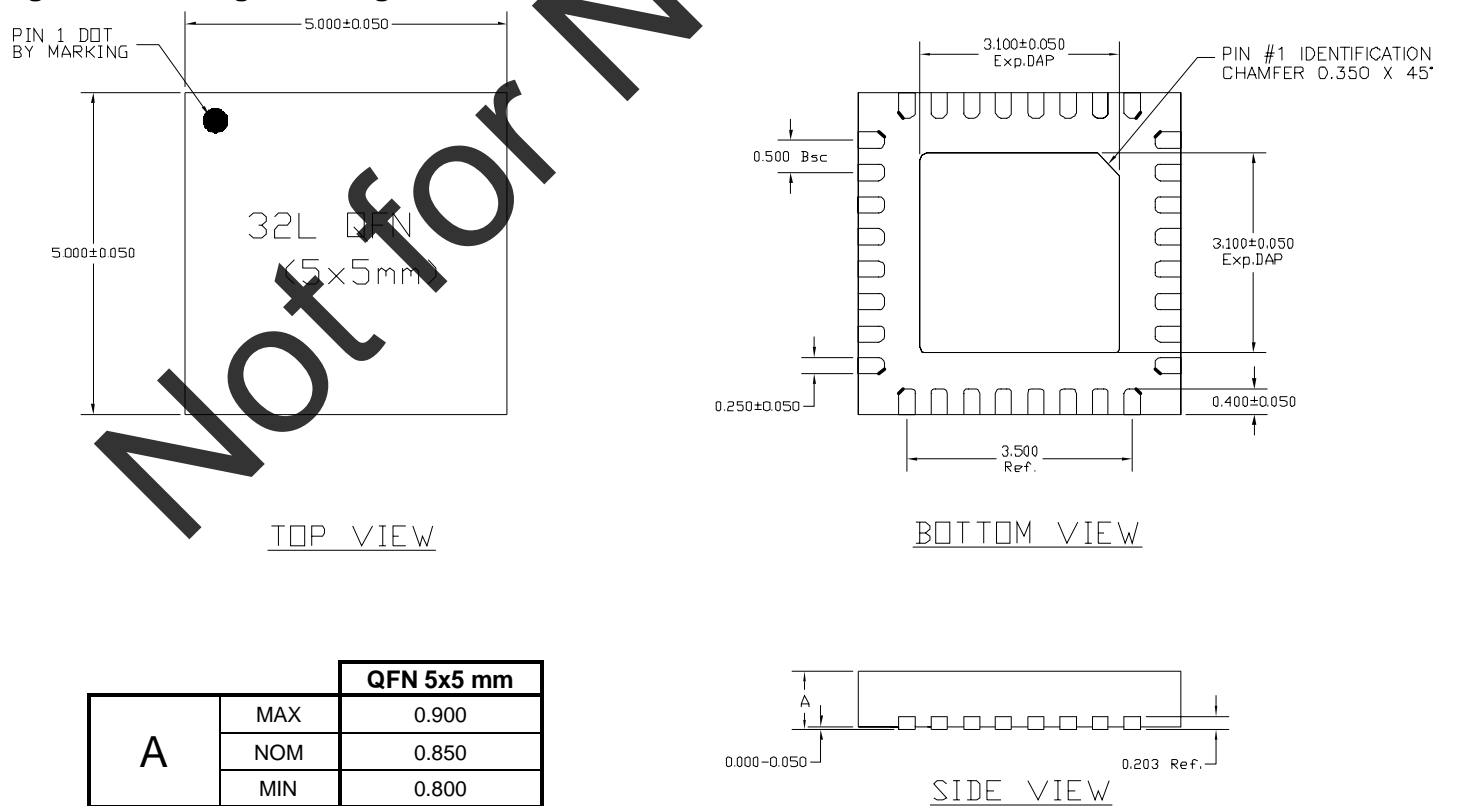


Figure 33. Package Drawing



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