



### REVISION HISTORY

| <u>Revision</u> | <u>Description</u>                                                                                                                                                                                                                                                                                                                                                         | <u>Issue Date</u> |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
| Rev. 1.0        | Initial Issue                                                                                                                                                                                                                                                                                                                                                              | Dec.01.2006       |
| Rev. 1.1        | Revised $V_{IH}$ to TTL compatible                                                                                                                                                                                                                                                                                                                                         | Jan.09.2008       |
| Rev. 1.2        | Revised $V_{IH}$ to $0.7 \cdot V_{CC}$                                                                                                                                                                                                                                                                                                                                     | May.06.2008       |
| Rev. 1.3        | Revised $V_{DR}$                                                                                                                                                                                                                                                                                                                                                           | Mar.03.2009       |
| Rev. 1.4        | Revised $V_{TERM}$ to $V_{T1}$ and $V_{T2}$<br>Revised Test Condition of $I_{SB1}/I_{DR}$<br>Revised <b>FEATURES &amp; ORDERING INFORMATION</b><br><b>Lead free and green package available to Green package available</b><br>Added packing type in <b>ORDERING INFORMATION</b><br>Deleted $T_{SOLDER}$ in <b>ABSOLUTE MAXIMUM RATINGS</b><br>Adding PKG type : 32 TSOP-II | Aug.05.2009       |
| Rev. 1.5        | Revised <b>PACKAGE OUTLINE DIMENSION</b> in page 9/10/11                                                                                                                                                                                                                                                                                                                   | May.07.2010       |
| Rev. 1.6        | Revised typo in <b>PIN CONFIGURATION</b>                                                                                                                                                                                                                                                                                                                                   | Jul.21.2010       |
| Rev. 1.7        | Revised <b>ORDERING INFORMATION</b> in page 12<br>Revised <b>PACKAGE OUTLINE DIMENSION</b> in page 8/12                                                                                                                                                                                                                                                                    | Aug.25.2010       |
| Rev. 1.8        | Revised typo in <b>REVISION HISTORY</b><br><b>ORDERING INFORMATION</b> in page 12 to 13                                                                                                                                                                                                                                                                                    | Oct.29.2010       |
| Rev. 1.9        | Added SL Grade<br>Deleted E Grade<br>Revised $I_{SB1}/I_{DR}$                                                                                                                                                                                                                                                                                                              | Aug.09.2011       |
| Rev. 1.10       | Added PKG type : 32 P-DIP                                                                                                                                                                                                                                                                                                                                                  | Nov.24.2011       |
| Rev. 1.11       | Revised "Standby Power Supply Current" in page 4<br>Revised "Data Retention Current" in page 8                                                                                                                                                                                                                                                                             | Apr.30.2012       |
| Rev. 1.12       | Revised <b>TEST CONDITION</b> of $I_{CC}/I_{CC1}/I_{SB1}$ in<br><b>DC ELECTRICAL CHARACTERISTICS</b> (page 4)<br>and $I_{DR}$ in <b>DATA RETENTION CHARACTERISTICS</b> (page 8)<br><b>ORDERING INFORMATION</b> (page16)                                                                                                                                                    | Jun.02.2015       |
| Rev. 1.13       | Deleted <b>WRITE CYCLE</b> Notes :<br>1. $WE\#, CE\#$ must be high during all address transitions. in page 7                                                                                                                                                                                                                                                               | Jun.29.2016       |
| Rev. 1.14       | Revised <b>GENERAL DESCRIPTION</b> in page 1                                                                                                                                                                                                                                                                                                                               | Apr.24.2017       |

### FEATURES

- Fast access time : 55/70ns
- Low power consumption:  
Operating current : 30/20mA (TYP.)  
Standby current : 4μA (TYP.) LL-version  
3μA (TYP.) SL-version
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450mil SOP  
32-pin 600mil PDIP  
32-pin 8mm x 20mm TSOP I  
32-pin 400mil TSOP II  
32-pin 8mm x 13.4mm sTSOP  
36-ball 6mm x 8mm TFBGA

### GENERAL DESCRIPTION

The LY62W5128 is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

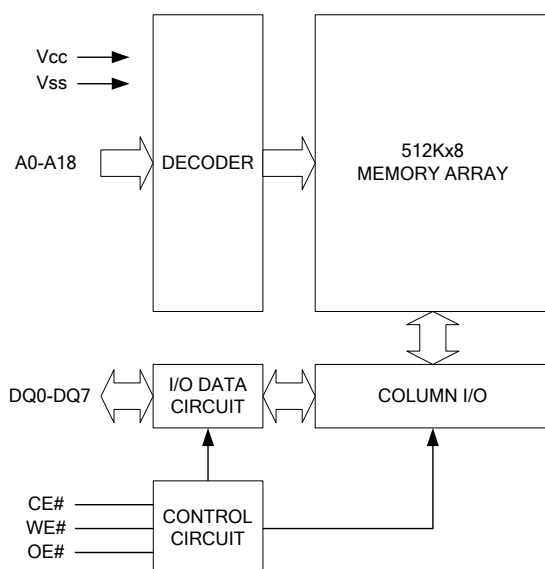
The LY62W5128 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62W5128 operates from a single power supply of 2.7V ~ 5.5V and all outputs are fully TTL compatible.

### PRODUCT FAMILY

| Product Family | Operating Temperature | V <sub>CC</sub> Range | Speed   | Power Dissipation                |                                   |
|----------------|-----------------------|-----------------------|---------|----------------------------------|-----------------------------------|
|                |                       |                       |         | Standby(I <sub>SB1</sub> , TYP.) | Operating(I <sub>CC</sub> , TYP.) |
| LY62W5128      | 0 ~ 70°C              | 2.7 ~ 5.5V            | 55/70ns | 4μA(LL)/3μA(SL)                  | 30/20mA                           |
| LY62W5128(I)   | -40 ~ 85°C            | 2.7 ~ 5.5V            | 55/70ns | 4μA(LL)/3μA(SL)                  | 30/20mA                           |

### FUNCTIONAL BLOCK DIAGRAM

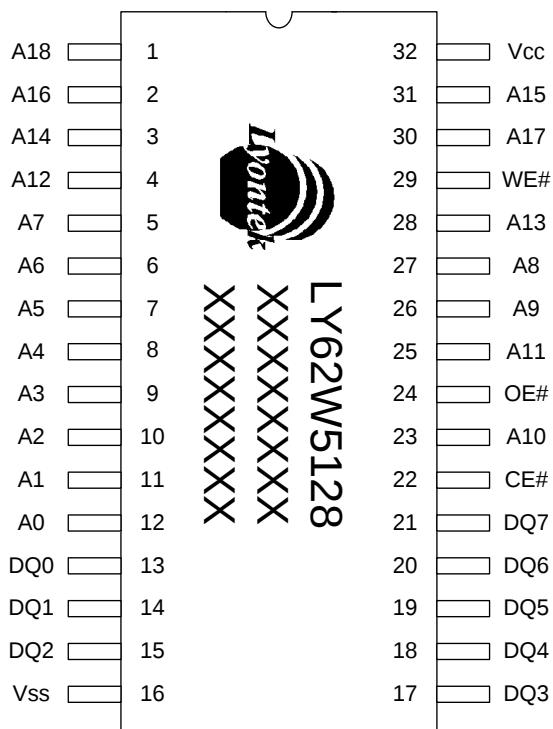


### PIN DESCRIPTION

| SYMBOL          | DESCRIPTION         |
|-----------------|---------------------|
| A0 - A18        | Address Inputs      |
| DQ0 - DQ7       | Data Inputs/Outputs |
| CE#             | Chip Enable Inputs  |
| WE#             | Write Enable Input  |
| OE#             | Output Enable Input |
| V <sub>CC</sub> | Power Supply        |
| V <sub>SS</sub> | Ground              |
| NC              | No Connection       |



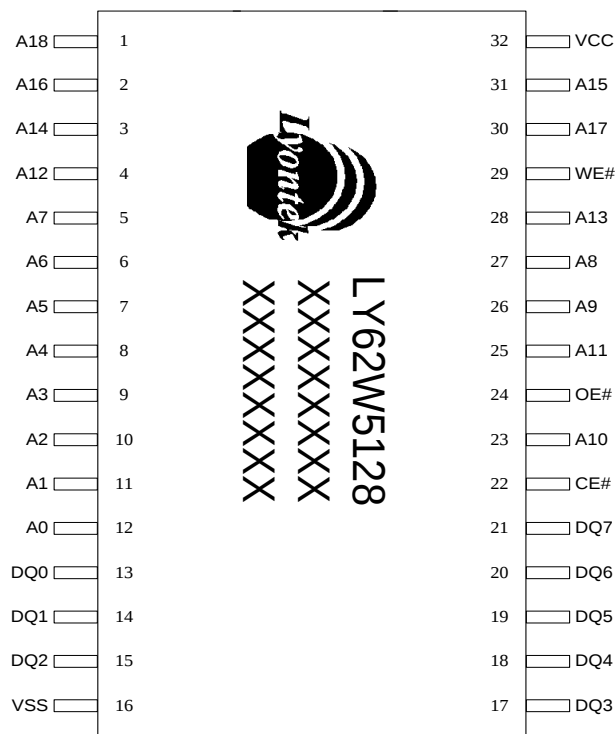
#### PIN CONFIGURATION



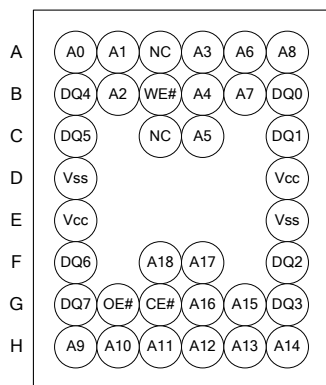
SOP / PDIP



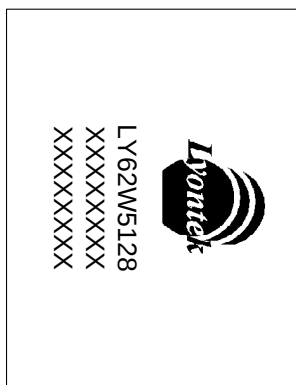
TSOP I / sTSOP



TSOP II



TFBGA(See through with Top View)



TFBGA(Top View)

**ABSOLUTE MAXIMUM RATINGS\***

| PARAMETER                                     | SYMBOL    | RATING                                 | UNIT |
|-----------------------------------------------|-----------|----------------------------------------|------|
| Voltage on $V_{CC}$ relative to $V_{SS}$      | $V_{T1}$  | -0.5 to 6.5                            | V    |
| Voltage on any other pin relative to $V_{SS}$ | $V_{T2}$  | -0.5 to $V_{CC}+0.5$                   | V    |
| Operating Temperature                         | $T_A$     | 0 to 70(C grade)<br>-40 to 85(I grade) | °C   |
| Storage Temperature                           | $T_{STG}$ | -65 to 150                             | °C   |
| Power Dissipation                             | $P_D$     | 1                                      | W    |
| DC Output Current                             | $I_{OUT}$ | 50                                     | mA   |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

| MODE           | CE# | OE# | WE# | I/O OPERATION | SUPPLY CURRENT    |
|----------------|-----|-----|-----|---------------|-------------------|
| Standby        | H   | X   | X   | High-Z        | $I_{SB1}$         |
| Output Disable | L   | H   | H   | High-Z        | $I_{CC}, I_{CC1}$ |
| Read           | L   | L   | H   | $D_{OUT}$     | $I_{CC}, I_{CC1}$ |
| Write          | L   | X   | L   | $D_{IN}$      | $I_{CC}, I_{CC1}$ |

Note: H =  $V_{IH}$ , L =  $V_{IL}$ , X = Don't care.



#### DC ELECTRICAL CHARACTERISTICS

| PARAMETER                              | SYMBOL                        | TEST CONDITION                                                                                                          |                   | MIN.                | TYP. <sup>*4</sup> | MAX.                 | UNIT |    |
|----------------------------------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------|-------------------|---------------------|--------------------|----------------------|------|----|
| Supply Voltage                         | V <sub>CC</sub>               |                                                                                                                         |                   | 2.7                 | 3.0                | 5.5                  | V    |    |
| Input High Voltage                     | V <sub>IH</sub> <sup>*1</sup> |                                                                                                                         |                   | 0.7*V <sub>CC</sub> | -                  | V <sub>CC</sub> +0.3 | V    |    |
| Input Low Voltage                      | V <sub>IL</sub> <sup>*2</sup> |                                                                                                                         |                   | - 0.2               | -                  | 0.6                  | V    |    |
| Input Leakage Current                  | I <sub>LI</sub>               | V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>                                                                     |                   | - 1                 | -                  | 1                    | μA   |    |
| Output Leakage Current                 | I <sub>LO</sub>               | V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> ,<br>Output Disabled                                               |                   | - 1                 | -                  | 1                    | μA   |    |
| Output High Voltage                    | V <sub>OH</sub>               | I <sub>OH</sub> = -1mA                                                                                                  |                   | 2.4                 | 2.7                | -                    | V    |    |
| Output Low Voltage                     | V <sub>OL</sub>               | I <sub>OL</sub> = 2mA                                                                                                   |                   | -                   | -                  | 0.4                  | V    |    |
| Average Operating Power supply Current | I <sub>CC</sub>               | Cycle time = MIN.<br>CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA<br>Other pins at V <sub>IL</sub> or V <sub>IH</sub> |                   | - 55                | -                  | 30                   | 60   | mA |
|                                        |                               |                                                                                                                         |                   | - 70                | -                  | 20                   | 50   | mA |
|                                        | I <sub>CC1</sub>              | Cycle time = 1μs<br>CE# ≤ 0.2V, I <sub>I/O</sub> = 0mA<br>Other pins at 0.2V or V <sub>CC</sub> -0.2V                   |                   | -                   | 4                  | 10                   | mA   |    |
| Standby Power Supply Current           | I <sub>SB1</sub>              | CE# ≥ V <sub>CC</sub> -0.2V                                                                                             |                   | LL/LLI              | -                  | 4                    | 50   | μA |
|                                        |                               | Others at 0.2V or V <sub>CC</sub> - 0.2V                                                                                | SL <sup>*5</sup>  | 25°C                | -                  | 3                    | 10   | μA |
|                                        |                               |                                                                                                                         | SLI <sup>*5</sup> | 40°C                | -                  | 3                    | 10   | μA |
|                                        |                               |                                                                                                                         |                   |                     | SL/SLI             | -                    | 3    | 25 |

Notes:

- $V_{IH}(\max) = V_{CC} + 3.0V$  for pulse width less than 10ns.
- $V_{IL}(\min) = V_{SS} - 3.0V$  for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at  $V_{CC} = V_{CC}(\text{TYP.})$  and  $T_A = 25^\circ C$
- This parameter is measured at  $V_{CC} = 3.0V$

#### CAPACITANCE ( $T_A = 25^\circ C$ , $f = 1.0MHz$ )

| PARAMETER                | SYMBOL    | MIN. | MAX. | UNIT |
|--------------------------|-----------|------|------|------|
| Input Capacitance        | $C_{IN}$  | -    | 6    | pF   |
| Input/Output Capacitance | $C_{I/O}$ | -    | 8    | pF   |

Note : These parameters are guaranteed by device characterization, but not production tested.

#### AC TEST CONDITIONS

|                                          |                                                  |
|------------------------------------------|--------------------------------------------------|
| Input Pulse Levels                       | 0.2V to $V_{CC} - 0.2V$                          |
| Input Rise and Fall Times                | 3ns                                              |
| Input and Output Timing Reference Levels | 1.5V                                             |
| Output Load                              | $C_L = 30pF + 1TTL$ , $I_{OH}/I_{OL} = -2mA/4mA$ |



### AC ELECTRICAL CHARACTERISTICS

#### (1) READ CYCLE

| PARAMETER                          | SYM.               | LY62W5128-55 |      | LY62W5128-70 |      | UNIT |
|------------------------------------|--------------------|--------------|------|--------------|------|------|
|                                    |                    | MIN.         | MAX. | MIN.         | MAX. |      |
| Read Cycle Time                    | t <sub>RC</sub>    | 55           | -    | 70           | -    | ns   |
| Address Access Time                | t <sub>AA</sub>    | -            | 55   | -            | 70   | ns   |
| Chip Enable Access Time            | t <sub>ACE</sub>   | -            | 55   | -            | 70   | ns   |
| Output Enable Access Time          | t <sub>OE</sub>    | -            | 30   | -            | 35   | ns   |
| Chip Enable to Output in Low-Z     | t <sub>CLZ</sub> * | 10           | -    | 10           | -    | ns   |
| Output Enable to Output in Low-Z   | t <sub>OLZ</sub> * | 5            | -    | 5            | -    | ns   |
| Chip Disable to Output in High-Z   | t <sub>CHZ</sub> * | -            | 20   | -            | 25   | ns   |
| Output Disable to Output in High-Z | t <sub>OHZ</sub> * | -            | 20   | -            | 25   | ns   |
| Output Hold from Address Change    | t <sub>OH</sub>    | 10           | -    | 10           | -    | ns   |

#### (2) WRITE CYCLE

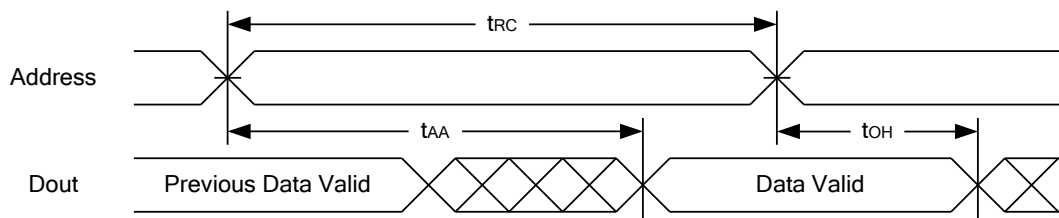
| PARAMETER                        | SYM.               | LY62W5128-55 |      | LY62W5128-70 |      | UNIT |
|----------------------------------|--------------------|--------------|------|--------------|------|------|
|                                  |                    | MIN.         | MAX. | MIN.         | MAX. |      |
| Write Cycle Time                 | t <sub>WC</sub>    | 55           | -    | 70           | -    | ns   |
| Address Valid to End of Write    | t <sub>AW</sub>    | 50           | -    | 60           | -    | ns   |
| Chip Enable to End of Write      | t <sub>CW</sub>    | 50           | -    | 60           | -    | ns   |
| Address Set-up Time              | t <sub>AS</sub>    | 0            | -    | 0            | -    | ns   |
| Write Pulse Width                | t <sub>WP</sub>    | 45           | -    | 55           | -    | ns   |
| Write Recovery Time              | t <sub>WR</sub>    | 0            | -    | 0            | -    | ns   |
| Data to Write Time Overlap       | t <sub>DW</sub>    | 25           | -    | 30           | -    | ns   |
| Data Hold from End of Write Time | t <sub>DH</sub>    | 0            | -    | 0            | -    | ns   |
| Output Active from End of Write  | t <sub>OW</sub> *  | 5            | -    | 5            | -    | ns   |
| Write to Output in High-Z        | t <sub>WHZ</sub> * | -            | 20   | -            | 25   | ns   |

\*These parameters are guaranteed by device characterization, but not production tested.

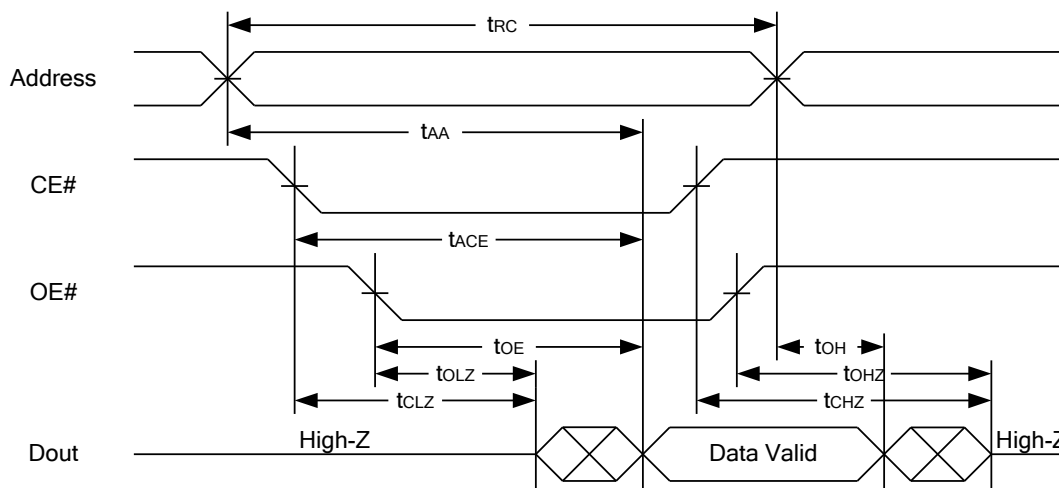


### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)



#### READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

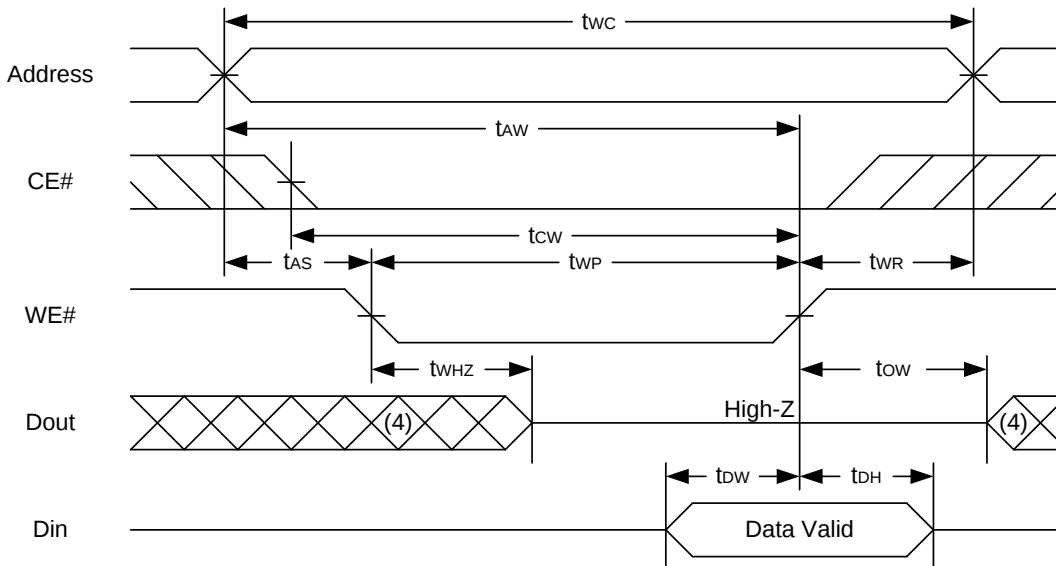


#### Notes :

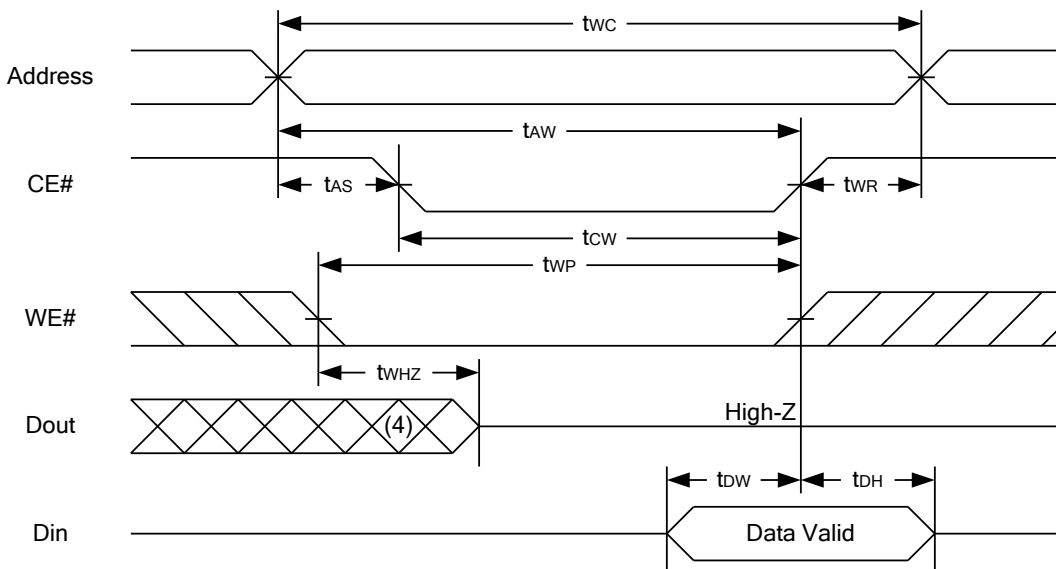
- 1.WE# is high for read cycle.
- 2.Device is continuously selected OE# = low, CE# = low.
- 3.Address must be valid prior to or coincident with CE# = low,; otherwise tAA is the limiting parameter.
- 4.tCLZ, tOLZ, tCHZ and toHZ are specified with CL = 5pF. Transition is measured  $\pm 500\text{mV}$  from steady state.
- 5.At any given temperature and voltage condition, tCHZ is less than tCLZ , toHZ is less than tOLZ.



#### WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



#### WRITE CYCLE 2 (CE# Controlled) (1,4,5)



#### Notes :

1. A write occurs during the overlap of a low CE#, low WE#.
2. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{OW}$  to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.

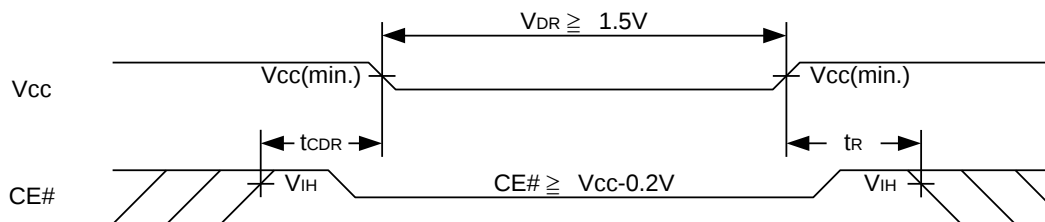


### DATA RETENTION CHARACTERISTICS

| PARAMETER                           | SYMBOL           | TEST CONDITION                                                                                             | MIN.              | TYP. | MAX. | UNIT       |
|-------------------------------------|------------------|------------------------------------------------------------------------------------------------------------|-------------------|------|------|------------|
| V <sub>CC</sub> for Data Retention  | V <sub>DR</sub>  | CE# $\geq$ V <sub>CC</sub> - 0.2V or CE2 $\leq$ 0.2V                                                       | 1.5               | -    | 5.5  | V          |
| Data Retention Current              | I <sub>DR</sub>  | V <sub>CC</sub> = 1.5V<br>CE# $\geq$ V <sub>CC</sub> - 0.2V<br>Other pins at 0.2V or V <sub>CC</sub> -0.2V | LL/LLI            | -    | 2    | 30 $\mu$ A |
|                                     |                  |                                                                                                            | SL 25°C           | -    | 2    | 8 $\mu$ A  |
|                                     |                  |                                                                                                            | SLI 40°C          | -    | 2    | 8 $\mu$ A  |
|                                     |                  |                                                                                                            | SL/SLI            | -    | 2    | 23 $\mu$ A |
| Chip Disable to Data Retention Time | t <sub>CDR</sub> | See Data Retention Waveforms (below)                                                                       | 0                 | -    | -    | ns         |
| Recovery Time                       | t <sub>R</sub>   |                                                                                                            | t <sub>RC</sub> * | -    | -    | ns         |

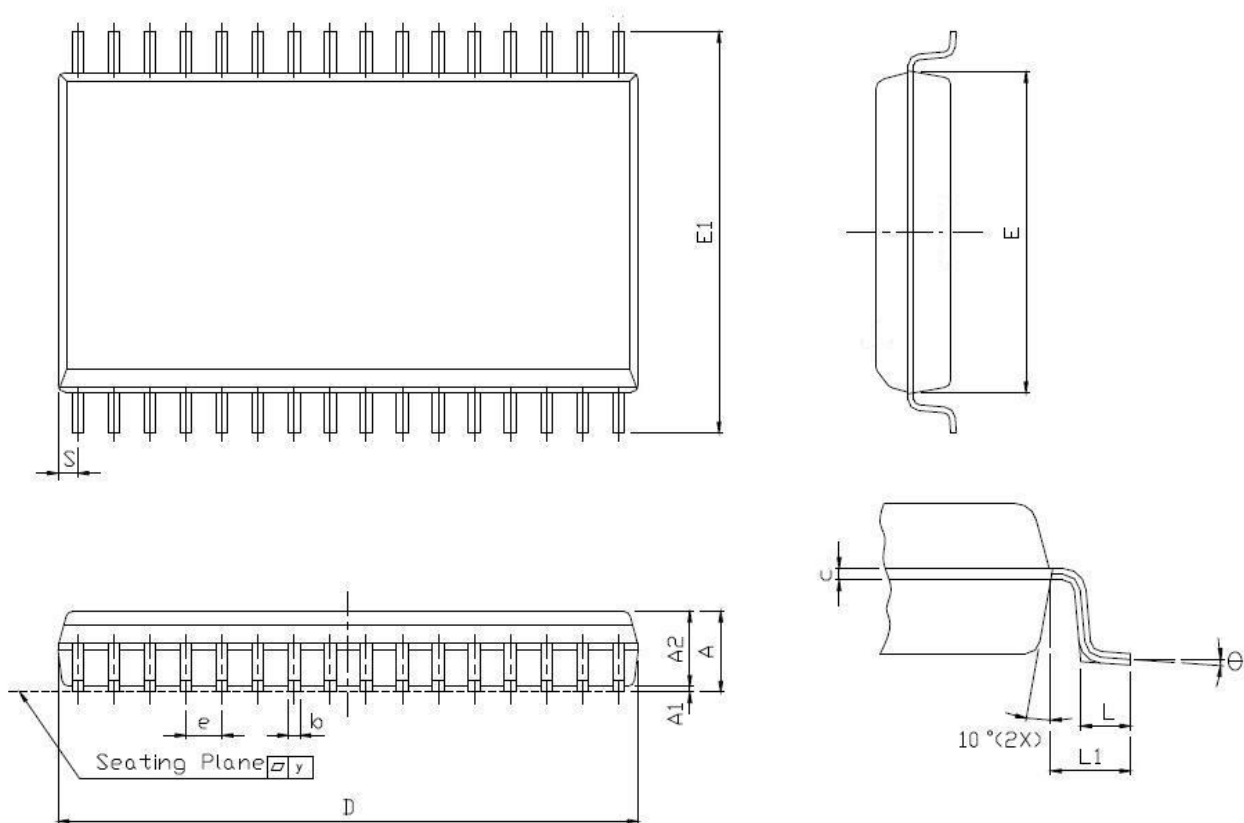
t<sub>RC</sub>\* = Read Cycle Time

### DATA RETENTION WAVEFORM



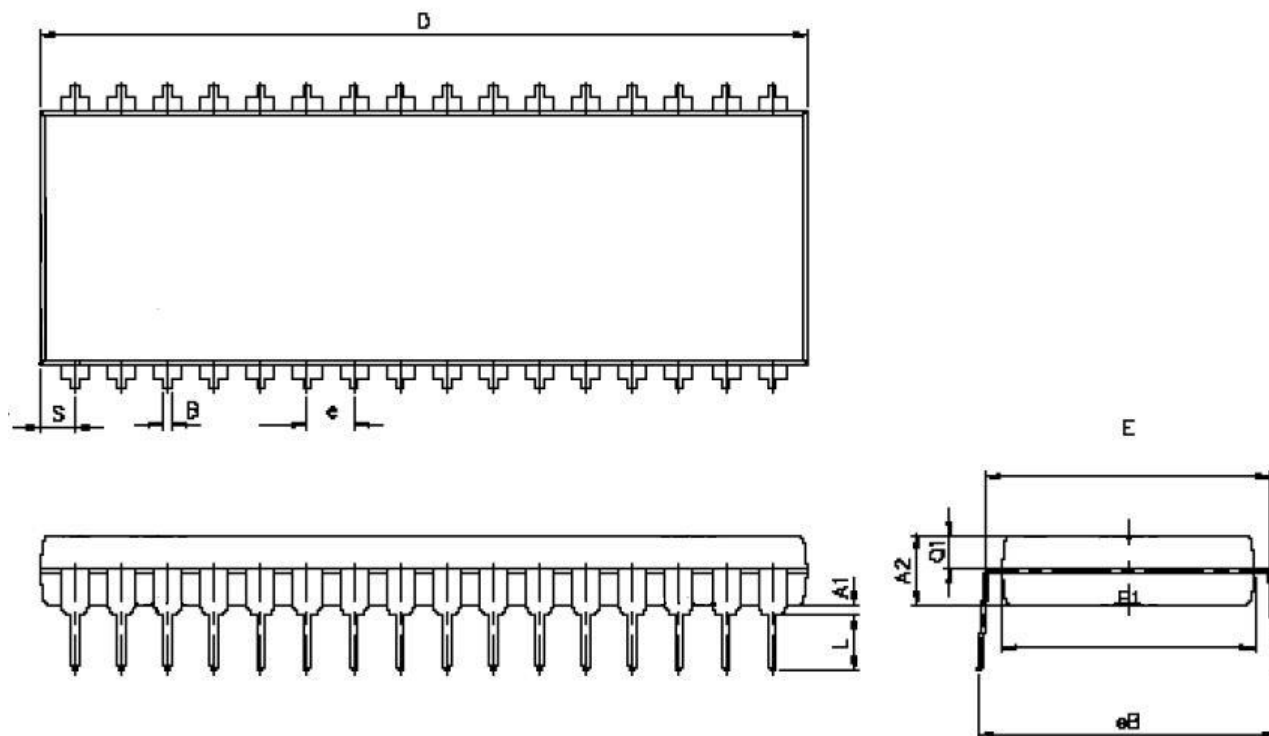
#### PACKAGE OUTLINE DIMENSION

##### 32-pin 450 mil SOP Package Outline Dimension



| SYMBOL | UNIT | INCH.(BASE) | MM(REF)      |
|--------|------|-------------|--------------|
| A      |      | 0.120(MAX)  | 3.048(MAX)   |
| A1     |      | 0.004(MIN)  | 0.102(MIN)   |
| A2     |      | 0.116(MAX)  | 2.946(MAX)   |
| b      |      | 0.016(TYP)  | 0.406(TYP)   |
| c      |      | 0.008(TYP)  | 0.203(TYP)   |
| D      |      | 0.817(MAX)  | 20.75(MAX)   |
| E      |      | 0.445±0.006 | 11.303±0.152 |
| E1     |      | 0.555±0.025 | 14.097±0.635 |
| e      |      | 0.050(TYP)  | 1.270(TYP)   |
| L      |      | 0.033±0.017 | 0.838±0.432  |
| L1     |      | 0.055±0.008 | 1.397±0.203  |
| S      |      | 0.026(MAX)  | 0.660(MAX)   |
| y      |      | 0.004(MAX)  | 0.101(MAX)   |
| Θ      |      | 0° -10°     | 0° -10°      |

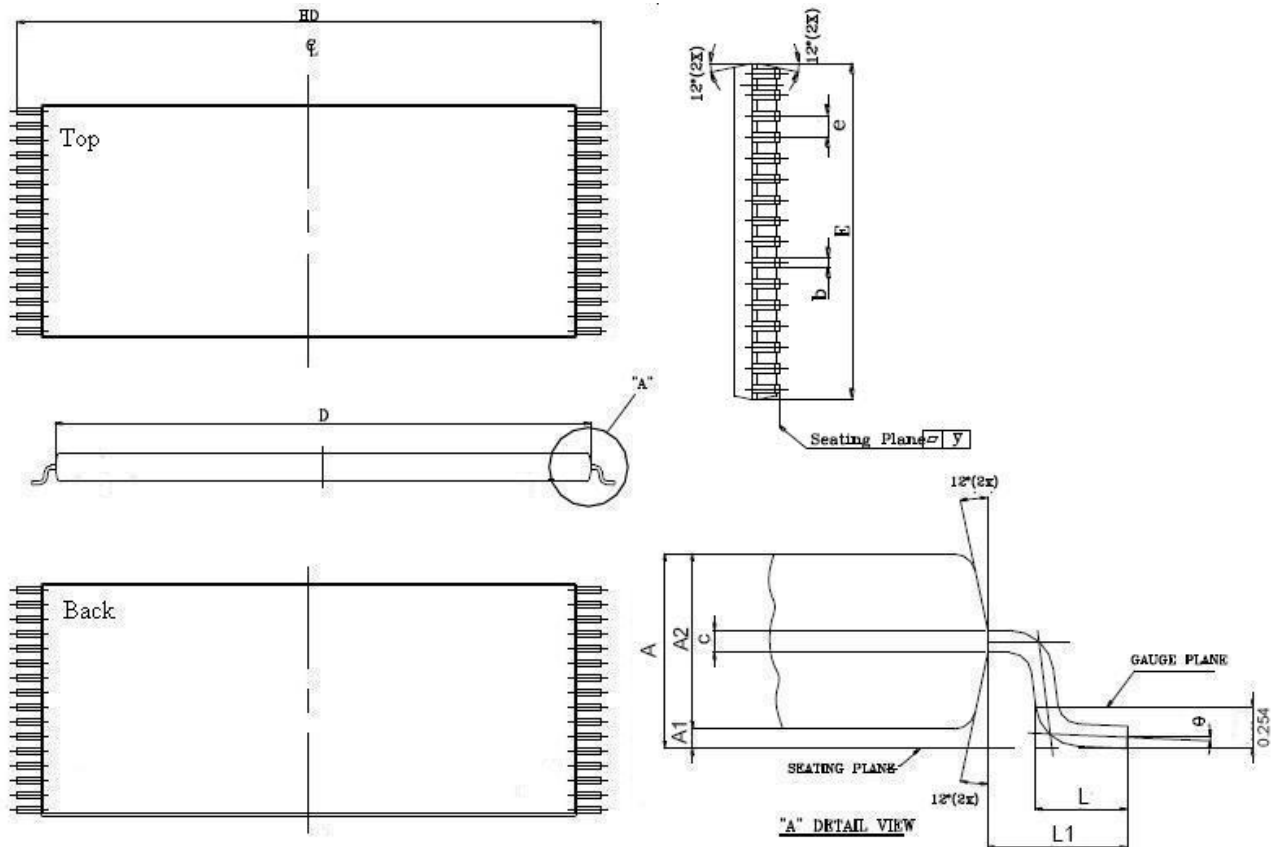
#### 32-pin 600 mil PDIP Package Outline Dimension



| SYM. | UNIT | INCH(BASE)  | MM(REF)       |
|------|------|-------------|---------------|
| A1   |      | 0.015(MIN)  | 0.381(MIN)    |
| A2   |      | 0.155±0.005 | 3.937±0.127   |
| B    |      | 0.018±0.005 | 0.457±0.127   |
| D    |      | 1.650±0.01  | 41.910±0.254  |
| E    |      | 0.600±0.010 | 15.240±0.254  |
| E1   |      | 0.545±0.005 | 13.843±0.127  |
| e    |      | 0.100(TYP)  | 2.540(TYP)    |
| eB   |      | 0.650±0.020 | 16.510±0.508. |
| L    |      | 0.158±0.043 | 4.013±1.092   |
| S    |      | 0.075±0.010 | 1.905±0.254   |
| Q1   |      | 0.070±0.005 | 1.778±0.127   |

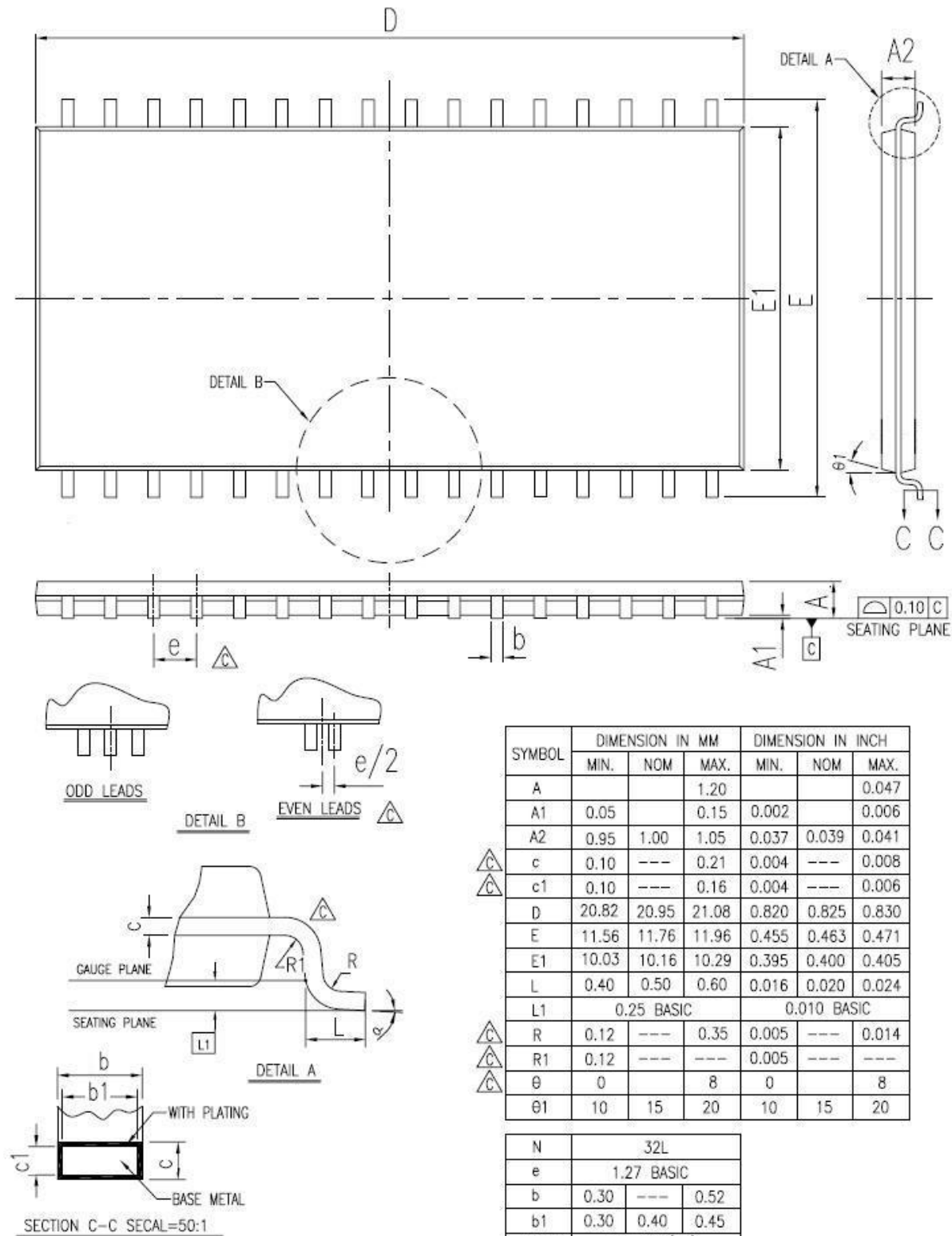
Note : D/E1/S dimension do not include mold flash.

#### 32-pin 8mm x 20mm TSOP I Package Outline Dimension



| SYM. | UNIT | INCH(BASE)    | MM(REF)      |
|------|------|---------------|--------------|
| A    |      | 0.047 (MAX)   | 1.20 (MAX)   |
| A1   |      | 0.004 ±0.002  | 0.10 ±0.05   |
| A2   |      | 0.039 ±0.002  | 1.00 ±0.05   |
| b    |      | 0.009 ±0.002  | 0.22 ±0.05   |
| c    |      | 0.006 ±0.002  | 0.155 ±0.055 |
| D    |      | 0.724 ±0.008  | 18.40 ±0.20  |
| E    |      | 0.315 ±0.008  | 8.00 ±0.20   |
| e    |      | 0.020 (TYP)   | 0.50 (TYP)   |
| HD   |      | 0.787 ±0.008  | 20.00 ±0.20  |
| L    |      | 0.024 ±0.004  | 0.60 ±0.10   |
| L1   |      | 0.0315 ±0.004 | 0.08 ±0.10   |
| y    |      | 0.003 (MAX)   | 0.08 (MAX)   |
| Θ    |      | 0°~5°         | 0°~5°        |

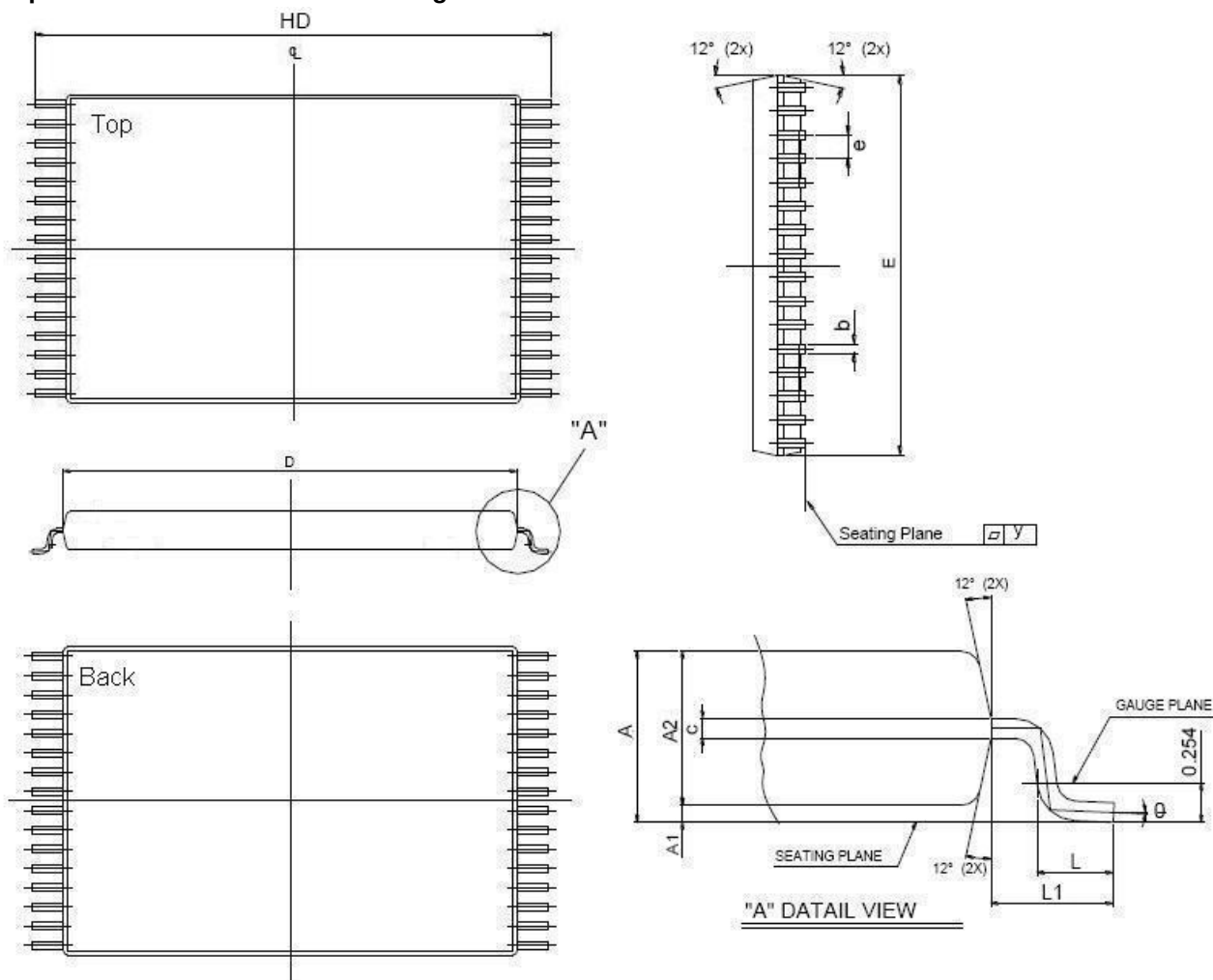
#### 32-pin 400 mil TSOP II Package Outline Dimension



NOTE : DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSIONS.  
D AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

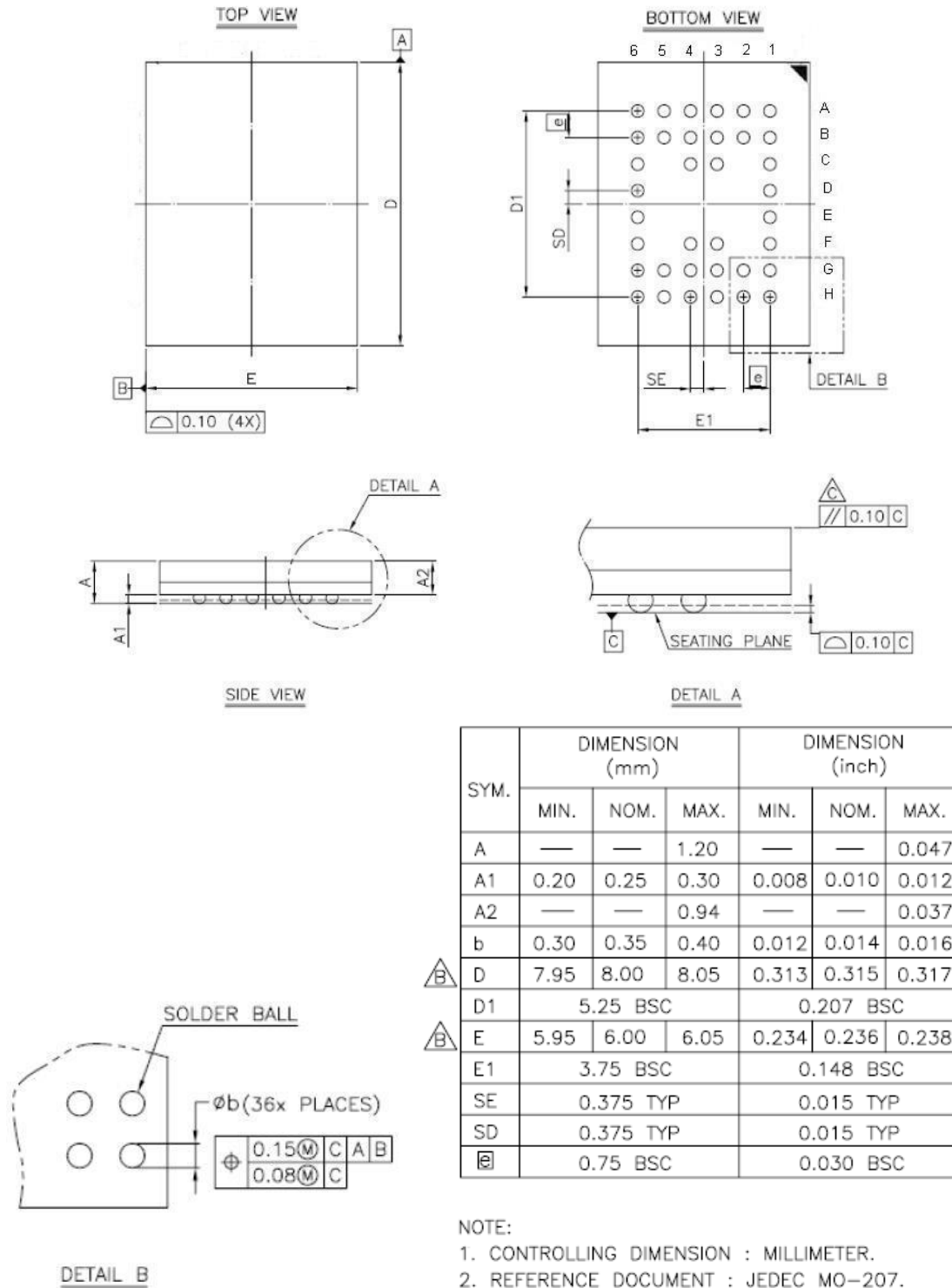


#### 32-pin 8mm x 13.4mm sTSP Package Outline Dimension



| SYM. | UNIT | INCH(BASE)   | MM(REF)      |
|------|------|--------------|--------------|
| A    |      | 0.049 (MAX)  | 1.25 (MAX)   |
| A1   |      | 0.004 ±0.002 | 0.10 ±0.05   |
| A2   |      | 0.039 ±0.002 | 1.00 ±0.05   |
| b    |      | 0.009 ±0.002 | 0.22 ±0.05   |
| c    |      | 0.006 ±0.002 | 0.155 ±0.055 |
| D    |      | 0.465 ±0.008 | 11.80 ±0.20  |
| E    |      | 0.315 ±0.008 | 8.00 ±0.20   |
| e    |      | 0.020 (TYP)  | 0.50 (TYP)   |
| HD   |      | 0.528±0.008  | 13.40 ±0.20. |
| L    |      | 0.02 ±0.008  | 0.50 ±0.20   |
| L1   |      | 0.031 ±0.005 | 0.8 ±0.125   |
| y    |      | 0.003 (MAX)  | 0.076 (MAX)  |
| Θ    |      | 0°~5°        | 0°~5°        |

#### 36-ball 6mm × 8mm TFBGA Package Outline Dimension



**ORDERING INFORMATION**

| Package Type        | Access Time (Speed)(ns) | Power Type              | Temperature Range(°C) | Packing Type | Lyontek Item No.   |
|---------------------|-------------------------|-------------------------|-----------------------|--------------|--------------------|
| 32-pin (450mil) SOP | 55                      | Special Ultra Low Power | 0°C ~70°C             | Tube         | LY62W5128SL-55SL   |
|                     |                         |                         |                       | Tape Reel    | LY62W5128SL-55SLT  |
|                     |                         |                         | -40°C ~85°C           | Tube         | LY62W5128SL-55SLI  |
|                     |                         |                         |                       | Tape Reel    | LY62W5128SL-55SLIT |
|                     |                         | Ultra Low Power         | 0°C ~70°C             | Tube         | LY62W5128SL-55LL   |
|                     |                         |                         |                       | Tape Reel    | LY62W5128SL-55LLT  |
|                     | 70                      | Special Ultra Low Power | 0°C ~70°C             | Tube         | LY62W5128SL-70SL   |
|                     |                         |                         |                       | Tape Reel    | LY62W5128SL-70SLT  |
|                     |                         |                         | -40°C ~85°C           | Tube         | LY62W5128SL-70SLI  |
|                     |                         |                         |                       | Tape Reel    | LY62W5128SL-70SLIT |
|                     |                         | Ultra Low Power         | 0°C ~70°C             | Tube         | LY62W5128SL-70LL   |
|                     |                         |                         |                       | Tape Reel    | LY62W5128SL-70LLT  |
|                     |                         |                         | -40°C ~85°C           | Tube         | LY62W5128SL-70LLI  |
|                     |                         |                         |                       | Tape Reel    | LY62W5128SL-70LLIT |



#### ORDERING INFORMATION

| Package Type         | Access Time (Speed)(ns) | Power Type              | Temperature Range(°C) | Packing Type | Lyontek Item No.  |
|----------------------|-------------------------|-------------------------|-----------------------|--------------|-------------------|
| 32-pin (600mil) PDIP | 55                      | Special Ultra Low Power | 0°C ~70°C             | Tube         | LY62W5128PL-55SL  |
|                      |                         |                         | -40°C ~85°C           | Tube         | LY62W5128PL-55SLI |
|                      |                         | Ultra Low Power         | 0°C ~70°C             | Tube         | LY62W5128PL-55LL  |
|                      |                         |                         | -40°C ~85°C           | Tube         | LY62W5128PL-55LLI |
|                      | 70                      | Special Ultra Low Power | 0°C ~70°C             | Tube         | LY62W5128PL-70SL  |
|                      |                         |                         | -40°C ~85°C           | Tube         | LY62W5128PL-70SLI |
|                      |                         | Ultra Low Power         | 0°C ~70°C             | Tube         | LY62W5128PL-70LL  |
|                      |                         |                         | -40°C ~85°C           | Tube         | LY62W5128PL-70LLI |



#### ORDERING INFORMATION

| Package Type                     | Access Time (Speed)(ns) | Power Type              | Temperature Range(°C) | Packing Type | Lyontek Item No.   |
|----------------------------------|-------------------------|-------------------------|-----------------------|--------------|--------------------|
| 32-pin<br>(8mm x 20mm)<br>TSOP I | 55                      | Special Ultra Low Power | 0°C ~70°C             | Tray         | LY62W5128LL-55SL   |
|                                  |                         |                         |                       | Tape Reel    | LY62W5128LL-55SLT  |
|                                  |                         |                         | -40°C ~85°C           | Tray         | LY62W5128LL-55SLI  |
|                                  |                         |                         |                       | Tape Reel    | LY62W5128LL-55SLIT |
|                                  |                         | Ultra Low Power         | 0°C ~70°C             | Tray         | LY62W5128LL-55LL   |
|                                  |                         |                         |                       | Tape Reel    | LY62W5128LL-55LLT  |
|                                  | 70                      |                         | -40°C ~85°C           | Tray         | LY62W5128LL-55LLI  |
|                                  |                         |                         |                       | Tape Reel    | LY62W5128LL-55LLIT |
|                                  |                         | Special Ultra Low Power | 0°C ~70°C             | Tray         | LY62W5128LL-70SL   |
|                                  |                         |                         |                       | Tape Reel    | LY62W5128LL-70SLT  |
|                                  |                         |                         | -40°C ~85°C           | Tray         | LY62W5128LL-70SLI  |
|                                  |                         |                         |                       | Tape Reel    | LY62W5128LL-70SLIT |
|                                  |                         | Ultra Low Power         | 0°C ~70°C             | Tray         | LY62W5128LL-70LL   |
|                                  |                         |                         |                       | Tape Reel    | LY62W5128LL-70LLT  |
|                                  |                         |                         | -40°C ~85°C           | Tray         | LY62W5128LL-70LLI  |
|                                  |                         |                         |                       | Tape Reel    | LY62W5128LL-70LLIT |



#### ORDERING INFORMATION

| Package Type            | Access Time (Speed)(ns) | Power Type              | Temperature Range(°C) | Packing Type | Lyontek Item No.   |
|-------------------------|-------------------------|-------------------------|-----------------------|--------------|--------------------|
| 32-pin (400mil) TSOP II | 55                      | Special Ultra Low Power | 0°C ~70°C             | Tray         | LY62W5128WL-55SL   |
|                         |                         |                         |                       | Tape Reel    | LY62W5128WL-55SLT  |
|                         |                         |                         | -40°C ~85°C           | Tray         | LY62W5128WL-55SLI  |
|                         |                         |                         |                       | Tape Reel    | LY62W5128WL-55SLIT |
|                         |                         | Ultra Low Power         | 0°C ~70°C             | Tray         | LY62W5128WL-55LL   |
|                         |                         |                         |                       | Tape Reel    | LY62W5128WL-55LLT  |
|                         | 70                      |                         | -40°C ~85°C           | Tray         | LY62W5128WL-55LLI  |
|                         |                         |                         |                       | Tape Reel    | LY62W5128WL-55LLIT |
|                         |                         | Special Ultra Low Power | 0°C ~70°C             | Tray         | LY62W5128WL-70SL   |
|                         |                         |                         |                       | Tape Reel    | LY62W5128WL-70SLT  |
|                         |                         |                         | -40°C ~85°C           | Tray         | LY62W5128WL-70SLI  |
|                         |                         |                         |                       | Tape Reel    | LY62W5128WL-70SLIT |
|                         |                         | Ultra Low Power         | 0°C ~70°C             | Tray         | LY62W5128WL-70LL   |
|                         |                         |                         |                       | Tape Reel    | LY62W5128WL-70LLT  |
|                         |                         |                         | -40°C ~85°C           | Tray         | LY62W5128WL-70LLI  |
|                         |                         |                         |                       | Tape Reel    | LY62W5128WL-70LLIT |

**ORDERING INFORMATION**

| Package Type                      | Access Time (Speed)(ns) | Power Type              | Temperature Range(°C) | Packing Type | Lyontek Item No.   |
|-----------------------------------|-------------------------|-------------------------|-----------------------|--------------|--------------------|
| 32-pin<br>(8mm x 13.4mm)<br>sTSOP | 55                      | Special Ultra Low Power | 0°C ~70°C             | Tray         | LY62W5128RL-55SL   |
|                                   |                         |                         |                       | Tape Reel    | LY62W5128RL-55SLT  |
|                                   |                         |                         | -40°C ~85°C           | Tray         | LY62W5128RL-55SLI  |
|                                   |                         |                         |                       | Tape Reel    | LY62W5128RL-55SLIT |
|                                   |                         | Ultra Low Power         | 0°C ~70°C             | Tray         | LY62W5128RL-55LL   |
|                                   |                         |                         |                       | Tape Reel    | LY62W5128RL-55LLT  |
|                                   | 70                      |                         | -40°C ~85°C           | Tray         | LY62W5128RL-55LLI  |
|                                   |                         |                         |                       | Tape Reel    | LY62W5128RL-55LLIT |
|                                   |                         | Special Ultra Low Power | 0°C ~70°C             | Tray         | LY62W5128RL-70SL   |
|                                   |                         |                         |                       | Tape Reel    | LY62W5128RL-70SLT  |
|                                   |                         |                         | -40°C ~85°C           | Tray         | LY62W5128RL-70SLI  |
|                                   |                         |                         |                       | Tape Reel    | LY62W5128RL-70SLIT |
|                                   |                         | Ultra Low Power         | 0°C ~70°C             | Tray         | LY62W5128RL-70LL   |
|                                   |                         |                         |                       | Tape Reel    | LY62W5128RL-70LLT  |
|                                   |                         |                         | -40°C ~85°C           | Tray         | LY62W5128RL-70LLI  |
|                                   |                         |                         |                       | Tape Reel    | LY62W5128RL-70LLIT |



#### ORDERING INFORMATION

| Package Type                    | Access Time (Speed)(ns) | Power Type              | Temperature Range(°C) | Packing Type | Lyontek Item No.   |
|---------------------------------|-------------------------|-------------------------|-----------------------|--------------|--------------------|
| 36-ball<br>(6mm x 8mm)<br>TFBGA | 55                      | Special Ultra Low Power | 0°C ~70°C             | Tray         | LY62W5128GL-55SL   |
|                                 |                         |                         |                       | Tape Reel    | LY62W5128GL-55SLT  |
|                                 |                         |                         | -40°C ~85°C           | Tray         | LY62W5128GL-55SLI  |
|                                 |                         |                         |                       | Tape Reel    | LY62W5128GL-55SLIT |
|                                 |                         | Ultra Low Power         | 0°C ~70°C             | Tray         | LY62W5128GL-55LL   |
|                                 |                         |                         |                       | Tape Reel    | LY62W5128GL-55LLT  |
|                                 | 70                      |                         | -40°C ~85°C           | Tray         | LY62W5128GL-55LLI  |
|                                 |                         |                         |                       | Tape Reel    | LY62W5128GL-55LLIT |
|                                 |                         | Special Ultra Low Power | 0°C ~70°C             | Tray         | LY62W5128GL-70SL   |
|                                 |                         |                         |                       | Tape Reel    | LY62W5128GL-70SLT  |
|                                 |                         |                         | -40°C ~85°C           | Tray         | LY62W5128GL-70SLI  |
|                                 |                         |                         |                       | Tape Reel    | LY62W5128GL-70SLIT |
|                                 |                         | Ultra Low Power         | 0°C ~70°C             | Tray         | LY62W5128GL-70LL   |
|                                 |                         |                         |                       | Tape Reel    | LY62W5128GL-70LLT  |
|                                 |                         |                         | -40°C ~85°C           | Tray         | LY62W5128GL-70LLI  |
|                                 |                         |                         |                       | Tape Reel    | LY62W5128GL-70LLIT |



**Lyontek Inc.**

**LY62W5128**

Rev. 1.14

**512K X 8 BIT LOW POWER CMOS SRAM**

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