HIGH VOLTAGE DC/DC BOOST CONVERTER WITH 0.5-A/1.3-A INTEGRATED SWITCH

FEATURES

- **2.5-V to 6-V Input Voltage Range**
- **Up to 27-V Output Voltage**
- **0.5-A Integrated Switch (TPS61080)**
  1.3-A Integrated Switch (TPS61081)
- **12 V/400 mA and 24 V/170 mA From 5-V Input (TYP)**
- **Integrated Power Diode**
- **1.2-MHz/600-kHz Selectable Fixed Switching Frequency**
- **Input to Output Isolation**
- **Short-Circuit Protection**
- **Programmable Soft Start**
- **Overvoltage Protection**
- **Up to 87% Efficiency**
- **10-Pin 3 mm×3 mm QFN Package**

APPLICATIONS

- **3.3V to 12V, 5V to 12V and 24V Boost Converter**
- **White LED Backlight for Media Form Factor Display**
- **OLED Power Supply**
- **xDSL Applications**
- **TFT-LCD Bias Supply**
- **White LED Flash Light**

DESCRIPTION

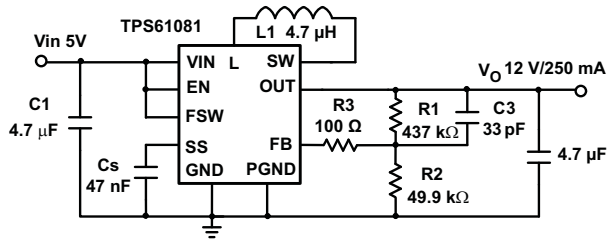
The TPS61080/1 is a 1.2MHz/600kHz fixed frequency boost regulator designed for high integration, which integrates a power switch, an input/output isolation switch and a power diode. When a short circuit condition is detected, the isolation switch opens up to disconnect the output from the input. As a result, the IC protects itself and the input source from any pin, except VIN, from being shorted to ground. The isolation switch also disconnects the output from input during shutdown to prevent any leakage current. Other provisions for protection include 0.5A/1.3A peak-to-peak over current protection, programmable soft start (SS), over voltage protection (OVP), thermal shutdown and under voltage lockout (UVLO).

The IC operates from input supplies including single Li-ion battery, triple NiMH, and regulated 5V, such as USB output. The output can be boosted up to 27V. TPS61080/1 can provide the supply voltages of OLED, TFT-LCD bias, 12V and 24V power rails. The output of TPS61080/1 can also be configured as a current source to power up to 7 WLED in flash light applications.

ORDERING INFORMATION

T_A	OVERCURRENT LIMIT	PACKAGE	PACKAGE MARKING
–40°C to 85°C	0.5A(min)	TPS61080DRCR	BCN
	1.3A(min)	TPS61081DRCR	BCO
	0.5A(min)	TPS61080DRCT	BCN
	1.3A(min)	TPS61081DRCT	BCO

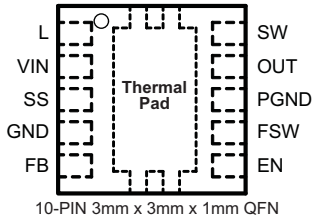
TYPICAL APPLICATION



L1: TDK VLCF5020T-4R7N1R7-1
C1: Murata GRM188R60J105K
C2: Murata GRM219R61C475K
C3: Feed forward capacitor for stability
R3: Noise decoupling resistor
Cs: Soft start programming capacitor

Figure 1. 5V to 12V, 250mA Step-Up DC/DC Converter

TOP VIEW



10-PIN 3mm x 3mm x 1mm QFN

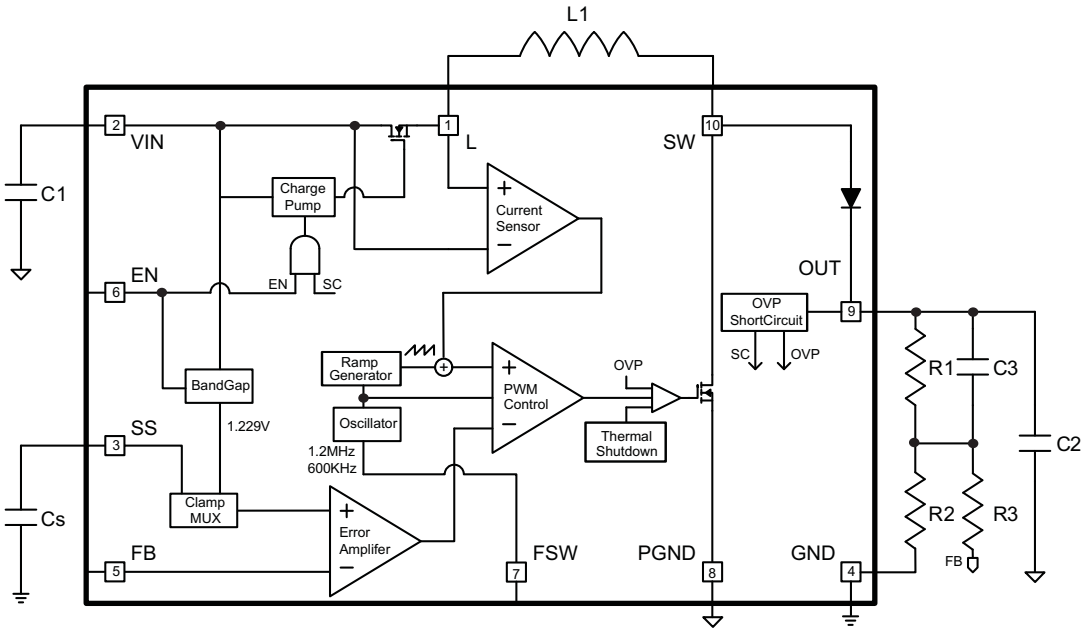
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
L	1	I	The inductor is connected between this pin and the SW pin. This pin connects to the source of the isolation FET as well. Minimize trace area at this pin to reduce EMI.
VIN	2	I	Input pin to the IC. It is the input to the boost regulator, and also powers the IC circuit. It is connected to the drain of the isolation FET as well.
EN	6	I	Enable pin. When the voltage of this pin falls below enable threshold for more than 74ms, the IC turns off and consumes less than 2 μA current.
GND	4		Signal ground of the IC
PGND	8		Power ground of the IC. It is connected to the source of the PWM switch. This pin should be made very close to the output capacitor in layout.
FB	5	I	Voltage feedback pin for the output regulation. It is regulated to an internal reference voltage. An external voltage divider from the output to GND with the center tap connected to this pin programs the regulated voltage. This pin can also be connected to a low side current sense resistor to program current regulation.
OUT	9	O	Output of the boost regulator. When the output voltage exceeds the 27V overvoltage protection (OVP) threshold, the PWM switch turns off until Vout drops 0.7V below the overvoltage threshold.
SW	10	I	Switching node of the IC. Connect the inductor between this pin and the L pin.
SS	3	I	Soft start programming pin. A capacitor between the SS pin and GND pin programs soft start timing.
FSW	7	I	Switching frequency selection pin. Logic high on the pin selects 1.2MHz, while logic low reduces the frequency to 600KHz for better light load efficiency.
Thermal Pad	–		The thermal pad should be soldered to the analog ground. If possible, use thermal via to connect to ground plane for ideal power dissipation.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	VALUE	UNIT
Supply Voltages on pin VIN(2)	–0.3 to 7	V
Voltages on pins EN, FB, SS, L and FSW(2)	–0.3 to 7	V
Voltage on pin OUT(2)	30V	V
Voltage on pin SW(2)	30V	V
Continuous Power Dissipation	See Dissipation Rating Table	
Operating Junction Temperature Range	–40 to 150	°C
Storage Temperature Range	–65 to 150	°C
Lead Temperature (soldering, 10 sec)	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	θ_{JC}	θ_{JA}	$T_A \leq 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
QFN(1)	3.21°C/W	270°C/W	370 mW	204 mW	148 mW
QFN(2)	3.21°C/W	48.7°C/W	2.05 W	1.13 W	821 mW

(1) Soldered PowerPAD™ on a standard 2-layer PCB without vias for thermal pad
(2) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input voltage range	2.5		6.0	V
VOUT	Output voltage range	VIN		27	V
L	Inductor(1)	4.7		10	µH
C_{in}	Input capacitor(1)	1			µF
C_{OUT}	Output capacitor(1)	4.7			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Refer to application section for further information

ELECTRICAL CHARACTERISTICS

VIN = 3.6 V, EN = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
VIN	Input voltage range		2.5		6.0	V
I_Q	Operating quiescent current into VIN	Device switching no load			6	mA
I_{SD}	Shutdown current	EN = GND			1	µA
V_{UVLO}	Under-voltage lockout threshold	VIN falling		1.65	1.8	V
V_{hys}	Under-voltage lockout hysterisis			50		mV
ENABLE						
V_{EN}	Enable level voltage	VIN = 2.5 V to 6 V	1.2			V
	Disable level voltage	VIN = 2.5 V to 6 V			0.4	
R_{en}	Enable pull down resistor		400	800	1600	kΩ
T_{off}	EN pulse width to disable	EN high to low	74			ms

ELECTRICAL CHARACTERISTICS (continued)

VIN = 3.6 V, EN = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
I_{ss}	Soft start bias current	T_A = 25°C	4.75	5	5.25	µA
			4.6	5	5.4	
V_{clp}	SS pin to FB pin accuracy	Vss = 500 mV	487	500	513	mV
FEEDBACK FB						
I_{FB}	Feedback input bias current	V_{FB} = 1.229 V	–100		100	nA
V_{FB}	Feedback regulation voltage		1.204	1.229	1.254	V
POWER SWITCH AND DIODE						
$R_{DS(ON)}$	Isolation MOSFET on-resistance			0.06	0.1	Ω
	N-channel MOSFET on-resistance	V_{IN} = VGS = 3.6 V		0.17	0.22	Ω
		V_{IN} = VGS = 2.5 V		0.2	0.32	
I_{LN_NFET}	N-channel leakage current	V_{DS} = 28 V		1	2	µA
V_F	Power diode forward voltage	Id = 1 A		0.85	1	V
I_{LN_ISO}	Isolation FET leakage current	L pin to ground			1	µA
OC AND SC						
I_{LIM}	N-Channel MOSFET current limit(1)	TPS61080, FSW = High or FSW = Low	0.5	0.7	1.0	A
		TPS61081, FSW = High or FSW = Low	1.3	1.6	2.0	
I_{SC}	Short circuit current limit	TPS61080	1.0		2.2	A
		TPS61081	2.0		3.5	
T_{scd}	Short circuit delay time			13		µs
T_{scr}	Short circuit release time			57		ms
V_{SC}	OUT short detection threshold (2)	VIN – VOUT		1.4		V
OSCILLATOR						
f_S	Oscillator frequency	FSW pin high	1.0	1.2	1.5	MHz
		FSW pin low	0.5	0.6	0.7	
D_{max}	Maximum duty cycle	FB = 1.0 V	90%	94%		
D_{min}	Minimum duty cycle			5%		
R_{fsw}	FSW pin pull down resistance		400	800	1600	kΩ
V_{FSW}	FSW high logic		1.6			V
	FSW low logic				0.8	
OVP						
Vovp	Output overvoltage protection	Vout rising	27	28	29	V
	Output overvoltage protection hysteresis	Vout falling		0.7		V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

(1) VIN = 3.6 V, Vout = 15 V, Duty cycle = 76%. See Figure 6 to Figure 9 for other operation conditions.
(2) OUT short circuit condition is detected if OUT stays lower than VIN – Vsc for 2 ms after IC enables.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Efficiency	Vs Iout, VIN=3.6V OUT=12V, 15V, 20V, 25V, FSW=HIGH, L=4.7 µH	2
	Vs Iout, VIN=3.6V OUT=12V, 15V, 20V, 25V, FSW=LOW, L=10 µH	3
	Vs Iout, VIN=3V, 3.6V, 5V, OUT=12V, FSW=HIGH, L=4.7 µH	4
	Vs Iout, VIN=3V, 3.6V, 5V, OUT=12V, FSW=LOW, L=10 µH	5
Overcurrent Limit	VIN=3.0V, 3.6V, 5V, FSW=High/Low	6, 7, 8, 9
Line Regulation	TPS61081, VIN=2.5V to 6V, OUT=12V, Iout=100mA	10
Load Regulation	TPS61081, VIN=3.6V, OUT=12V	11
Soft Start	TPS61081, VIN=3.6V, OUT=12V, Iout=150mA, FSW=HIGH, Css=47nF	12
OUT SC Protection	TPS61081, VIN=3.6V, OUT=12V, Iout=150mA, FSW=HIGH	13
Transient Response	TPS61080, VIN=3.6V, OUT=12V, Iout=10mA to 60mA, Cff=33pF, L=10µH	14
	TPS61081, VIN=3.6V, OUT=12V, Iout=25mA to 150mA, Cff=33pF, L=4.7µH	15
Input and Output Ripple	TPS61081, VIN=3.6V, OUT=12V, Iout=150mA	16
OVP	TPS61080/1	17
SS to FB accuracy	TPS61080/1	18
Minimum Load Requirement	TPS61080/1, VIN =3.6V and 5V, FSW = HIGH, L=4.7µH	19

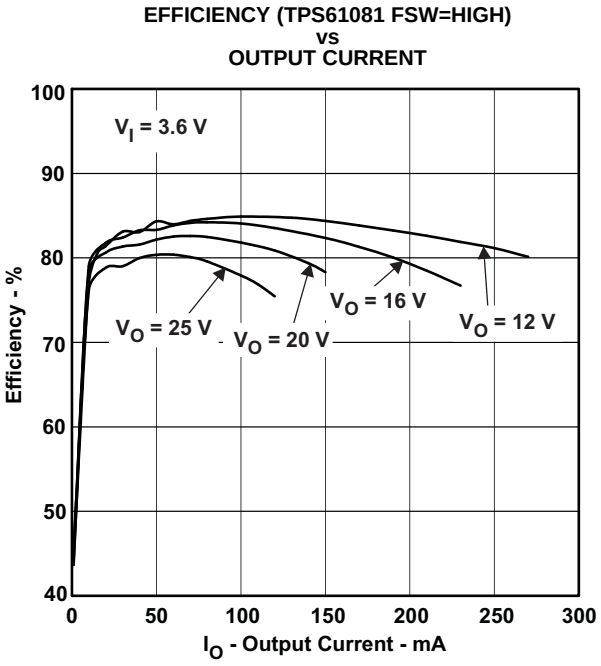


Figure 2.

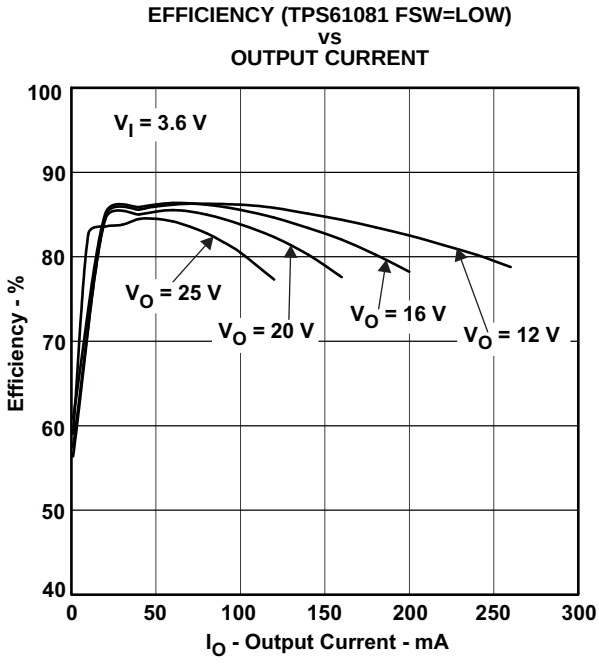


Figure 3.

EFFICIENCY (TPS61081 FSW=HIGH)
vs
OUTPUT CURRENT

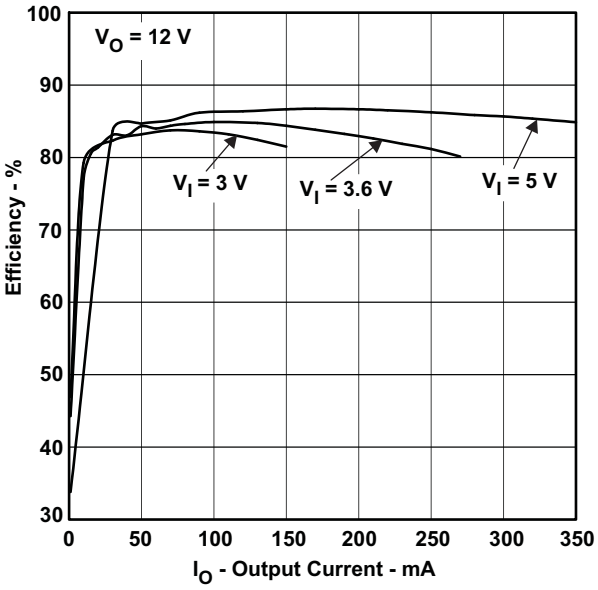


Figure 4.

EFFICIENCY (TPS61081 FSW=LOW)
vs
OUTPUT CURRENT

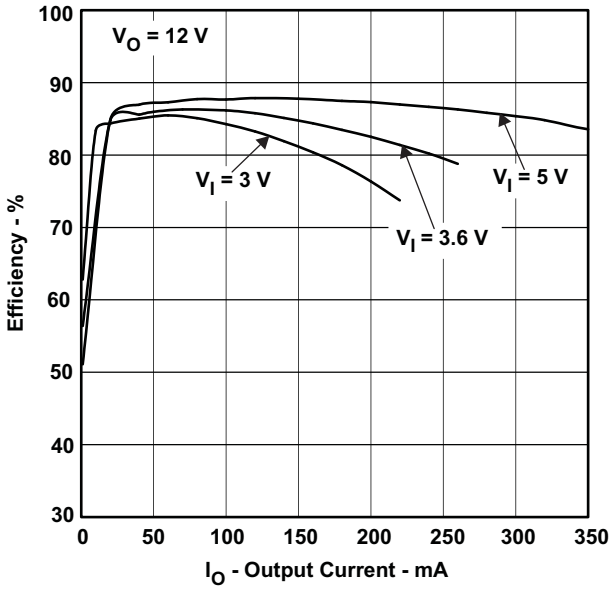


Figure 5.

OVER CURRENT LIMIT (TPS61080 FSW=LOW)
vs
DUTY CYCLE

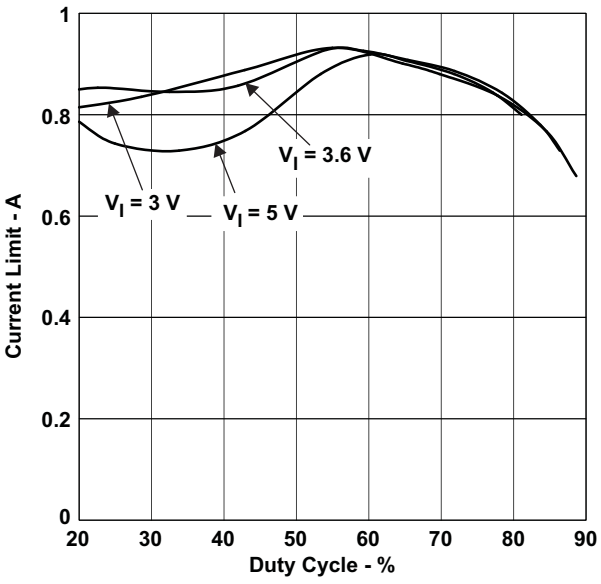


Figure 6.

OVER CURRENT LIMIT (TPS61080 FSW=HIGH)
vs
DUTY CYCLE

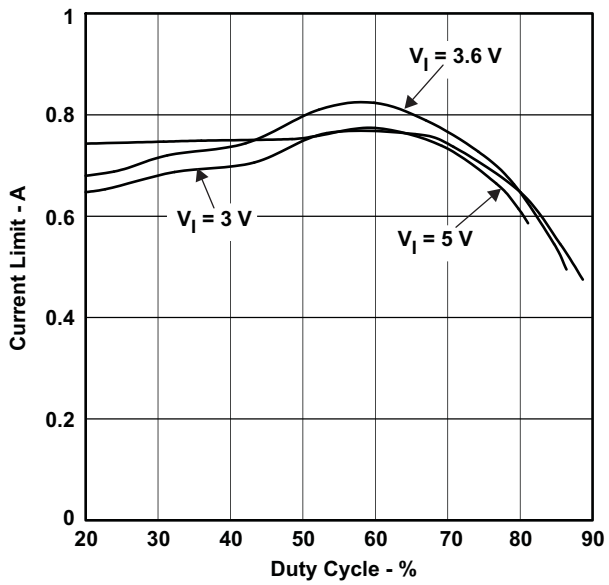


Figure 7.

OVER CURRENT LIMIT (TPS61081 FSW=LOW)
vs
DUTY CYCLE

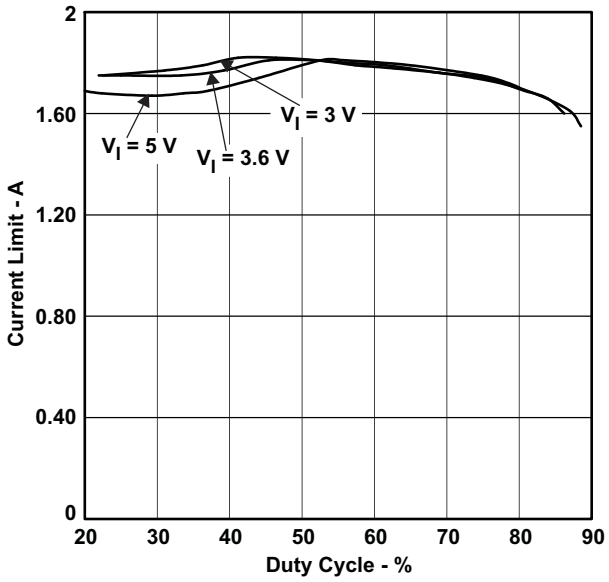


Figure 8.

OVER CURRENT LIMIT (TPS61081 FSW=HIGH)
vs
DUTY CYCLE

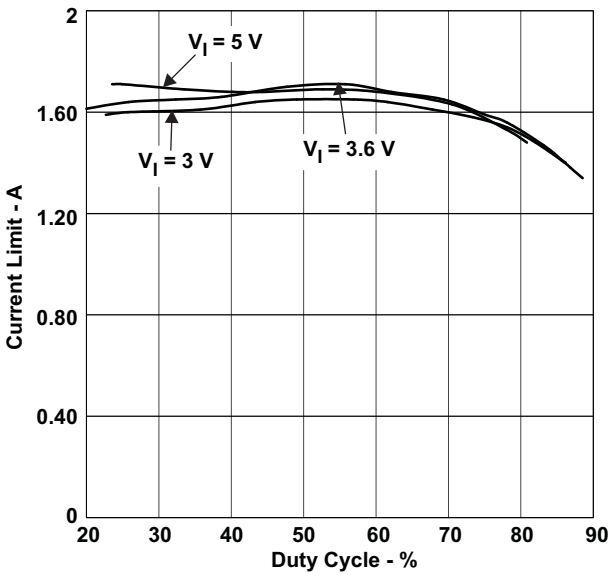


Figure 9.

LINE REGULATION TPS61081

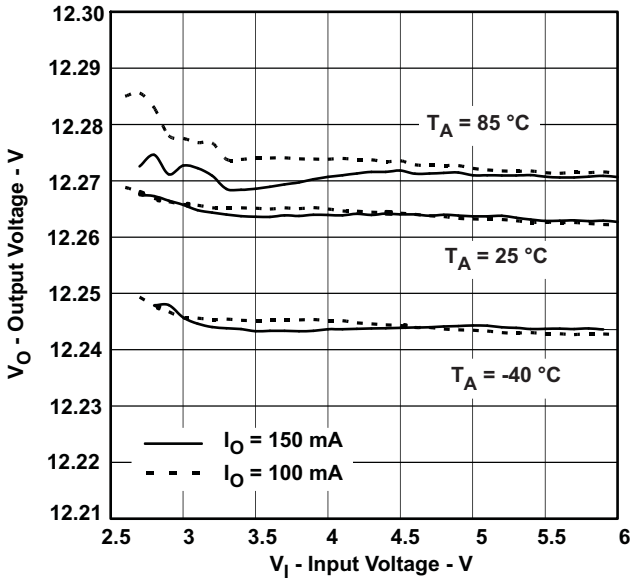


Figure 10.

LOAD REGULATION TPS61081

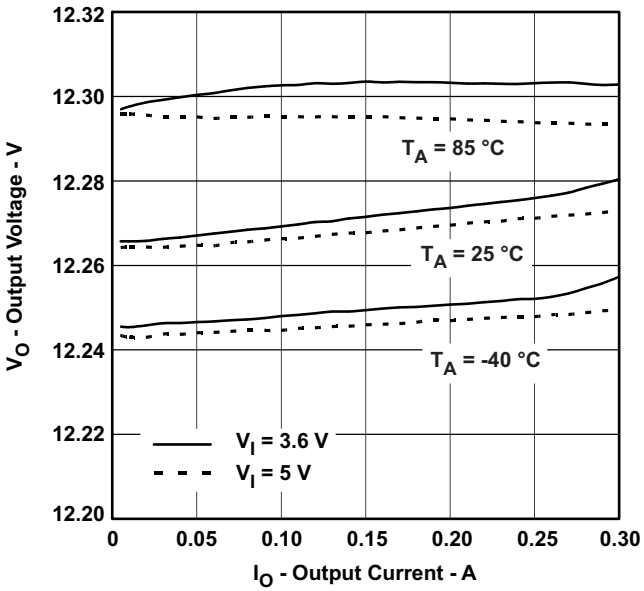


Figure 11.

Soft Start TPS61081

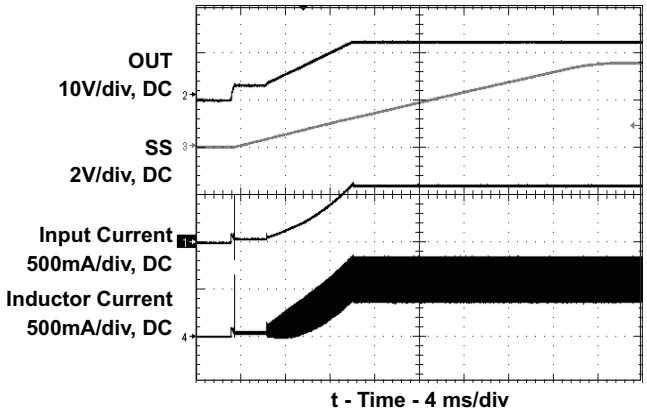


Figure 12.

Vout SC PROTECTION TPS61081

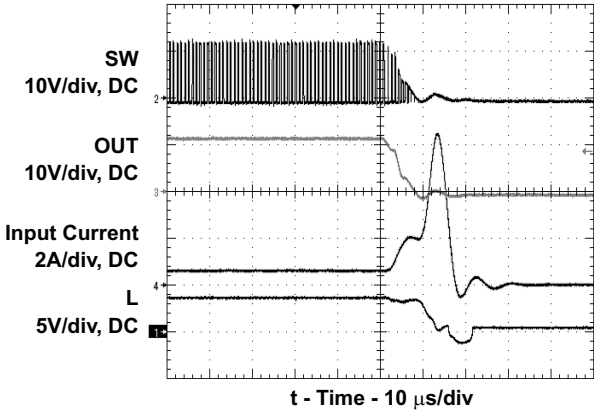


Figure 13.

TRANSIENT RESPONSE TPS61080

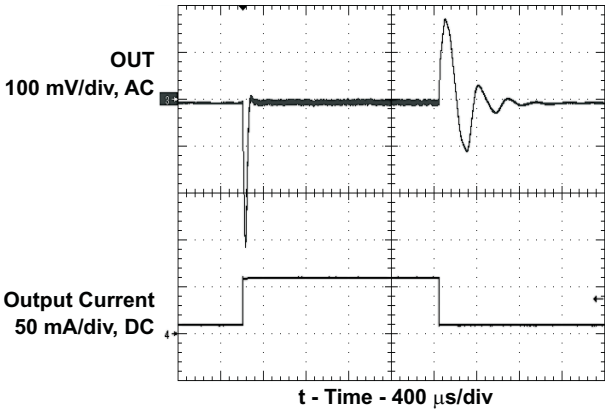


Figure 14.

TRANSIENT RESPONSE TPS61081

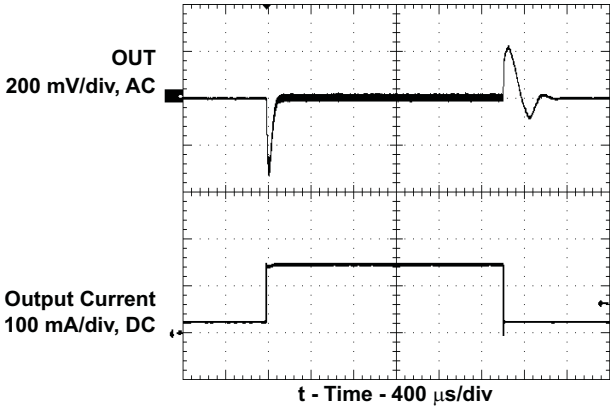


Figure 15.

INPUT AND OUTPUT RIPPLE TPS61081

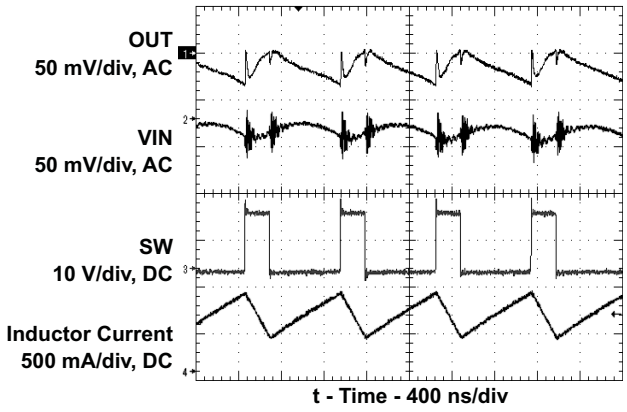


Figure 16.

OVP TPS61081

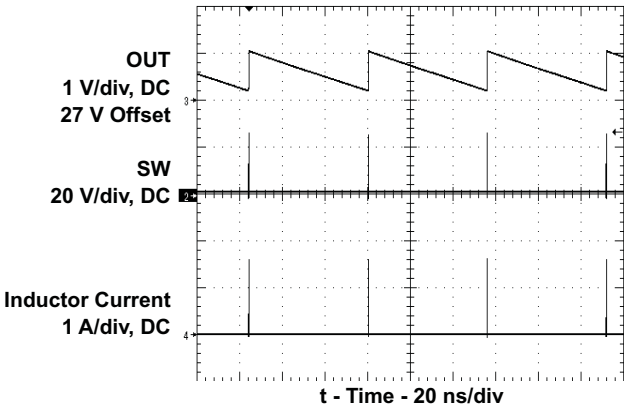


Figure 17.

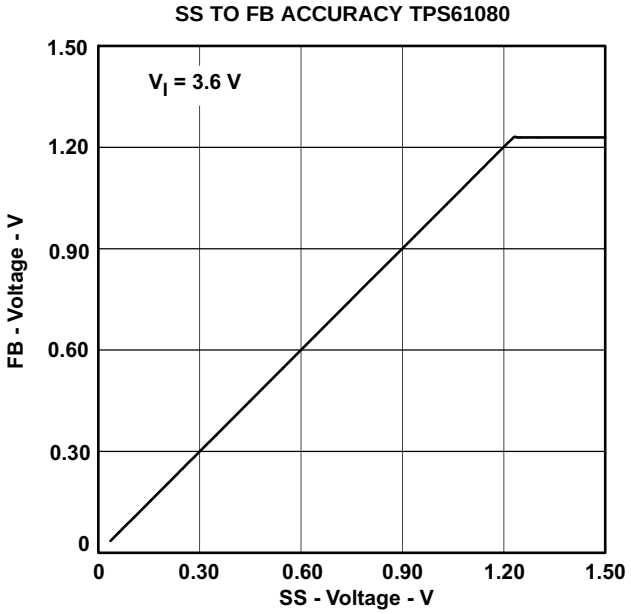


Figure 18.

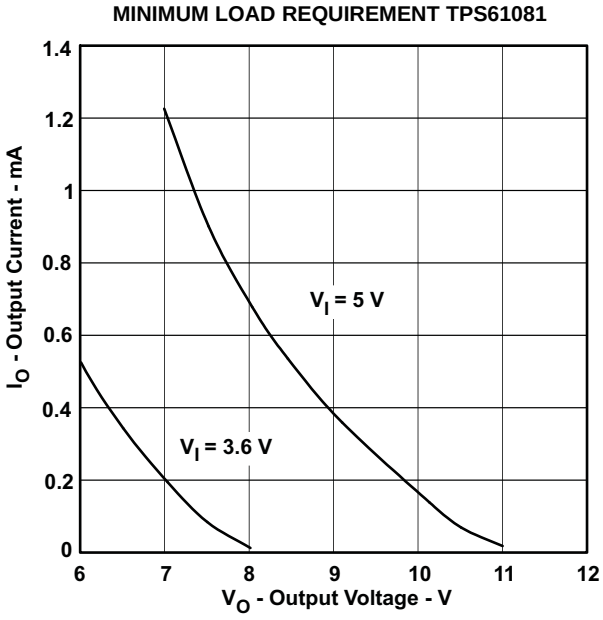


Figure 19.

DETAILED DESCRIPTION

OPERATION

TPS61080/1 is a highly integrated boost regulator for up to 27V output. In addition to the on-chip 0.5A/1.2A PWM switch and power diode, this IC also builds in an input side isolation switch as shown in the block diagram. One common issue with conventional boost regulator is the conduction path from input to output even when PWM switch is turned off. It creates three problems, inrush current during start up, output leakage voltage under shutdown, and unlimited short circuit current. To address these issues, TPS61080/1 turns off the isolation switch under shutdown mode and short circuit condition to eliminate any possible current path. Although the isolation switch has low $R_{DS(on)}$ for small power losses, shorting the VIN and L pin can bypass the switch and further enhance the efficiency.

TPS61080/1 adopts current mode control with constant PWM (pulse width modulation) frequency. The switching frequency can be configured to either 600KHz or 1.2MHz through the FSW pin. 600KHz improves light load efficiency, while 1.2MHz allows using smaller external component. The PWM operation turns on the PWM switch at the beginning of each switching cycle. The input voltage is applied across the inductor and stores the energy as inductor current ramps up. The load current is provided by the output capacitor. When the inductor current across the threshold set by error amplifier output, the PWM switch is turned off, and the power diode is forward biased. The inductor transfers its stored energy to replenish the output capacitor. This operation repeats in the next switching cycle.

The error amplifier compares the FB pin voltage with an internal reference, and its output determines the duty cycle of the PWM switching. This close loop system requires loop compensation for stable operation. TPS61080/1 has internal compensation circuitry which accommodates a wide range of input and output voltages. The TPS61080/1 integrates slope compensation to the current ramp to avoid the sub-harmonic oscillation that is intrinsic to current mode control schemes.

START UP

TPS61080/1 turns on the isolation FET when the EN pin is pulled high, provided that the input voltage is higher than the undervoltage lockout threshold. The Vgs of the isolation FET is clamped to maintain high on-resistance and limit the current charging the output capacitor. This feature limits the in-rush current that could pull down the input supply and cause system instability. Once the output capacitor is charged to VIN, the IC removes the Vgs clamp to fully turn on the isolation FET and at the same time actives soft start by charging the capacitor on the SS pin. If OUT stays lower than VIN-Vsc following a 2ms delay after enable is taken high, the IC recognizes a short circuit condition. In this case, the isolation FET turns off, and IC remains off until the EN pin toggles or VIN cycles through power on reset (POR).

During the soft start phase, the SS pin capacitor is charged by internal bias current of the SS pin. The SS pin capacitor programs the ramp up slope. The SS pin voltage clamps the reference voltage of the FB pin, therefore the output capacitor rise time follows the SS pin voltage. Without the soft start, the inductor current could reach the over current limit threshold, and there is potential for output overshoot. see the APPLICATION INFORMATION section on selecting soft start capacitor values. Pulling the SS pin to ground disables the PWM switching. However, unlike being disabled by pulling EN low, the IC continues to draw quiescent current and the isolation FET remains on.

OVERCURRENT AND SHORT CIRCUIT PROTECTION

TPS61080/1 has a pulse by pulse over current limit feature which turns off the power switch once the inductor current reaches the overcurrent limit. The PWM circuitry resets itself at the beginning of the next switch cycle. The overcurrent threshold determines the available output current. However, the maximum output is also a function of the input voltage, output voltage, switching frequency and inductor value. Larger inductor values and 1.2MHz switching frequency increase the current output capability because of the reduced current ripple. See the APPLICATION INFORMATION section for the maximum output current calculation.

In typical boost converter topologies, if the output is grounded, turning off the power switch does not limit the current because a current path exists from the input to output through the inductor and power diode. To eliminate this path, TPS61080/1 turns off the isolation FET between the input and the inductor. This circuit is triggered when the inductor current remains above short circuit current limit for more than 13µs, or the OUT pin voltage falls below VIN-1.4V for more than 2ms. An internal catch-diode between the L pin and ground turns on to provide a current discharge path for the inductor. If the short is caused by the output being low, then the IC

DETAILED DESCRIPTION (continued)

shuts down and waits for EN to be toggled or a POR. If the short protection is triggered by short circuit current limit, the IC attempts to start up one time. After 57ms, the IC restarts in a fashion described in the above section. If the short is cleared, the boost regulator properly starts up and reaches output regulation. However, after reaching regulation, if another event of short circuit current limit occurs, the IC goes into shutdown mode again, and the fault can only be cleared by toggling the EN pin or POR. Under a permanent short circuit, the IC shuts down after a start up failure and waits for POR or the EN pin toggling.

The same circuit also protects the ICs and external components when the SW pin is shorted to ground. These features provide much more comprehensive and reliable protection than the conventional boost regulator. Table 1 lists the IC protection against the short of each IC pin.

Table 1. TPS61080/1 Short Circuit Protection Mode

SHORTED TO GND	FAULT DETECTION	IC OPERATION	HOW TO CLEAR THE FAULT
L, SW	INDUCTOR > I_{SC} for 13 µs	Turn off isolation FET	IC restarts after 57ms; If it happens again, the fault can only be cleared by toggling EN or POR.
OUT (during start up)	OUT <Vin– 1.4V for 2 ms	IC shuts down	Cleared by toggling EN or POR
OUT (after start up)	OUT <Vin– 1.4V without delay	IC shuts down	Cleared by toggling EN or POR
EN	N/A	IC disabled	N/A
FSW	N/A	600 kHz switching frequency	N/A
SS	N/A	Disable PWM switching and no output; but still dissipate quiescent current.	N/A
FB	N/A	Over voltage protection of the OUT pin	OUT voltage fails by OVP hysteresis
GND, PGND, VIN	N/A	N/A	N/A

OVERVOLTAGE PROTECTION

When TPS61080/1 is configured as regulated current output as shown in the TYPICAL APPLICATIONS, the output voltage can run away if the current load is disconnected. The over voltage condition can also occur if the FB pin is shorted to the ground. To prevent the SW node and the output capacitor from exceeding the maximum voltage rating, an over voltage protection circuit turns off the boost regulator as soon as the output voltage exceeds the OVP threshold. When the output voltage falls 0.7V below the OVP threshold, the regulator resumes the PWM switching unless the output voltage exceeds the OVP threshold.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout prevents mis-operation of the device for input voltages below 1.65 V (typical). When the input voltage is below the undervoltage threshold, the device remains off and both PWM and isolation switch are turned off, providing isolation between input and output. The undervoltage lockout threshold is set below minimum operating voltage of 2.5V to avoid any transient VIN dip to trigger UVLO and causes converter reset. For the VIN voltage between UVLO threshold and 2.5V, the IC still maintains its operation. However, the spec is not assured.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the isolation and PWM switches when the typical junction temperature of 160°C is exceeded. The IC restarts if the junction temperature drops by 15°C.

ENABLE

Connecting the EN pin low turns off the power switch immediately, but keeps the isolation FET on. If the EN pin is logic low for more than 74ms, the IC turns off the isolation FET and enters shutdown mode drawing less than 1µA current. The enable input pin has an internal 800kΩ pull down resistor to disable the device when the pin is floating.

FREQUENCY SELECTION

The FSW pin can be connected to either a logic high or logic low to program the switching frequency to1.2MHz or 600kHz respectively. The 600kHz switching frequency provides better efficiency because of lower switching losses. This advantage becomes more evident at light load when switching losses dominate overall losses. The higher switching frequency shrinks external component size and thus the size of power solution. High switching frequency also improves load transient response since the smaller value inductor takes less time to ramp up and down current. The other benefits of high switching frequency are lower output ripples and a higher maximum output current. Overall, it is recommended to use 1.2MHz switching frequency unless light load efficiency is a major concern.

The FSW pin has internal 800kΩ pull up resistor to the VIN pin. Floating this pin programs the switching frequency to 1.2MHz.

MAXIMUM and MINIMUM OUTPUT CURRENT

The over-current limit in a boost converter limits the maximum input current and thus maximum input power from a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the over-current limit, the input voltage, the output voltage and the conversion efficiency all affect maximum current output. Since the over-current limit clamps the peak inductor current, the current ripple has to be subtracted to derive maximum DC current. The current ripple is a function of the switching frequency, the inductor value and the duty cycle.

$$I_p = \frac{1}{L \times \left(\frac{1}{Vout + Vf - Vin} + \frac{1}{Vin}\right) \times Fs} \quad (1)$$

where

Ip = inductor peak to peak ripple
L = inductor value
Vf = power diode forward voltage
Fs = Switching frequency

The following equations take into account of all the above factors for maximum output current calculation.

$$Iout\_max = \frac{Vin \times \left(Ilim - \frac{I_p}{2}\right) \times \eta}{Vout} \quad (2)$$

where

Ilim = overcurrent limit
η = conversion efficiency

To minimize the variation in the overcurrent limit threshold, the TPS61080/1 uses the VIN and OUT pin voltage to compensate for the variation caused by the slope compensation. However, the threshold still has some dependency on the VIN and OUT voltage. Use Figure 6 to Figure 9 to identify the typical over-current limit in your application, and use 25% tolerance to account for temperature dependency and process variations.

Because of the minimum duty cycle of each power switching cycle of TPS61080/1, the device can lose regulation at the very light load. Use the following equations to calculate PWM duty cycle under discontinues conduction mode (DCM).

$$Ipeak = \sqrt{2 \times Iload \times \frac{Vout + Vf - Vin}{L \times Fs}}$$

$$D = L \times \frac{Ipeak}{Vin} \times Fs \quad (3)$$

Where

Ipeak = inductor peak to peak ripple in DCM
Iload = load current
D = PWM switching duty cycle

If the calculated duty cycle is less than 5%, minimum load should be considered to the boost output to ensure regulation. Figure 19 provides quick reference to identify the minimum load requirements for two input voltages.

APPLICATION INFORMATION

PROGRAM OUTPUT VOLTAGE

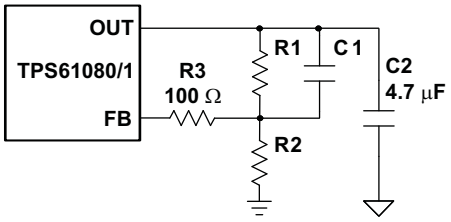


Figure 20. Feed Forward Capacitor Connecting With Feedback Resistor Divider

To program the output voltage, select the values of R1 and R2 (See Figure 20) according to the following equation.

$$R1 = R2 \times \left(\frac{Vout}{1.229V} - 1\right) \quad (4)$$

A optimum value for R2 is around 50kΩ which sets the current in the resistor divider chain to 1.229V/50kΩ = 24.58µA. The output voltage tolerance depends on the V_{FB} accuracy and the resistor divider.

FEED FORWARD CAPACITOR

A feed forward capacitor on the feedback divider, shown in Figure 20, improves transient response and phase margin. This network creates a low frequency zero and high frequency pole at

$$F_Z = \frac{1}{2\pi R1 \times C1} \quad (5)$$

$$F_P = \left(\frac{1}{R1} + \frac{1}{R2}\right)\frac{1}{2\pi C1} \quad (6)$$

The frequency of the pole is determined by C1 and paralleled resistance of R1 and R2. For high output voltage, R1 is much bigger than R2. So

$$F_P = \frac{1}{2\pi R2C1} \text{ when } R1 >> R2. \quad (7)$$

The loop gains more phase margin from this network when (Fz+Fp)/2 is placed right at crossover frequency, which is approximately 15kHz with recommended L and C. The typical value for the zero frequency is between 1kHz to 10KHz. For high output voltage, the zero and pole are further apart which makes the feed forward capacitor very effective. For low output voltage, the benefit of the feed forward capacitor is less visible. Table 2 gives the typical R1, R2 and the feed forward capacitor values at the certain output voltage. However, the transient response is not greatly improved which implies that the zero frequency is too high or low to increase the phase margin.

Table 2. Recommended Feed Forward Capacitor Values With Different Output Voltage

Output Voltage	R1	R2	C1(Feed Forward)
12V	437kΩ	49.9kΩ	33pF
16V	600kΩ	49.9kΩ	42pF
20V	762kΩ	49.9kΩ	56pF
25V	582kΩ	30.1kΩ	120pF

The 100Ω resistor is added to reduce noise coupling from the OUT to the FB pin through the feed forward capacitor. Without the resistor, the regulator may oscillate at high output current.

SOFT START CAPACITOR

The voltage at the SS pin clamps the internal reference voltage, which allows the output voltage to ramp up slowly. The soft start time is calculated as

$$t_{ss} = \frac{C_{ss} \times 1.229}{I_{ss}} \quad (8)$$

where

C_{ss} = soft start capacitor

I_{ss} = soft start bias current (TYP 5 μA)

1.229V is the typical value of the reference voltage.

During start up, input current has to be supplied to charge the output capacitor. This current is proportional to rising slope of the output voltage, and peaks when output reaches regulation.

$$I_{in\_cout} = C_{out} \frac{I_{ss} \times V_{out}}{C_{ss} \times V_{in} \times \eta} \quad (9)$$

Where

I_{in_cout} = additional input current for charging the output capacitor

The maximum input during soft start is

$$I_{in\_ss} = I_{in\_cout} + \frac{V_{out}}{V_{in} \times \eta} \times I_{load} \quad (10)$$

Output overshoot can occur if the input current at startup exceeds the inductor saturation current and/or reaches current limit because the error amplifier loses control of the voltage feedback loop. The in-rush current can also pull down input sources, potentially causing system reset. Therefore, select C_{ss} to make I_{in_ss} stay below the inductor saturation current, the IC over current limit and the input's maximum supply current.

TPS61080/1 can also be configured for constant current output, as shown in the typical applications. In this configuration, a current sense resistor is connected to FB pin for output current regulation. In order to reduce power loss on the sense resistor, FB pin reference voltage can be lowered by connecting a resistor to the SS pin The new reference voltage is simply the resistor value times the SS pin bias current. However, keep in mind that this reference has higher tolerance due to the tolerance of the bias current and sense resistor, and the offset of the clamp circuit. Refer to the specification V_{CLP} and I_{SS} to calculate the tolerance as following.

$$K_{ref} = \sqrt{K_{Vclp}^2 + K_{Iss}^2 + K_R^2} \quad (11)$$

Where

K_{ref} = percentage tolerance of the FB reference voltage.
K_{Vclp} = percentage tolerance of the clamp circuit.
K_{Iss} = percentage tolerance of the SS pin bias current.
K_R = percentage tolerance of the SS pin resistor.

Without considering the SS pin resistor tolerance, the FB reference voltage has ±5.6% under the room temperature.

INDUCTOR SELECTION

Because the selection of the inductor affects steady state operation, transient behavior and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

The inductor's inductance value determines the inductor ripple current. It is generally recommended to set peak to peak ripple current given by Equation 4 to 30–40% of DC current. Also, the inductor value should not be beyond the range in the recommended operating conditions table. It is a good compromise of power losses and inductor size. Inductor DC current can be calculated as

$$I_{L\_DC} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta} \quad (12)$$

The internal loop compensation for PWM control is optimized for the external component shown in the typical application circuit with consideration of component tolerance. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM in which inductor current ramps down to zero before the end of each switching cycle. It reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. An inductor with larger inductance reduces the gain and phase margin of the feedback loop, possibly resulting in instability.

For these reasons, 10µH inductors are recommended for TPS61080 and 4.7µH inductors for TPS61081 for most applications. However, 10µH inductor is also suitable for 600kHz switching frequency.

Regulator efficiency is dependent on the resistance of its high current path and switching losses associated with the PWM switch and power diode. Although the TPS61080/1 has optimized the internal switches, the overall efficiency still relies on inductor's DC resistance (DCR); Lower DCR improves efficiency. However, there is a trade off between DCR and inductor size, and shielded inductors typically have higher DCR than unshielded ones. Table 3 list recommended inductor models.

Table 3. Recommended Inductor for TPS61080/1

TPS61080	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	Size (L×W×H mm)	VENDOR
VLCF4018T	10	188	0.74	4.0 × 4.0 × 1.8	TDK
CDRH4D16NP	10	118	0.96	4.0 × 4.0 × 1.8	Sumida
LQH43CN100K	10	240	0.65	4.5 × 3.6 × 2.6	Murata
TPS61081	**L (µH)**	**DCR MAX (mΩ)**	**SATURATION CURRENT (A)**	**Size (L×W×H mm)**	**VENDOR**
VLCF5020T	4.7	122	1.74	5.0 × 5.0 × 2.0	TDK
VLCF5014A	6.8	190	1.4	5.0 × 5.0 × 1.4	TDK
CDRH4D14/HP	4.7	140	1.4	4.8 × 4.8 × 1.5	Sumida
CDRH4D22/HP	10	144	1.5	5.0 × 5.0 × 2.4	Sumida

INPUT AND OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to meet output ripple and loop stability requirements. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{out} = \frac{(V_{out} - V_{in})I_{out}}{V_{out} \times Fs \times V_{ripple}} \quad (13)$$

V_{ripple} = Peak to peak output ripple.

For VIN = 3.6V, Vout = 20V, and Fs = 1.2MHz, 0.1% ripple (20mV) would require 1.0µ capacitor, however, the minimum recommended output capacitor for control loop stability is 4.7 µF. For this value, ceramic capacitors are a good choice for its size, cost and availability.

The additional output ripple component caused by ESR is calculated using:

$$V_{ripple\_ESR} = I_{out} \times R_{ESR} \quad (14)$$

Due to its low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

During a load transient, the output capacitor at the output of the boost converter has to supply or absorb transient current before the inductor current ramps up its steady state value. Larger capacitors always help to reduce the voltage over and under shoot during a load transient. A larger capacitor also helps loop stability. Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The Dc bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, almost leave margin on voltage rating to ensure adequate capacitance.

The popular vendors for high value ceramic capacitors are:

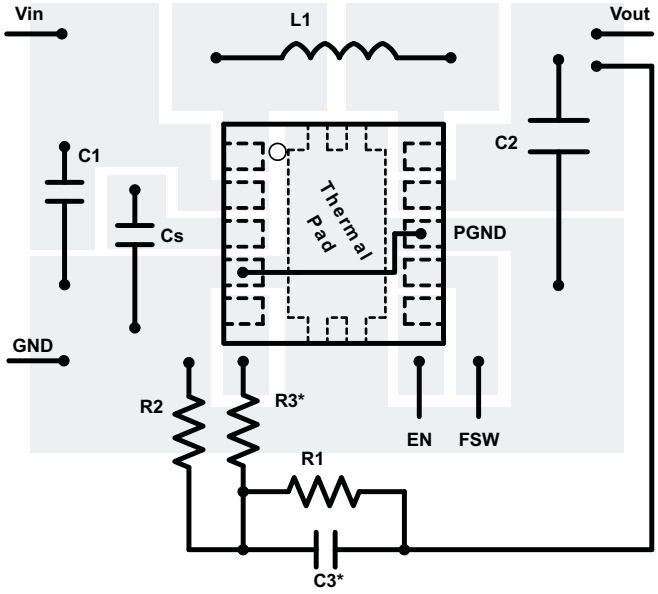
TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

LAYOUT CONSIDERATION

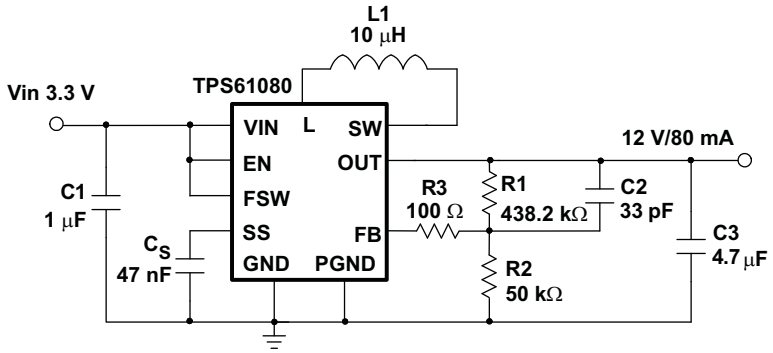
As for all switching power supplies, the layout is an important step in the design, especially for high current and high switching frequencies. If layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for high current paths and for power ground tracks. Input capacitor needs not only close to the VIN, but also to the GND pin to reduce the voltage ripple seen by the IC. The L and SW pin are conveniently located on the edge of the IC, therefore inductor can be placed close to the IC. The output capacitor needs to be placed near the load to minimize ripple and maximize transient performance.

To minimize the effects of ground noise, use a common node for all power ground that is connected to the PGND pin, and a different one for signal ground tying to the GND pin. Connect two ground nodes together at the load if possible. This allows the GND pin to be close to the output ground for good DC regulation. Any voltage difference between these two nodes would be gained up by feedback divider on the output. It is also beneficial to have the ground of the output capacitor close to PGND since there is a large current between them. To lay out signal ground, it is recommended to use short traces separated from power ground traces.



TYPICAL APPLICATION

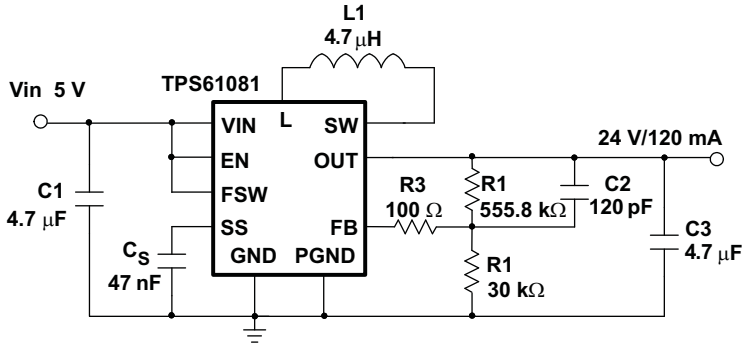
3.3 V to 12 V, 80 mA Step-up DC/DC Converter



L1: Sumida CDRH4D16FBNP-100NC
C1: Murata GRM188R60J105K; C3: Murata GRM219R61C475K

Figure 21.

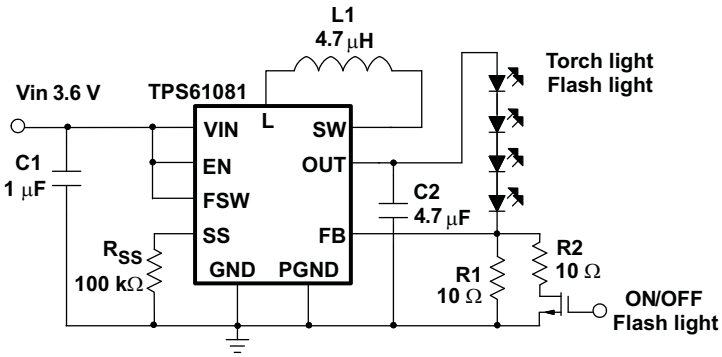
5 V to 24 V, 120 mA Step-up DC/DC Converter



L1: TDK VLCF5020T- 4RN1R7-1
C1: Murata GRM188R60J475K; C3: Murata GRM55ER61H475K

Figure 22.

50 mA Torch Light and 100 mA Flash Light

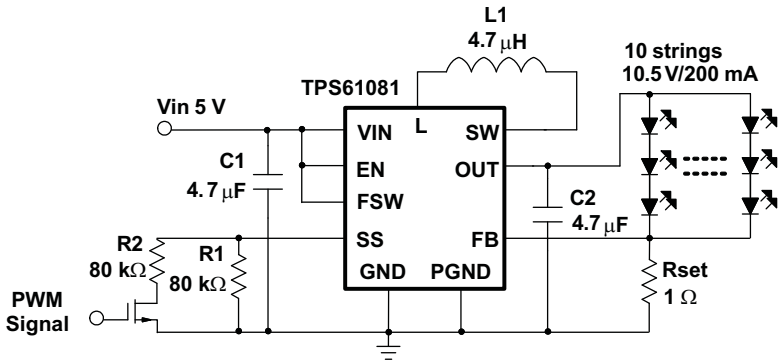


L1: TDK VLCF5020T- 4R7N1R7-1
C1: Murata GRM188R60J105K; C2: Murata GRM219R61C475K

Figure 23.

TYPICAL APPLICATION (continued)

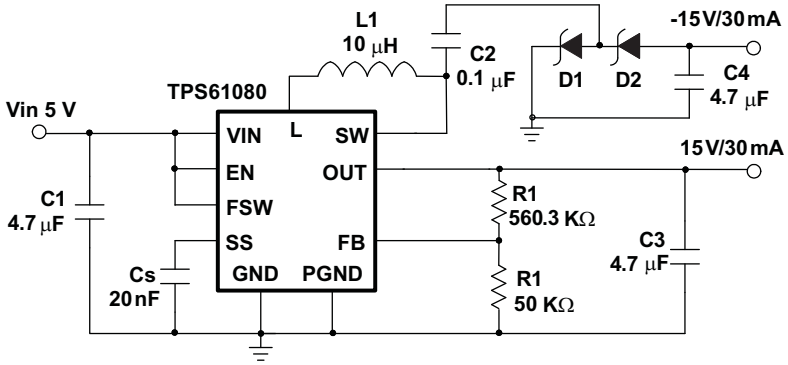
30 WLEDs Driver in Media Factor Form Display



L1: TDK VLCF5020T- 4R7N1R7-1
C1: Murata GRM188R60J475K; C2: Murata GRM219R61C475K

Figure 24.

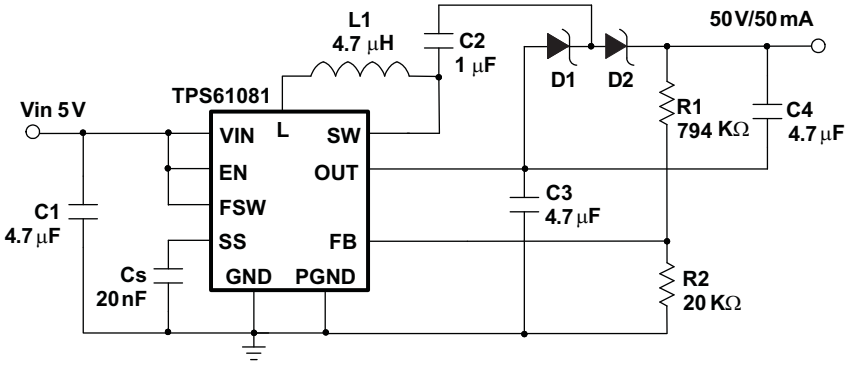
+/– 15 V Dual Output Converter



L1: Sumida CDRH4D16NP-100NC
C1: Murata GRM188R60J475K; C3,C4: Murata GRM219R61C475K
D1,D2: ON Semiconductor MBR0520

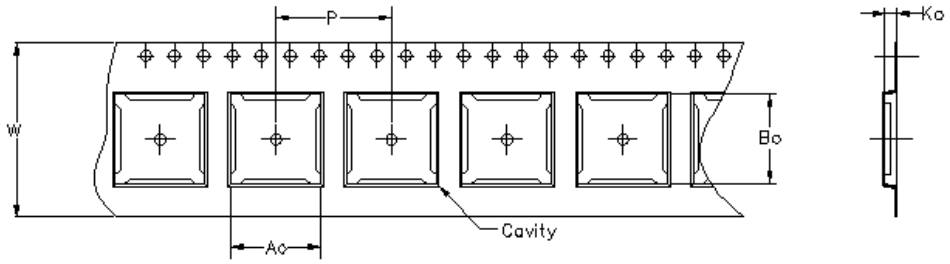
Figure 25.

5 V to 50 V, 50 mA Step-up DC/DC Converter with Output Doubler



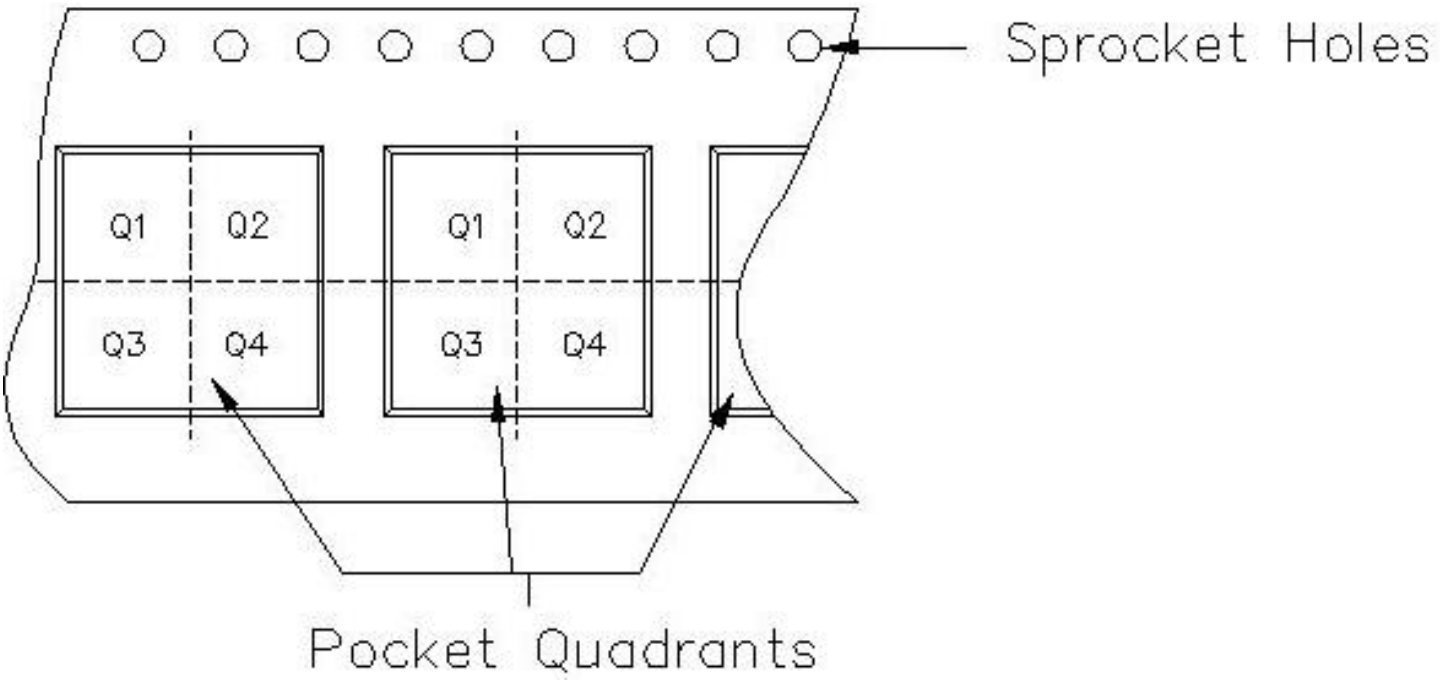
L1: TDK VLCF5020T-4R7N1R7-1
C1: Murata GRM188R60J475K; C3: Murata GRM219R61C475K
D1,D2: ON Semiconductor MBR0520

Figure 26.



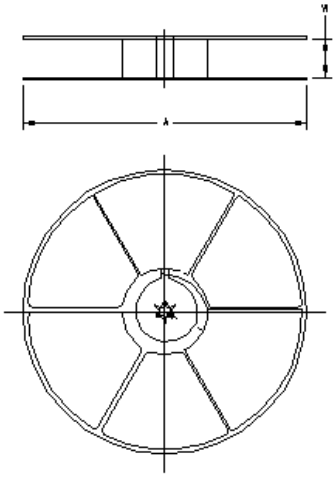
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



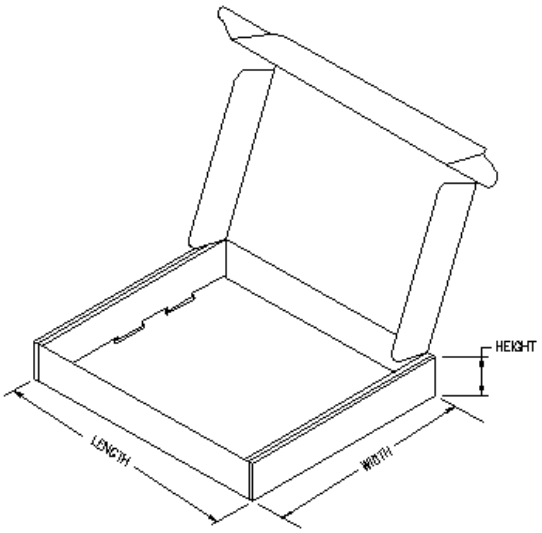
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61080DRCR	DRC	10	MLA	330	12	3.3	3.3	1.1	8	12	PKGORNT2TR-MSP
TPS61080DRCT	DRC	10	MLA	180	12	3.3	3.3	1.1	8	12	PKGORNT2TR-MSP
TPS61081DRCR	DRC	10	MLA	330	12	3.3	3.3	1.1	8	12	PKGORNT2TR-MSP
TPS61081DRCT	DRC	10	MLA	180	12	3.3	3.3	1.1	8	12	PKGORNT2TR-MSP

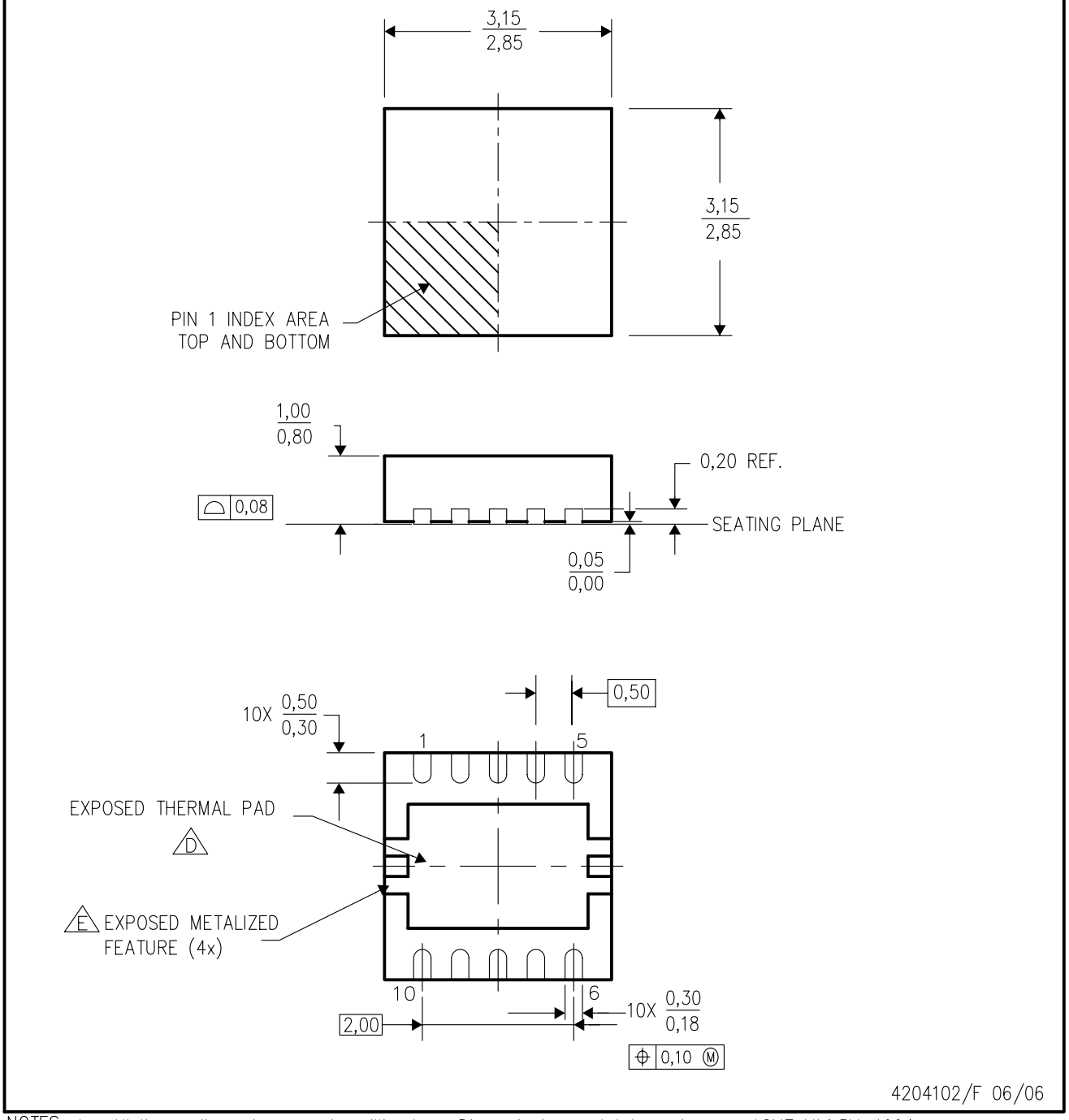


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS61080DRCR	DRC	10	MLA	346.0	346.0	29.0
TPS61080DRCT	DRC	10	MLA	190.0	212.7	31.75
TPS61081DRCR	DRC	10	MLA	346.0	346.0	29.0
TPS61081DRCT	DRC	10	MLA	190.0	212.7	31.75


HEIGHT
LENGTH
WIDTH

DRC (S–PDSO–N10) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL PAD MECHANICAL DATA

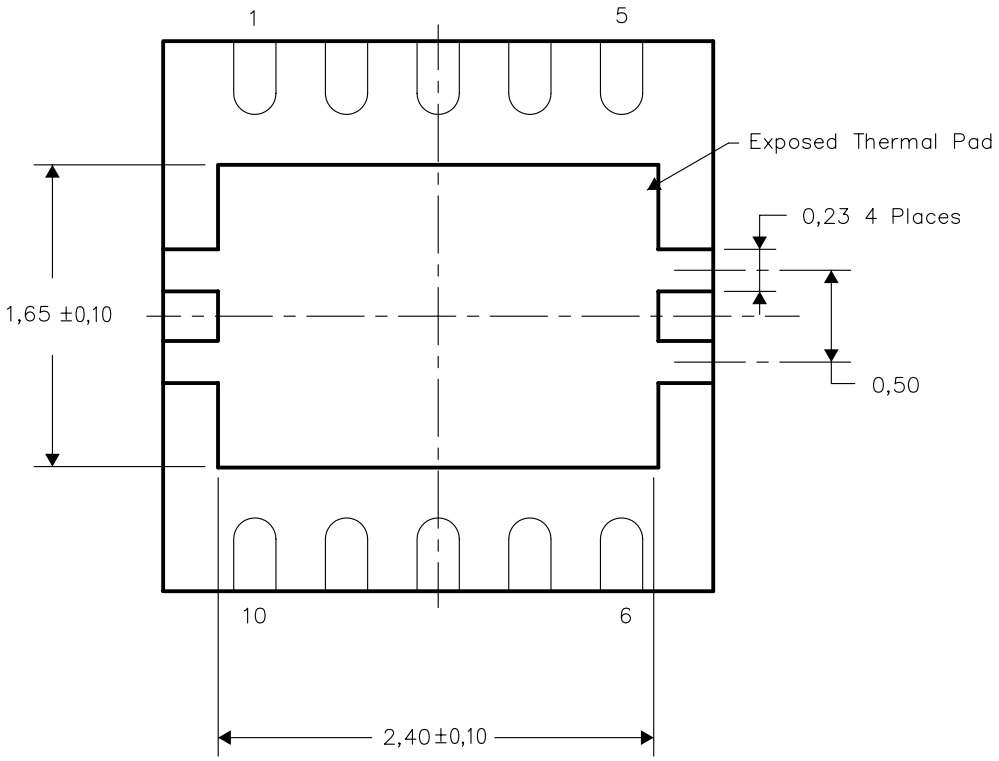
DRC (S–PDSO–N10)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

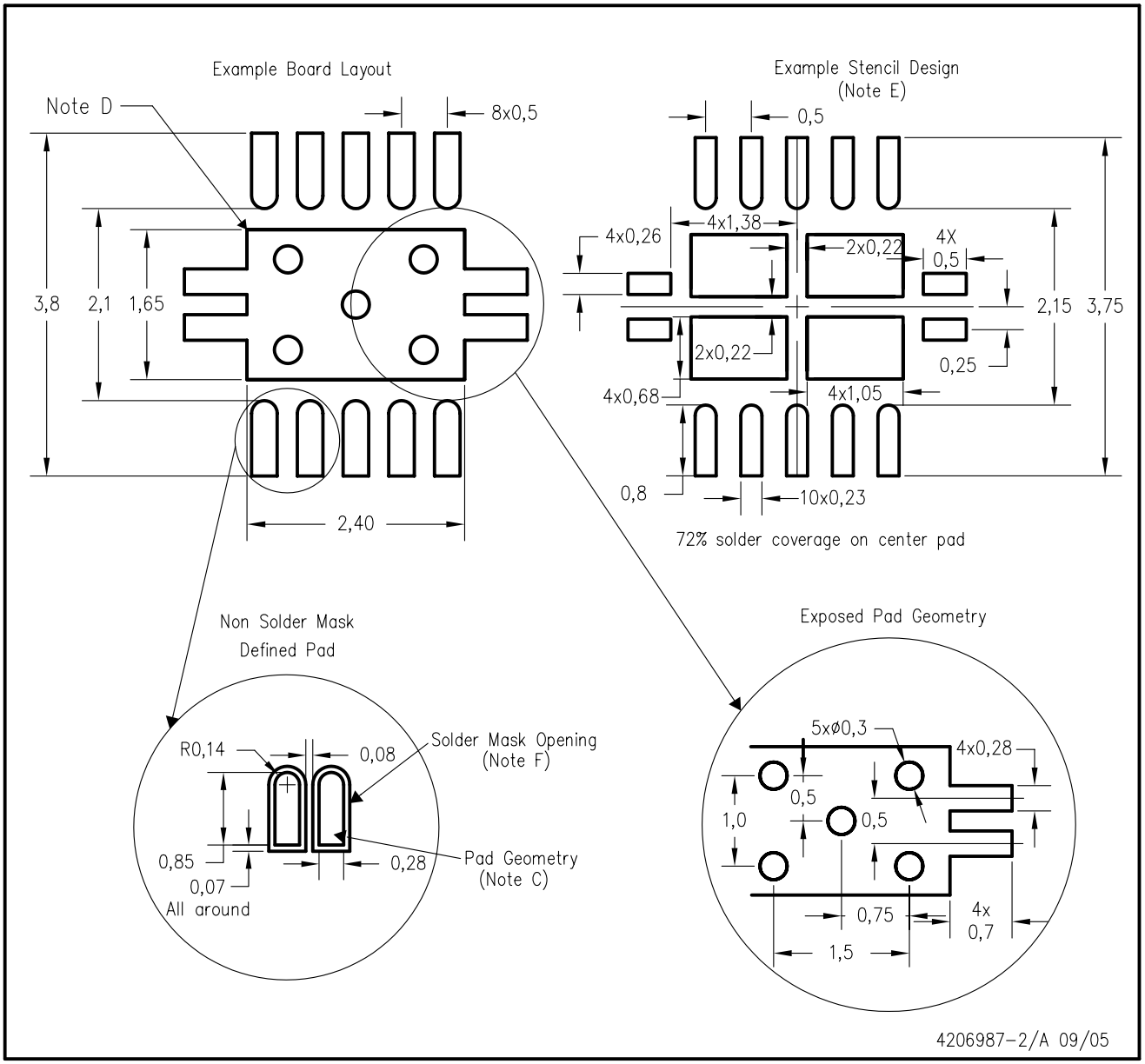


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRC (S–PDSO–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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