

## DM74ALS169B

### Synchronous Four-Bit Up/Down Counters

#### General Description

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The DM74ALS169B is a four-bit binary up/down counter. The carry output is decoded to prevent spikes during normal mode of counting operation. Synchronous operation is provided so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of clock input waveform.

These counters are fully programmable; that is, the outputs may each be preset either HIGH or LOW. The load input circuitry allows loading with carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count enable inputs ( $\bar{P}$  and  $\bar{T}$ ) must be LOW to count. The direction of the count is determined by the level of the up/down input. When the input is HIGH, the counter counts UP; when LOW, it counts DOWN. Input T is fed forward to enable the carry outputs. The carry output thus enabled will produce a low level output pulse with a duration approximately equal to the high portion of the  $Q_A$  output when counting UP, and approximately equal to the low portion of the  $Q_A$  when counting DOWN. This low level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable  $\bar{P}$  or  $\bar{T}$  inputs are allowed regardless of the level of the clock input.

The control functions for these counters are fully synchronous. Changes at control inputs (enable  $\bar{P}$ , enable  $\bar{T}$ , load, up/down) which modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

#### Features

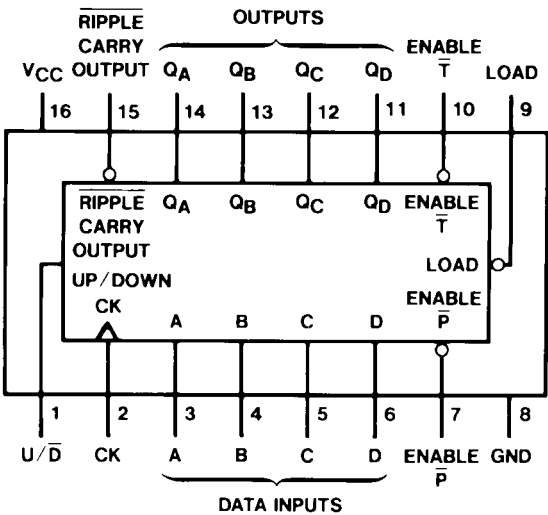
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and  $V_{CC}$  range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Synchronously programmable
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- ESD inputs

#### Ordering Code:

| Order Number | Package Number | Package Description                                                         |
|--------------|----------------|-----------------------------------------------------------------------------|
| DM74ALS169BM | M16A           | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74ALS169BN | N16E           | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide       |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

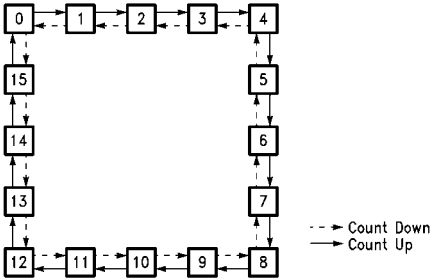
Connection Diagram



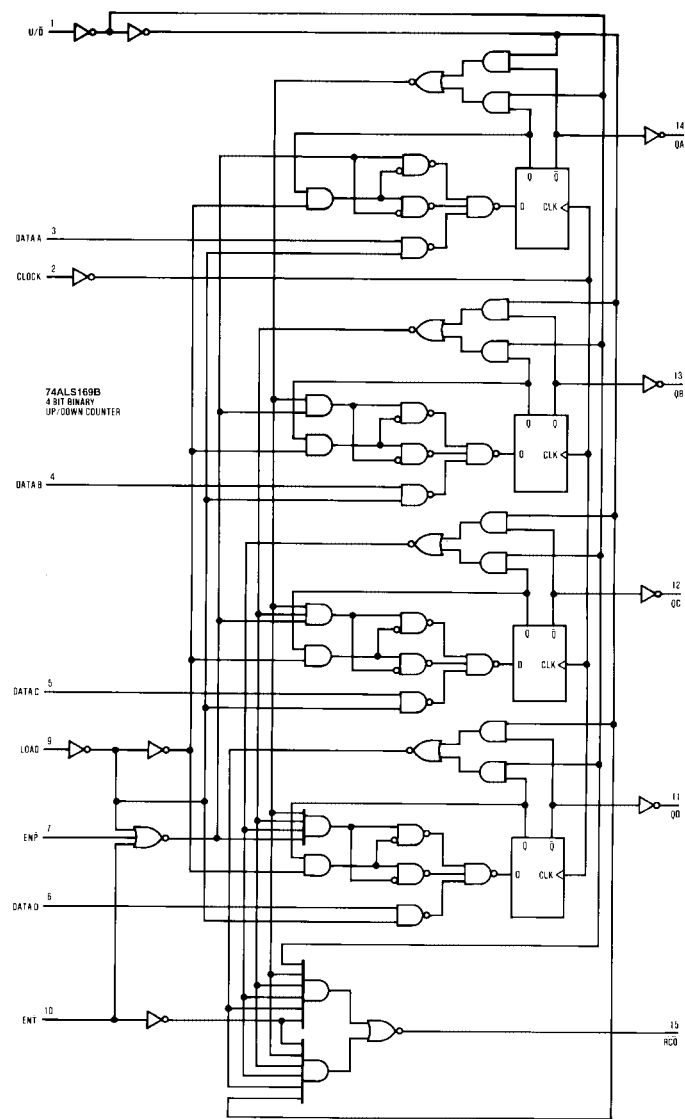
Mode Select Table

| LOAD | $\overline{EP}$ | $\overline{ET}$ | $\overline{U/D}$ | Action on Rising Clock Edge    |
|------|-----------------|-----------------|------------------|--------------------------------|
| L    | X               | X               | X                | Load ( $P_n \rightarrow Q_n$ ) |
| H    | L               | L               | H                | Count Up (Increment)           |
| H    | L               | L               | L                | Count Down (Decrement)         |
| H    | H               | X               | X                | No Change (Hold)               |
| H    | X               | H               | X                | No Change (Hold)               |

State Diagram



## Logic Diagram



**Absolute Maximum Ratings**(Note 1)

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range | 0°C to +70°C    |
| Storage Temperature Range            | –65°C to +150°C |
| Typical $\theta_{JA}$                |                 |
| N Package                            | 78.1°C/W        |
| M Package                            | 106.8°C/W       |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

| Symbol    | Parameter                 |                                      | Min           | Nom | Max  | Units |
|-----------|---------------------------|--------------------------------------|---------------|-----|------|-------|
| $V_{CC}$  | Supply Voltage            |                                      | 4.5           | 5   | 5.5  | V     |
| $V_{IH}$  | HIGH Level Input Voltage  |                                      | 2             |     |      | V     |
| $V_{IL}$  | LOW Level Input Voltage   |                                      |               |     | 0.8  | V     |
| $I_{OH}$  | HIGH Level Output Current |                                      |               |     | –0.4 | mA    |
| $I_{OL}$  | LOW Level Output Current  |                                      |               |     | 8    | mA    |
| $f_{CLK}$ | Clock Frequency           |                                      | 0             |     | 40   | MHz   |
| $t_{SU}$  | Setup Time (Note 2)       | Data;<br>A, B, C, D                  | 15 $\uparrow$ | 6   |      | ns    |
|           |                           | $\overline{En\ P}, \overline{En\ T}$ | 15 $\uparrow$ | 8   |      | ns    |
|           |                           | $\overline{Load}$                    | 15 $\uparrow$ | 8   |      | ns    |
|           |                           | $\overline{U/D}$                     | 15 $\uparrow$ | 10  |      | ns    |
| $t_H$     | Hold Time (Note 2)        | Data;<br>A, B, C, D                  | 0 $\uparrow$  | –3  |      | ns    |
|           |                           | $\overline{En\ P}, \overline{En\ T}$ | 0 $\uparrow$  | –3  |      | ns    |
|           |                           | $\overline{Load}$                    | 0 $\uparrow$  | –4  |      | ns    |
|           |                           | $\overline{U/D}$                     | 0 $\uparrow$  | –4  |      | ns    |
| $t_W$     | Width of Clock Pulse      |                                      | 13            |     |      | ns    |

**Note 2:** The symbol ( $\uparrow$ ) indicates that the rising edge of the clock is used as reference.

## Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$

| Symbol   | Parameter                            | Conditions                                             | Min          | Typ  | Max  | Units   |
|----------|--------------------------------------|--------------------------------------------------------|--------------|------|------|---------|
| $V_{IK}$ | Input Clamp Voltage                  | $V_{CC} = 4.5V$ , $I_I = -18\text{ mA}$                |              |      | -1.5 | V       |
| $V_{OH}$ | HIGH Level<br>Output Voltage         | $I_{OH} = -0.4\text{ mA}$<br>$V_{CC} = 4.5V$ to $5.5V$ | $V_{CC} - 2$ |      |      | V       |
| $V_{OL}$ | LOW Level<br>Output Voltage          | $V_{CC} = 4.5V$<br>$I_{OL} = 8\text{ mA}$              |              | 0.35 | 0.5  | V       |
| $I_I$    | Input Current @ Max<br>Input Voltage | $V_{CC} = 5.5V$ , $V_{IH} = 7V$                        |              |      | 0.1  | mA      |
| $I_{IH}$ | HIGH Level Input Current             | $V_{CC} = 5.5V$ , $V_{IH} = 2.7V$                      |              |      | 20   | $\mu A$ |
| $I_{IL}$ | LOW Level Input Current              | $V_{CC} = 5.5V$ , $V_{IL} = 0.4V$                      |              |      | -0.2 | mA      |
| $I_O$    | Output Drive Current                 | $V_{CC} = 5.5V$ , $V_O = 2.25V$                        | -30          |      | -112 | mA      |
| $I_{CC}$ | Supply Current                       | $V_{CC} = 5.5V$                                        |              | 15   | 25   | mA      |

## Switching Characteristics

over recommended operating free air temperature range

| Symbol    | Parameter                                          | Conditions                                                             | From                      | To                               | Min | Max | Units |
|-----------|----------------------------------------------------|------------------------------------------------------------------------|---------------------------|----------------------------------|-----|-----|-------|
| $f_{MAX}$ | Maximum Clock Frequency                            |                                                                        |                           |                                  | 40  |     | MHz   |
| $t_{PLH}$ | Propagation Delay Time<br>LOW-to-HIGH Level Output | $V_{CC} = 4.5V$ to $5.5V$<br>$R_L = 500\Omega$<br>$C_L = 50\text{ pF}$ | Clock                     | $\overline{\text{Ripple Carry}}$ | 3   | 20  | ns    |
| $t_{PHL}$ | Propagation Delay Time<br>HIGH-to-LOW Level Output |                                                                        | Clock                     | $\overline{\text{Ripple Carry}}$ | 6   | 20  | ns    |
| $t_{PLH}$ | Propagation Delay Time<br>LOW-to-HIGH Level Output |                                                                        | Clock                     | Any Q                            | 2   | 15  | ns    |
| $t_{PHL}$ | Propagation Delay Time<br>HIGH-to-LOW Level Output |                                                                        | Clock                     | Any Q                            | 5   | 20  | ns    |
| $t_{PLH}$ | Propagation Delay Time<br>LOW-to-HIGH Level Output |                                                                        | En T                      | $\overline{\text{Ripple Carry}}$ | 2   | 13  | ns    |
| $t_{PHL}$ | Propagation Delay Time<br>HIGH-to-LOW Level Output |                                                                        | En T                      | $\overline{\text{Ripple Carry}}$ | 3   | 16  | ns    |
| $t_{PLH}$ | Propagation Delay Time<br>LOW-to-HIGH Level Output |                                                                        | $U/\overline{D}$ (Note 3) | $\overline{\text{Ripple Carry}}$ | 5   | 19  | ns    |
| $t_{PHL}$ | Propagation Delay Time<br>HIGH-to-LOW Level Output |                                                                        | $U/\overline{D}$ (Note 3) | $\overline{\text{Ripple Carry}}$ | 5   | 19  | ns    |

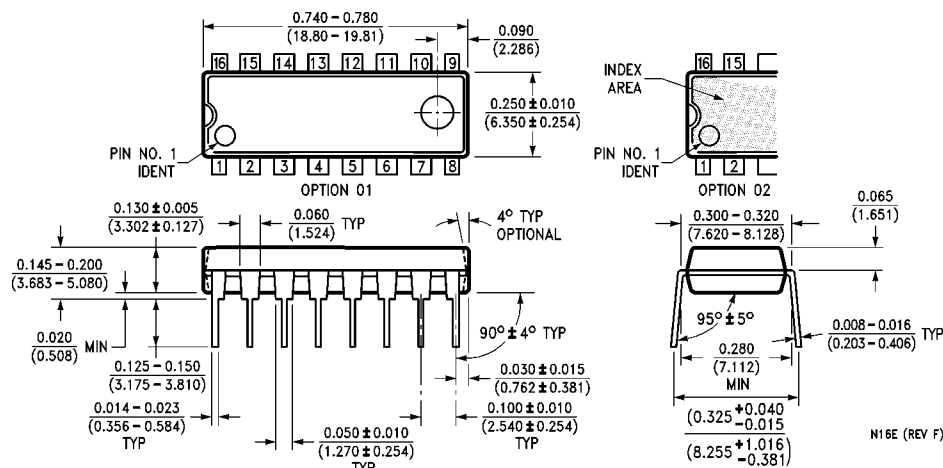
**Note 3:** Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum, the ripple carry output will be out of phase.

# Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow  
Package Number M16A

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N16E

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)