

# FlexiSLIC™

Subscriber Line Interface Circuit

PBL 38621/2, Version 2

Wired Communications



Never stop thinking.

## FlexiSLIC

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DS1

**Previous Version:**

Page	Subjects (major changes since last revision)

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<b>Table of Contents</b>		<b>Page</b>
<b>1</b>	<b>Overview</b> . . . . .	<b>7</b>
1.1	Features . . . . .	7
1.2	Typical Applications . . . . .	7
1.3	Description . . . . .	8
1.4	Block Diagram . . . . .	9
<b>2</b>	<b>Pin Configuration</b> . . . . .	<b>10</b>
<b>3</b>	<b>Electrical Characteristics</b> . . . . .	<b>14</b>
3.1	Characteristics . . . . .	16
<b>4</b>	<b>Application Schematic</b> . . . . .	<b>26</b>
4.1	Recommended Components . . . . .	27
4.2	Design Supporting Tools . . . . .	28
<b>5</b>	<b>Transmission</b> . . . . .	<b>29</b>
5.1	General . . . . .	29
5.2	Two-Wire Impedance . . . . .	30
5.3	Two-Wire to Four-Wire Gain . . . . .	30
5.4	Four-Wire to Two-Wire Gain . . . . .	31
5.5	Four-Wire to Four-Wire Gain . . . . .	31
5.6	Hybrid Function . . . . .	31
5.7	Longitudinal Impedance . . . . .	33
5.8	Capacitors $C_{TC}$ and $C_{RC}$ . . . . .	33
5.9	AC - DC Separation Capacitor, $C_{HP}$ . . . . .	33
5.10	High-pass Transmit Filter . . . . .	33
5.11	Capacitor $C_{LP}$ . . . . .	33
<b>6</b>	<b>Battery Feed</b> . . . . .	<b>35</b>
6.1	CODEC Receive Interface . . . . .	35
6.2	Programmable Overhead Voltage (POV) . . . . .	38
6.3	Analog Temperature Guard . . . . .	39
<b>7</b>	<b>Loop Monitoring Functions</b> . . . . .	<b>39</b>
7.1	Loop Current Detector . . . . .	39
7.2	Ground Key Detector . . . . .	39
7.3	Ring Trip Detector . . . . .	40
<b>8</b>	<b>Relay Driver</b> . . . . .	<b>40</b>
<b>9</b>	<b>Control Inputs</b> . . . . .	<b>41</b>
9.1	Open Circuit ( $C3, C2, C1 = 0, 0, 0$ ) . . . . .	41
9.2	Ringling ( $C3, C2, C1 = 0, 0, 1$ ) . . . . .	41
9.3	Active States . . . . .	41
<b>10</b>	<b>Overvoltage Protection</b> . . . . .	<b>41</b>

<b>Table of Contents</b>		<b>Page</b>
10.1	Overvoltage Protection - General .....	41
10.2	Secondary Protection .....	41
<b>11</b>	<b>Power-Up Sequence .....</b>	<b>42</b>
<b>12</b>	<b>Printed Circuit Board Layout .....</b>	<b>42</b>
<b>13</b>	<b>Package Outlines .....</b>	<b>43</b>
13.1	24-pin SSOP Package .....	43
13.2	24-pin SOIC Package .....	44
13.3	28-pin PLCC Package .....	45

<b>List of Figures</b>	<b>Page</b>
Figure 1	Block Diagram . . . . . 9
Figure 2	Pin Configuration, 24L-SOIC, 24L-SSOP and 28L-PLCC (top view). . 10
Figure 3	Overhead Level, $V_{TRO}$ , Two-Wire Port . . . . . 23
Figure 4	Longit. to Metallic, $B_{LME}$ and Longit. to Four-Wire, $B_{LFE}$ Balance . . . . 24
Figure 5	Metallic to Longit., $B_{MLE}$ and Four-Wire to Longit. Balance, $B_{FLE}$ . . . . 24
Figure 6	Overhead Level, $V_{TXO}$ , Four-Wire Transmit Port . . . . . 24
Figure 7	Frequency Response, Insertion Loss, Gain Tracking . . . . . 25
Figure 8	Application Example of PBL 38621/2 with CODEC/filter . . . . . 26
Figure 9	Simplified AC Model of PBL 38621/2 . . . . . 29
Figure 10	Hybrid Function . . . . . 32
Figure 11	Codec Receive Interface . . . . . 36
Figure 12	Battery Feed Characteristics . . . . . 37
Figure 13	Programmable Overhead Voltage (POV). $R_L = 600 \Omega$ or Infinite . . . . 38
Figure 14	<b>P-SSOP-24-1</b> (Plastic Shrink Small Outline Package). . . . . 43
Figure 15	<b>P-DSO-24-1</b> (Plastic Dual Small Outline Package) . . . . . 44
Figure 16	<b>P-LCC-28-2</b> (Plastic Leaded Chip Carrier Package) . . . . . 45

**List of Tables****Page**

Table 1	Pin Definition and Functions . . . . .	10
Table 2	SLIC Operating States . . . . .	13
Table 3	Absolute Maximum Ratings . . . . .	14
Table 4	Operating Range . . . . .	15
Table 5	Characteristics . . . . .	16
Table 6	Resistors (values according to IEC E96 series). . . . .	27
Table 7	Capacitors (values according to IEC E96 series) . . . . .	27
Table 8	Diodes . . . . .	28
Table 9	Feeding Setup . . . . .	34
Table 10	Battery Overhead. . . . .	35
Table 11	Internal bias current of RSN. . . . .	36

# FlexiSLIC

## Subscriber Line Interface Circuit

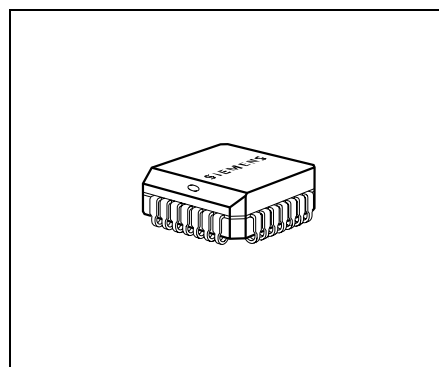
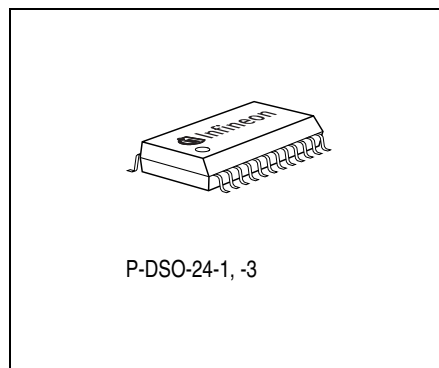
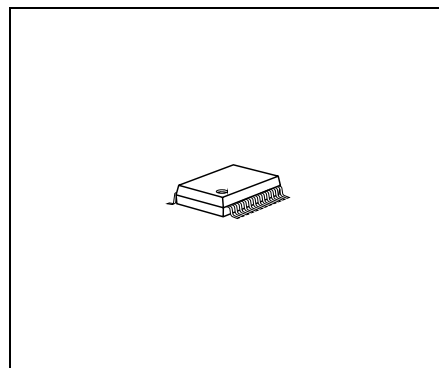
PBL 38621/2

Version 2

## 1 Overview

### 1.1 Features

- 24-pin SSOP package
- High and low battery with automatic switching
- 60 mW on-hook power dissipation in active state
- On-hook transmission
- Long loop battery feed tracks Vbat for maximum line voltage
- Selectable transmit gain (1x or 0.5x)
- No power-up sequence
- 44 V open loop voltage @ -48 V battery feed
- Full longitudinal current capability during on-hook state
- Analog overtemperature protection permits transmission while the protection circuits is active
- Polarity reversal
- Integrated Ring Relay driver
- Ground key detector
- Programmable signal headroom
- -40 °C to +85 °C ambient temperature range



### 1.2 Typical Applications

- Basic functionality Central Office Line card
- Private branch exchange (PABX)
- Digital added mainline (DAML)
- Terminal adapters (CPE)
- ISDN terminal adapters
- Other shortloop applications

Type	Package
PBL 38621/2 SH	P-SSOP-24-1
PBL 38621/2 SO	P-DSO-24-1
PBL 38621/2 QN	P-LCC-28-2



### **1.3 Description**

The PBL 38621/2 Subscriber Line Interface Circuit (SLIC) is a 90 V bipolar integrated circuit for use in PBX, Terminal adapters and other telecommunications equipment. The PBL 38621/2 SLIC has been optimized for low total line interface cost and for a high degree of flexibility in different applications.

The PBL 38621/2 SLIC has constant current feed, programmable to maximum 30 mA. A second lower battery voltage may be connected to the device to reduce short loop power dissipation. The SLIC automatically switches between the two battery supply voltages without need for external components or external control.

The SLIC incorporates loop current, ground key and ring-trip detection functions. The PBL 38621/2 is compatible with loop start signalling.

Two- to four-wire and four- to two-wire voice frequency (VF) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter, for example SiCoFi PEB 2466. The programmable two-wire impedance, complex or real, is set by a simple external network.

Longitudinal voltages are suppressed by a feedback loop in the SLIC and the longitudinal balance specifications meet Bellcore TR909 requirements.

The PBL 38621/2 SLIC package options are 24-pin SSOP, 24-pin SOIC or 28-pin PLCC.



## 1.4 Block Diagram

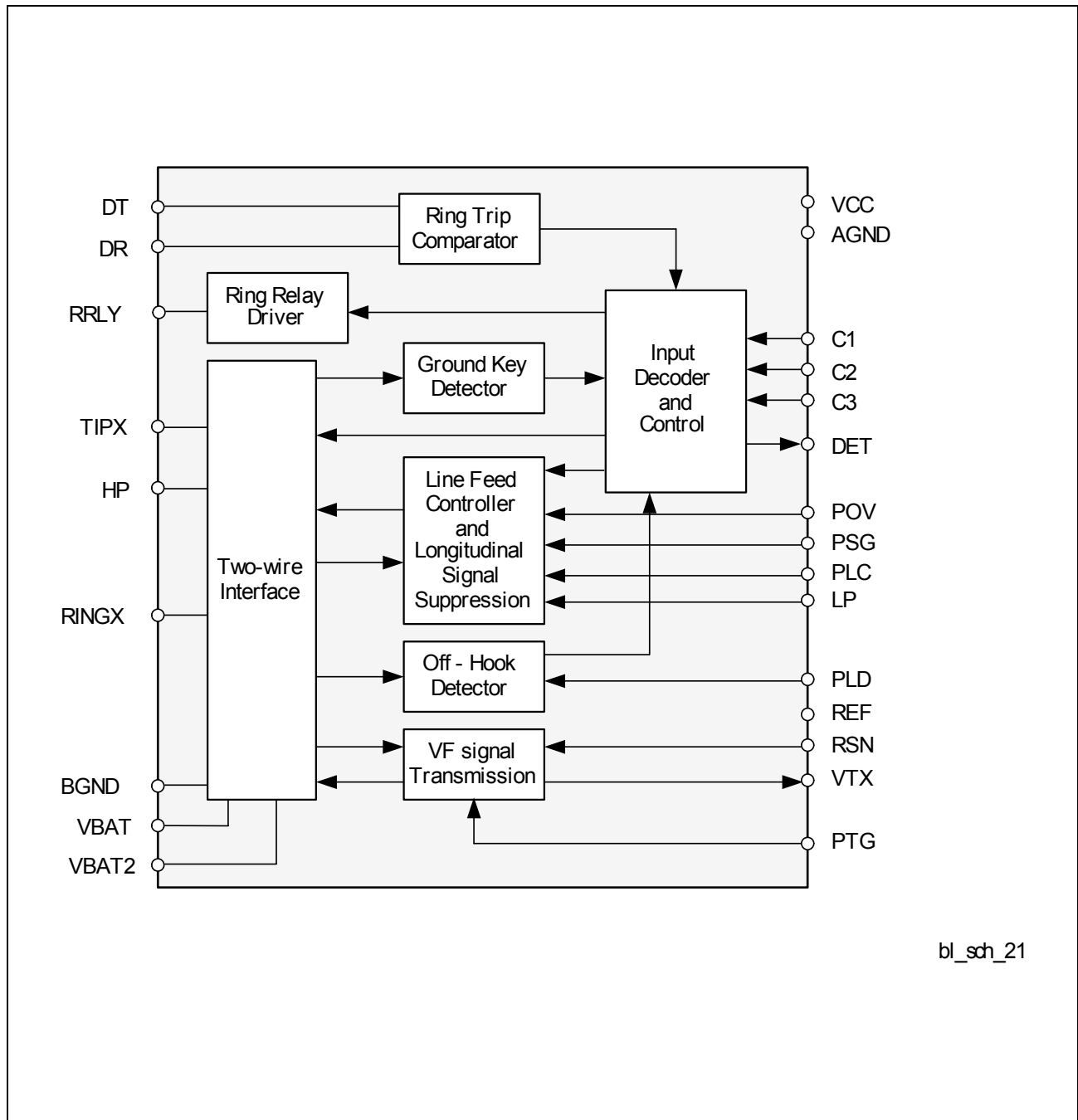
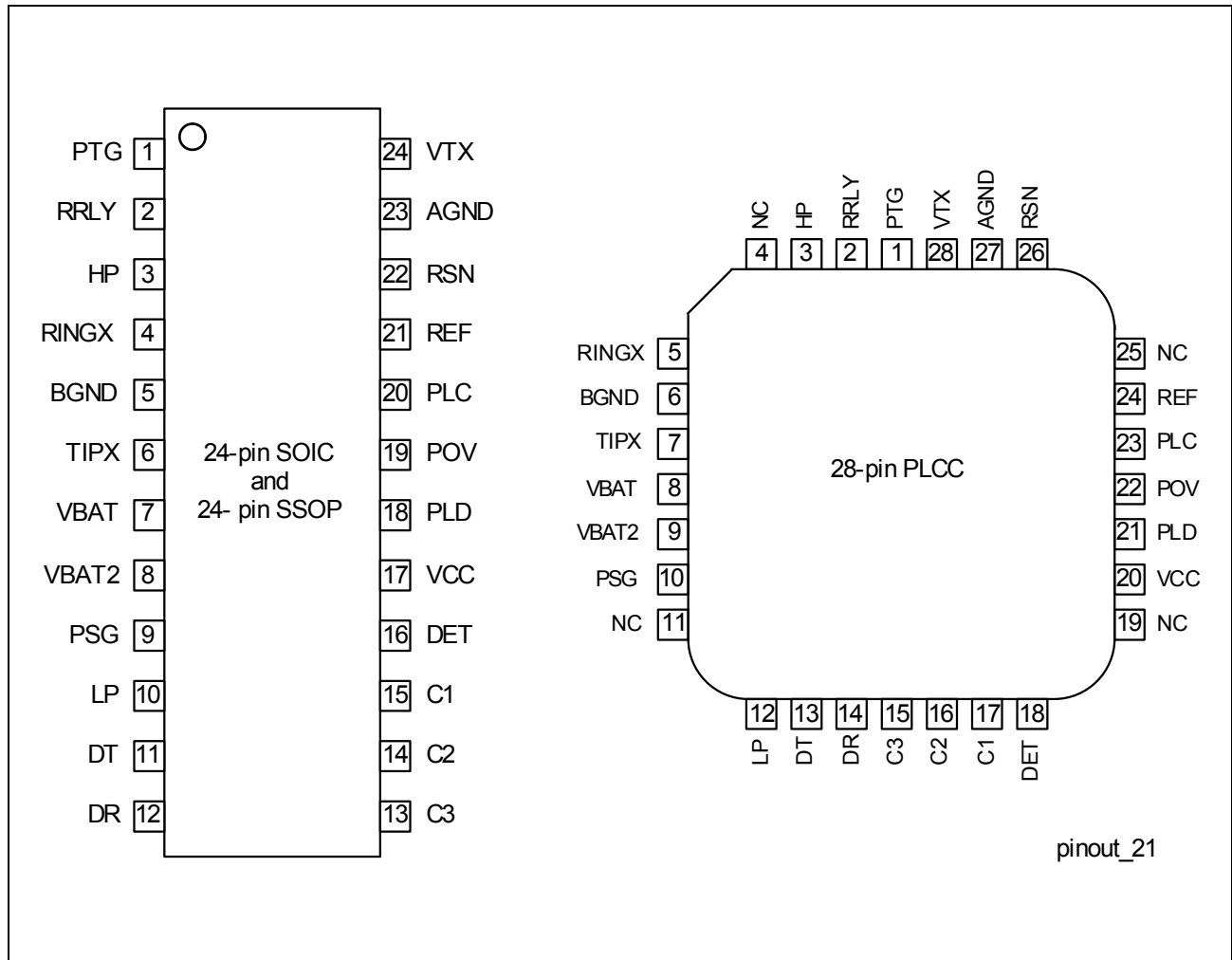


Figure 1 Block Diagram

## 2 Pin Configuration



**Figure 2** Pin Configuration, 24L-SOIC, 24L-SSOP and 28L-PLCC (top view).

**Table 1** Pin Definition and Functions

P-DSO P-SSOP Pin No.	P-LCC Pin No.	Name	I/O	Function
1	1	PTG	–	Programmable transmit gain. Left open transmit gain = 0.0 dB, connected to AGND transmit gain = -6.02 dB.
2	2	RRLY	O	Ring relay driver output. The relay coil may be connected to maximum +14 V.
3	3	HP	–	Connection for high pass filter capacitor, $C_{HP}$ . Other end of $C_{HP}$ connects to TIPX.

**Pin Configuration**
**Table 1 Pin Definition and Functions (cont'd)**

P-DSO P-SSOP Pin No.	P-LCC Pin No.	Name	I/O	Function
4	5	RINGX	–	The RINGX pin connects to the ring lead of the two-wire interface via over voltage protection components and ring relay (and optional test relay).
5	6	BGND	–	Battery ground, should be tied together with AGND.
6	7	TIPX	–	The TIPX pin connects to the tip lead of the two-wire interface via over voltage protection components and ring relay (and optional test relay).
7	8	VBAT	–	Battery supply voltage. Negative with respect to GND.
8	9	VBAT2	–	An optional second (2) Battery Voltage connects to this pin via an external diode.
9	10	PSG	–	Programmable saturation guard. The resistive part of the DC feed characteristics is not used for PBL 38621/2, $R_{SG} = 0 \Omega$
10	12	LP	–	Connection for low pass filter capacitor, $C_{LP}$ . Other end of $C_{LP}$ connects to VBAT.
11	13	DT	I	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The external ring trip network connects to this input.
12	14	DS	I	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The external ring trip network connects to this input.
13	15	C3	I	C1, C2, C3 are digital inputs, which control the SLIC operating states. Refer to <a href="#">Table 2</a> for details.
14	16	C2	I	
15	17	C1	I	

**Pin Configuration**
**Table 1 Pin Definition and Functions (cont'd)**

<b>P-DSO P-SSOP Pin No.</b>	<b>P-LCC Pin No.</b>	<b>Name</b>	<b>I/O</b>	<b>Function</b>
16	18	DET	O	Detector output. Active low when indicating loop or ring-trip detection, active high when indicating ground key detection.
17	20	VCC	–	+5 V power supply.
18	21	PLD	–	Programmable loop detector threshold. The loop detection threshold is programmed by a resistor connected from this pin to AGND.
19	22	POV	–	Programmable overhead voltage. If pin is left open: The overhead voltage is internally set to min 1.0 V in off- and on-hook. If a resistor is connected between this pin and AGND: The overhead voltage can be set to higher values.
20	23	PLC	–	Programmable line current, the constant part of the DC feed characteristic is programmed by a resistor connected from this pin to AGND.
21	24	REF	–	A reference, 49.9 k $\Omega$ , resistor should be connected from this pin to AGND.
22	26	RSN	–	Receive summing node. 200 times the AC current flowing into this pin equals the metallic (transversal) AC current flowing from RINGX to TIPX. Programming networks for two-wire impedance and receive gain connect to the receive node. A resistor should be connected from this pin to AGND.
23	27	AGND	–	Analog ground, should be tied together with BGND.

**Pin Configuration**
**Table 1 Pin Definition and Functions (cont'd)**

P-DSO P-SSOP Pin No.	P-LCC Pin No.	Name	I/O	Function
24	28	VTX	O	Transmit vf output. The AC voltage difference between TIPX and RINGX, the AC metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of one (or one half, see pin PTG). The two-wire impedance programming network connects between VTX and RSN.
-	4, 11, 19, 25	NC	—	Not Connected.

**Table 2 SLIC Operating States**

State	C3	C2	C1	SLIC Operating State	Active Detector (DET Response)
0	0	0	0	Open circuit	No active detector (DET is set high)
1	0	0	1	Ringling	Ring-trip detector (DET active low)
2	0	1	0	Active	Loop detector (DET active low)
3	0	1	1	Not applicable	—
4	1	0	0	Not applicable	—
5	1	0	1	Active	Ground key detector (DET active high)
6	1	1	0	Active reverse	Loop detector (DET active low)
7	1	1	1	Active reverse	Ground key detector (DET active high)

### 3 Electrical Characteristics

**Table 3 Absolute Maximum Ratings**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Temperature, Humidity						
Storage temperature range	$T_{\text{Stg}}$	-55	–	+150	°C	–
Operating temperature range	$T_{\text{Amb}}$	-40	–	+110	°C	–
Operating junction temperature range <sup>1)</sup>	$T_{\text{J}}$	-40	–	+140	°C	–
Power Supply ( $-40\text{ }^{\circ}\text{C} \leq T_{\text{Amb}} \leq +85\text{ }^{\circ}\text{C}$ )						
$V_{\text{CC}}$ with respect to A/BGND	$V_{\text{CC}}$	-0.4	–	6.5	V	–
$V_{\text{BAT2}}$ with respect to A/BGND	$V_{\text{BAT2}}$	$V_{\text{BAT}}$	–	0.4	V	–
$V_{\text{BAT}}$ with respect to A/BGND, continuous	$V_{\text{BAT}}$	-75	–	0.4	V	–
$V_{\text{BAT}}$ with respect to A/BGND, 10 ms	$V_{\text{BAT}}$	-80	–	0.4	V	–
Power Dissipation						
Continuous power dissipation	$P_{\text{D}}$	–	–	1.5	W	$T_{\text{Amb}} \leq +85\text{ }^{\circ}\text{C}$
Ground						
Voltage between AGND and BGND	$V_{\text{G}}$	-0.3	–	0.3	V	–
Relay Driver						
Ring relay supply voltage	–	–	–	BGN D+14	V	–
Ring Trip Comparator						
Input voltage	$V_{\text{DT}}, V_{\text{DR}}$	$V_{\text{BAT}}$	–	AGN D	V	–
Input current	$I_{\text{DT}}, I_{\text{DR}}$	-5	–	5	mA	–
Digital Inputs, Outputs (C1, C2, C3, DET)						
Input voltage	$V_{\text{ID}}$	-0.4	–	$V_{\text{CC}}$	V	–
Output voltage	$V_{\text{OD}}$	-0.4	–	$V_{\text{CC}}$	V	–

**Electrical Characteristics**
**Table 3 Absolute Maximum Ratings (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
TIPX and RINGX Terminals ( $-40\text{ }^{\circ}\text{C} \leq T_{\text{Amb}} \leq +85\text{ }^{\circ}\text{C}$ , $V_{\text{BAT}} = -50\text{ V}$ )						
TIPX or RINGX current	$I_{\text{TIPX}}$ , $I_{\text{RINGX}}$	-100	–	100	mA	–
TIPX or RINGX voltage, continuous (referenced to AGND) <sup>2)</sup>	$V_{\text{TA}}$ , $V_{\text{RA}}$	-80	–	2	V	–
TIPX or RINGX <sup>2)</sup>	$V_{\text{TA}}$ , $V_{\text{RA}}$	$V_{\text{BAT}}$ - 10	–	5	V	pulse < 10 ms, $t_{\text{Rep}} > 10\text{ s}$
TIPX or RINGX <sup>2)</sup>	$V_{\text{TA}}$ , $V_{\text{RA}}$	$V_{\text{BAT}}$ - 25	–	10	V	pulse < 1 $\mu\text{s}$ , $t_{\text{Rep}} > 10\text{ s}$
TIP or RING <sup>2)3)</sup>	$V_{\text{TA}}$ , $V_{\text{RA}}$	$V_{\text{BAT}}$ - 35	–	15	V	pulse < 250 ns, $t_{\text{Rep}} > 10\text{ s}$

1) The circuit includes thermal protection. Operation above max. junction temperature may degrade device reliability.

2) With the diodes  $D_{\text{VB}}$  and  $D_{\text{VB2}}$  included, see [Figure 8](#).

3)  $R_{\text{F1}}$  and  $R_{\text{F2}} > 20\text{ }\Omega$  is also required. Pulse is supplied to RING and TIP outside  $R_{\text{F1}}$  and  $R_{\text{F2}}$ .

**Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

**Table 4 Operating Range**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Ambient temperature	$T_{\text{Amb}}$	-40	–	+85	$^{\circ}\text{C}$	–
$V_{\text{CC}}$ with respect to AGND	$V_{\text{CC}}$	4.75	–	5.25	V	–
$V_{\text{BAT}}$ with respect to AGND	$V_{\text{BAT}}$	-58	–	-8	V	–
AGND with respect to BGND	$V_{\text{G}}$	-100	–	100	mV	–



**Electrical Characteristics**
**3.1 Characteristics**

The specification is made with following setup:  $-40\text{ }^{\circ}\text{C} \leq T_{\text{Amb}} \leq +85\text{ }^{\circ}\text{C}$ , PTG = open (see pin description),  $V_{\text{CC}} = +5\text{ V} \pm 5\%$ ,  $V_{\text{BAT}} = -58\text{ V}$  to  $-40\text{ V}$ ,  $V_{\text{BAT2}} = -17\text{ V}$ ,  $R_{\text{LC}} = 38.3\text{ k}\Omega$ ,  $I_{\text{L}} = 22\text{ mA}$ ,  $R_{\text{L}} = 600\text{ }\Omega$ ,  $R_{\text{F1}} = R_{\text{F2}} = 0$ ,  $R_{\text{REF}} = 49.9\text{ k}\Omega$ ,  $C_{\text{HP}} = 47\text{ nF}$ ,  $C_{\text{LP}} = 0.15\text{ }\mu\text{F}$ ,  $R_{\text{T}} = 120\text{ k}\Omega$ ,  $R_{\text{SG}} = 0\text{ k}\Omega$ ,  $R_{\text{RX}} = 60\text{ k}\Omega$ ,  $R_{\text{R}} = 52.3\text{ k}\Omega$ ,  $R_{\text{OV}} = \text{infinite}$ .

Current definition: current is positive if flowing into a pin unless stated otherwise.

**Table 5 Characteristics**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Two-Wire Port						
Overhead level <sup>1)</sup> , Active, 1% THD $R_{\text{OV}}$ = infinite see <b>Figure 3</b>	$V_{\text{TRO}}$	1.0	—	—	$V_{\text{Peak}}$	—
		1.0	—	—	$V_{\text{Peak}}$	On-Hook, $I_{\text{LDC}} \leq 5 \text{ mA}$
Input impedance <sup>2)</sup>	$Z_{\text{TRX}}$	—	$Z_{\text{T}}/200$	—	$\Omega$	—
Longitudinal impedance	$Z_{\text{LOT}}, Z_{\text{LOR}}$	—	20	35	$\Omega/\text{wire}$	$0 < f < 100 \text{ Hz}$
Longitudinal current limit	$I_{\text{LOT}}, I_{\text{LOR}}$	10	—	—	$\text{mA}_{\text{rms}}/\text{wire}$	Active
Longitudinal to metallic balance (IEEE standard 455-1984)	$B_{\text{LM}}$	53	—	—	dB	$0.2 \text{ kHz} \leq f \leq 1.0 \text{ kHz}$
		53	—	—	dB	$1.0 \text{ kHz} < f < 3.4 \text{ kHz}$
		53	—	—	dB	Reverse polarity $0.2 \text{ kHz} < f < 3.4 \text{ kHz}$
Longitudinal to metallic balance $B_{\text{LME}} = 20 \times \log E_{\text{LO}}/V_{\text{TR}} $ , see <b>Figure 4</b>	$B_{\text{LME}}$	53	75	—	dB	$0.2 \text{ kHz} \leq f \leq 1.0 \text{ kHz}$
		53	70	—	dB	$1.0 \text{ kHz} < f < 3.4 \text{ kHz}$
		53	68	—	dB	Reverse polarity $0.2 \text{ kHz} < f < 3.4 \text{ kHz}$

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Longitudinal to four-wire balance $B_{LFE} = 20 \times \log E_{LO}/V_{TX} $ , see <a href="#">Figure 4</a>	$B_{LFE}$	53	75	–	dB	$0.2 \text{ kHz} \leq f \leq 1.0 \text{ kHz}$
		53	70	–	dB	$1.0 \text{ kHz} < f < 3.4 \text{ kHz}$
		53	68	–	dB	Reverse polarity $0.2 \text{ kHz} < f < 3.4 \text{ kHz}$
Metallic to longitudinal balance $B_{MLE} = 20 \times \log V_{TR}/V_{LO} $ , $E_{RX} = 0 \text{ V}$ , see <a href="#">Figure 5</a>	$B_{MLE}$	40	50	–	dB	$0.2 \text{ kHz} < f < 3.4 \text{ kHz}$
Four-wire to longitudinal balance $B_{FLE} = 20 \times \log E_{RX}/V_{LO} $ , see <a href="#">Figure 5</a>	$B_{FLE}$	40	50	–	dB	$0.2 \text{ kHz} < f < 3.4 \text{ kHz}$
Two-wire return loss <sup>3)</sup> $r = 20 \times \log \left  \frac{Z_{TRX} + Z_L}{Z_{TRX} - Z_L} \right $	$r$	27	35	–	dB	$0.2 \text{ kHz} < f < 1.0 \text{ kHz}$
		20	22	–	dB	$1.0 \text{ kHz} < f < 3.4 \text{ kHz}$
TIPX idle voltage	$V_{TI}$	–	-1.1	–	V	Active, $I_L = 0 \text{ mA}$
RINGX idle voltage	$V_{RI}$	–	$V_{BAT} + 2.5$	–	V	Active, $I_L = 0 \text{ mA}$
Open loop voltage	$V_{TR}$	–	$V_{BAT} + 3.6$	–	V	Active, $I_L = 0 \text{ mA}$
<b>Four-Wire Transmit Port (VTX)</b>						
Overhead level <sup>4)</sup> , Load imp. > 20 kΩ 1% THD see <a href="#">Figure 6</a>	$V_{TXO}$	1.0	–	–	$V_{Peak}$	–
		1.0	–	–	$V_{Peak}$	On-Hook, $I_L \leq 5 \text{ mA}$
Output offset voltage	$\Delta V_{TX}$	-100	–	100	mV	–

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Output impedance	$Z_{TX}$	–	15	50	$\Omega$	$0.2 \text{ kHz} < f < 3.4 \text{ kHz}$

**Four-Wire Receive Port (receive summing node = RSN)**

RSN DC voltage	$V_{RSNdc}$	1.15	1.25	1.35	V	$I_{RSN} = -55 \mu\text{A}$
RSN impedance		–	8	20	$\Omega$	$0.2 \text{ kHz} < f < 3.4 \text{ kHz}$
RSN current ( $I_{RSN}$ ) to metallic loop current ( $I_L$ ) gain	$\alpha_{RSN}$	–	200	–	ratio	$0.3 \text{ kHz} < f < 3.4 \text{ kHz}$

**Frequency Response**

Two-wire to four-wire, relative to 0 dBm, 1.0 kHz, $E_{RX} = 0 \text{ V}$ , see <a href="#">Figure 7</a>	$g_{2-4}$	-0.20	–	0.10	dB	$0.3 \text{ kHz} < f < 3.4 \text{ kHz}$
		-1.0	–	0.1	dB	$f = 8 \text{ kHz}, 12 \text{ kHz}, 16 \text{ kHz}$
Four-wire to two-wire, relative to 0 dBm, 1.0 kHz, $E_L = 0 \text{ V}$ , see <a href="#">Figure 7</a>	$g_{4-2}$	-0.2	–	0.1	dB	$0.3 \text{ kHz} < f < 3.4 \text{ kHz}$
		-1.0	–	0	dB	$f = 8 \text{ kHz}, 12 \text{ kHz}$
		-2.0	–	0	dB	$f = 16 \text{ kHz}$
Four-wire to four-wire, relative to 0 dBm, 1.0 kHz, $E_L = 0 \text{ V}$ , see <a href="#">Figure 7</a>	$g_{4-4}$	-0.2	–	0.1	dB	$0.3 \text{ kHz} < f < 3.4 \text{ kHz}$

**Insertion Loss**

Two-wire to four-wire <sup>5)</sup> , $G_{2-4} = 20 \times \log V_{TX}/V_{TR} $ , 0 dBm, 1.0 kHz	$G_{2-4}$	-0.2	–	0.2	dB	$E_{RX} = 0 \text{ V}$ , PTG = Open see <a href="#">Figure 7</a>
		-6.22	-6.02	-5.82	dB	PTG = AGND
Four-wire to two-wire <sup>6)</sup> , $G_{4-2} = 20 \times \log V_{TR}/E_{RX} $ , $E_L = 0 \text{ V}$ , see <a href="#">Figure 7</a>	$G_{4-2}$	-0.2	–	0.2	dB	0 dBm, 1.0 kHz

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gain Tracking						
Two-wire to four-wire <sup>7)</sup> , Ref. -10 dBm, 1.0 kHz, see <a href="#">Figure 7</a>		-0.1	–	0.1	dB	-40 dBm to +0 dBm
		-0.2	–	0.2	dB	-55 dBm to -40 dBm
Four-wire to two-wire, Ref. -10 dBm, 1.0 kHz, see <a href="#">Figure 7</a>		-0.1	–	0.1	dB	-40 dBm to +0 dBm
		-0.2	–	0.2	dB	-55 dBm to -40 dBm
Noise						
Idle channel noise at two-wire port <sup>8)</sup> (TIPX-RINGX) or four- wire (VTX) output		–	–	12	dBmC	C-message weighting
		–	–	-78	dBmp	Psophometrical weighting
Harmonic Distortion						
Two-wire to four-wire, see <a href="#">Figure 7</a>		–	-67	-50	dB	0 dBm
Four-wire to two-wire		–	-67	-50	dB	0.3 kHz < f < 3.4 kHz
Battery Feed Characteristics						
Constant loop current, R <sub>LC</sub> in kΩ see <a href="#">Figure 12</a>	I <sub>LProg</sub>	0.92 × I <sub>LProg</sub>	I <sub>LProg</sub>	1.08 × I <sub>LProg</sub>	mA	$I_{LProg} = \frac{1000}{R_{LC}} - 4, 0$
	I <sub>LProg</sub> @ 30 mA	0.95 × I <sub>LProg</sub>	I <sub>LProg</sub>	1.05 × I <sub>LProg</sub>	mA	$I_{LProg} = \frac{1000}{R_{LC}} - 4, 2$
	I <sub>LProg</sub> @ 18 mA	0.94 × I <sub>LProg</sub>	I <sub>LProg</sub>	1.06 × I <sub>LProg</sub>	mA	$I_{LProg} = \frac{1000}{R_{LC}} - 3, 9$
Open circuit loop current	I <sub>LOC</sub>	-100	0	100	μA	R <sub>L</sub> = 0 Ω
Loop Detector						

**Electrical Characteristics**
**Table 5**      **Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Programmable threshold, $I_{LTh} = 500/R_{LD}$	$I_{LTh}$	$0.85 \times I_{LTh}$	$I_{LTh}$	$1.15 \times I_{LTh}$	mA	$R_{LD}$ in k $\Omega$ , $7 \text{ mA} \leq I_{LTh}$
<b>Ground Key Detector</b>						
Ground key detector threshold		10	16	22	mA	$I_{TIPX}$ and $I_{RINGX}$ difference to trigger ground key detector.
<b>Ring Trip Comparator</b>						
Offset voltage	$\Delta V_{DTDR}$	-20	0	20	mV	Source resistance, $R_S = 0 \Omega$
Input bias current	$I_B$	-200	-20	200	nA	$I_B = (I_{DT} + I_{DR})/2$
Input common mode range	$V_{DT}, V_{DR}$	$V_{BAT} + 1$	—	-1	V	—
<b>Ring Relay Driver</b>						
Saturation voltage	$V_{OL}$	—	0.2	0.5	V	$I_{OL} = 50 \text{ mA}$
Off state leakage current	$I_{LK}$	—	—	10	$\mu\text{A}$	$V_{OH} = 12 \text{ V}$
<b>Digital Inputs (C1, C2, C3)</b>						
Input low voltage	$V_{IL}$	0	—	0.5	V	—
Input high voltage	$V_{IH}$	2.5	—	$V_{CC}$	V	—
Input low current	$I_{IL}$	—	—	-50	$\mu\text{A}$	$V_{IL} = 0.5 \text{ V}$
Input high current	$I_{IH}$	—	—	50	$\mu\text{A}$	$V_{IH} = 2.5 \text{ V}$

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Detector Output (DET)						
Output low voltage	$V_{OL}$	—	—	0.7	V	$I_{OL} = 0.5 \text{ mA}$
Internal pull-up resistor to $V_{CC}$		—	15	—	k $\Omega$	—
Power Dissipation ( $V_{BAT} = -48 \text{ V}$ , $V_{BAT2} = -17 \text{ V}$ )						
Power Dissipation	$P_1$	—	10	15	mW	Open circuit
Power Dissipation	$P_2$	—	60	80	mW	Active (On-hook) Long current = 0 mA
Power Dissipation	$P_3$	—	290	—	mW	Active (Off-hook) $R_L = 300 \Omega$
Power Dissipation	$P_4$	—	145	—	mW	Active (Off-hook) $R_L = 500 \Omega$
Power Supply Currents ( $V_{BAT} = -48 \text{ V}$ )						
$V_{CC}$ current	$I_{CC}$	—	1.2	2.0	mA	Open circuit
$V_{BAT}$ current	$I_{BAT}$	-0.1	-0.05	—	mA	Open circuit
$V_{CC}$ current	$I_{CC}$	—	2.8	4.0	mA	Active, On-hook, Long current = 0 mA
$V_{BAT}$ current	$I_{BAT}$	-1.5	-1.0	—	mA	Active, On-hook, Long current = 0 mA
Power Supply Rejection Ratios						
$V_{CC}$ to 2- or 4-wire port		30	42	—	dB	Active, $f = 1 \text{ kHz}$ , $V_n = 100 \text{ mV}$
$V_{BAT2}$ to 2- or 4-wire port		40	60	—	dB	Active, $f = 1 \text{ kHz}$ , $V_n = 100 \text{ mV}$
$V_{BAT}$ to 2- or 4-wire port		36	45	—	dB	Active, $f = 1 \text{ kHz}$ , $V_n = 100 \text{ mV}$

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

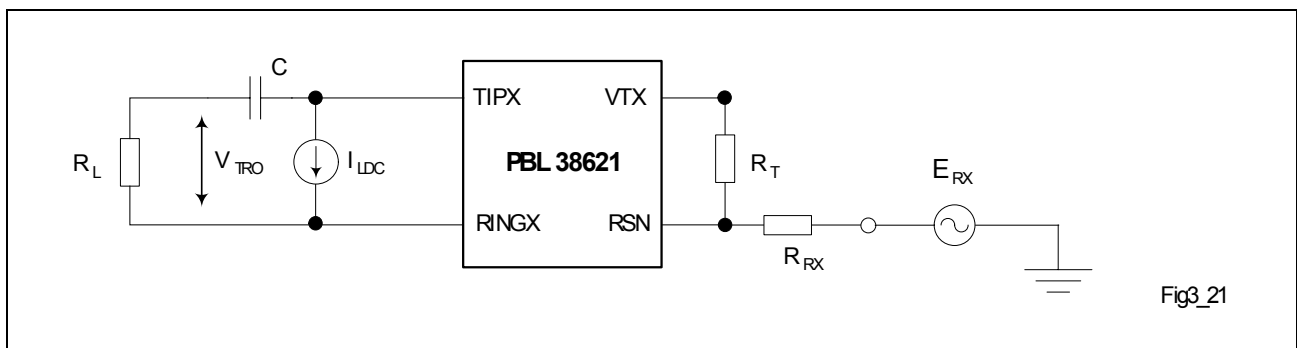
Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Temperature Guard						
Junction threshold temperature	$T_{JG}$	—	145	—	°C	—
Thermal Resistance						
24-pin SSOP	$\Theta_{JP24SSOP}$	—	55	—	°C/W	—
	$R_{th, jA}$	—	66.9	—	°C/W	P-SSOP-24-1, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber
24-pin SOIC	$\Theta_{JP24SOIC}$	—	43	—	°C/W	—
	$R_{th, jA}$	—	80.2	—	°C/W	P-DSO-24-1-3, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber
28-pin PLCC	$\Theta_{JP28PLCC}$	—	39	—	°C/W	—
	$R_{th, jA}$	—	50.4	—	°C/W	P-LCC-28-2, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber

1) The overhead level can be adjusted with the resistor  $R_{OV}$  for higher levels, for example min 3.1  $V_{Peak}$ , and is specified at the two-wire port with the signal source at the four-wire receive port.



## Electrical Characteristics

- 2) The two-wire impedance is programmable by selection of external component values according to:  
 $Z_{TRX} = Z_T / (|G_{2-4S} \times \alpha_{RSN}|)$  where:  
 $Z_{TRX}$  = impedance between the TIPX and RINGX terminals  
 $Z_T$  = programming network between the VTX and RSN terminals  
 $G_{2-4S}$  = transmit gain, nominally = 1 (or 0.5, see pin PTG)  
 $\alpha_{RSN}$  = receive current gain, nominally 200 (current defined as positive flowing into the receive summing node, RSN, and when flowing from ring to tip).
- 3) Higher return loss values can be achieved by adding a reactive component to  $R_T$ , the two-wire terminating impedance programming resistance, for example by dividing  $R_T$  into two equal halves and connecting a capacitor from the common point to ground.
- 4) The overhead level can be adjusted with the resistor  $R_{OV}$  for higher levels, for example min 3.1 V<sub>Peak</sub>, and is specified at the four-wire transmit port, (VTX) with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is  $G_{2-4S} = 1$  (or 0.5, see pin PTG).
- 5) Pin PTG = Open sets transmit gain to nom. 0.0 dB.  
 Pin PTG = AGND sets transmit gain to nom. -6.02 dB  
 Secondary resistor  $R_F$  impact the insertion loss as explained in the text, [Chapter 5](#). The specified insertion loss is for  $R_F = 0$ .
- 6) The specified insertion loss tolerance does not include errors caused by external components.
- 7) The level is specified at the two-wire port.
- 8) The two-wire idle noise is specified with the port terminated in 600  $\Omega$  ( $R_L$ ), and with the four-wire receive port grounded ( $E_{RX} = 0$ ; see [Figure 7](#)). The four-wire idle noise at  $V_{TX}$  is specified with the two-wire port terminated in 600  $\Omega$  ( $R_L$ ). The noise specification is referenced to a 600  $\Omega$  two-wire impedance level at  $V_{TX}$ . The four-wire receive port is grounded ( $E_{RX} = 0$ ).



**Figure 3 Overhead Level,  $V_{TRO}$ , Two-Wire Port**

$$1/\omega C \ll R_L, R_L = 600 \, \Omega, R_T = 120 \, k\Omega, R_{RX} = 60 \, k\Omega$$

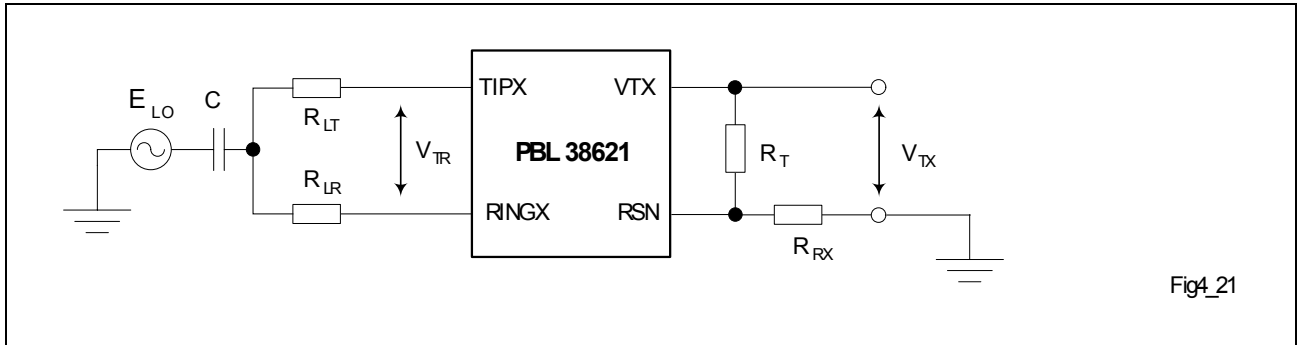


Fig4\_21

**Figure 4 Longit. to Metallic,  $B_{LME}$  and Longit. to Four-Wire,  $B_{LFE}$  Balance**

$1/\omega C \ll 150 \Omega$ ,  $R_{LT} = R_{LR} = R_L / 2 = 300 \Omega$ ,  $R_T = 120 \text{ k}\Omega$ ,  $R_{RX} = 60 \text{ k}\Omega$

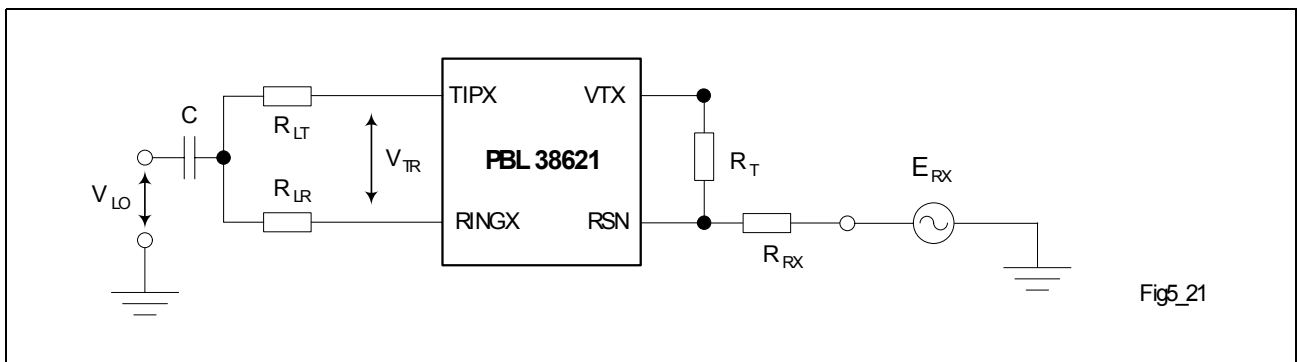


Fig5\_21

**Figure 5 Metallic to Longit.,  $B_{MLE}$  and Four-Wire to Longit. Balance,  $B_{FLE}$**

$1/\omega C \ll 150 \Omega$ ,  $R_{LT} = R_{LR} = R_L / 2 = 300 \Omega$ ,  $R_T = 120 \text{ k}\Omega$ ,  $R_{RX} = 60 \text{ k}\Omega$

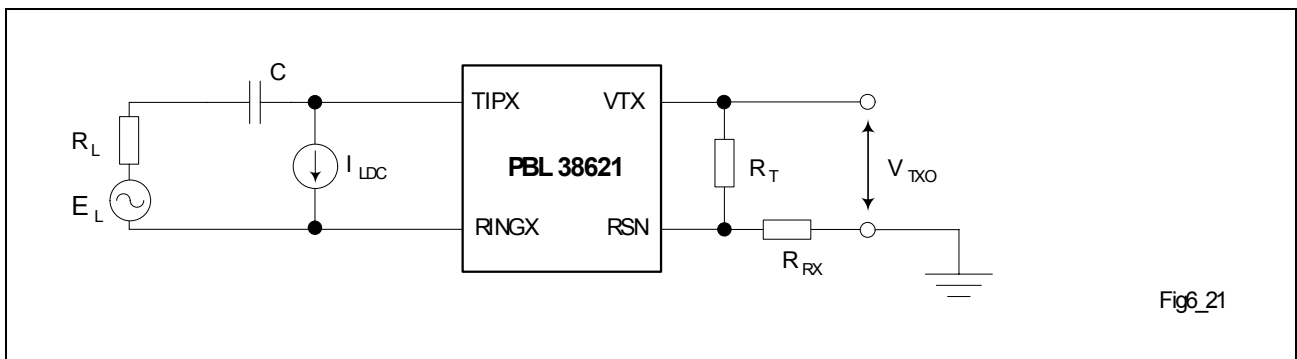
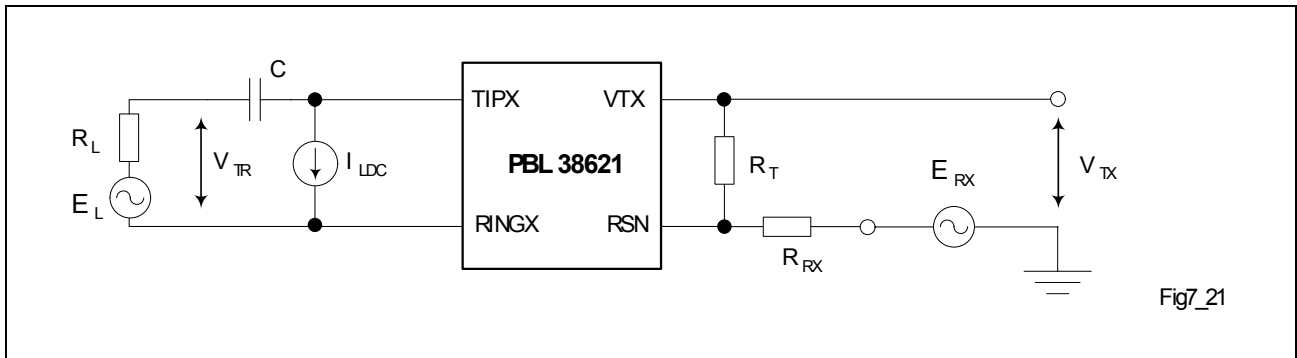


Fig6\_21

**Figure 6 Overhead Level,  $V_{TXO}$ , Four-Wire Transmit Port**

$1/\omega C \ll R_L$ ,  $R_L = 600 \Omega$ ,  $R_T = 120 \text{ k}\Omega$ ,  $R_{RX} = 60 \text{ k}\Omega$



**Figure 7 Frequency Response, Insertion Loss, Gain Tracking**

$1/\omega C \ll R_L$ ,  $R_L = 600 \, \Omega$ ,  $R_T = 120 \, k\Omega$ ,  $R_{RX} = 60 \, k\Omega$

## 4 Application Schematic

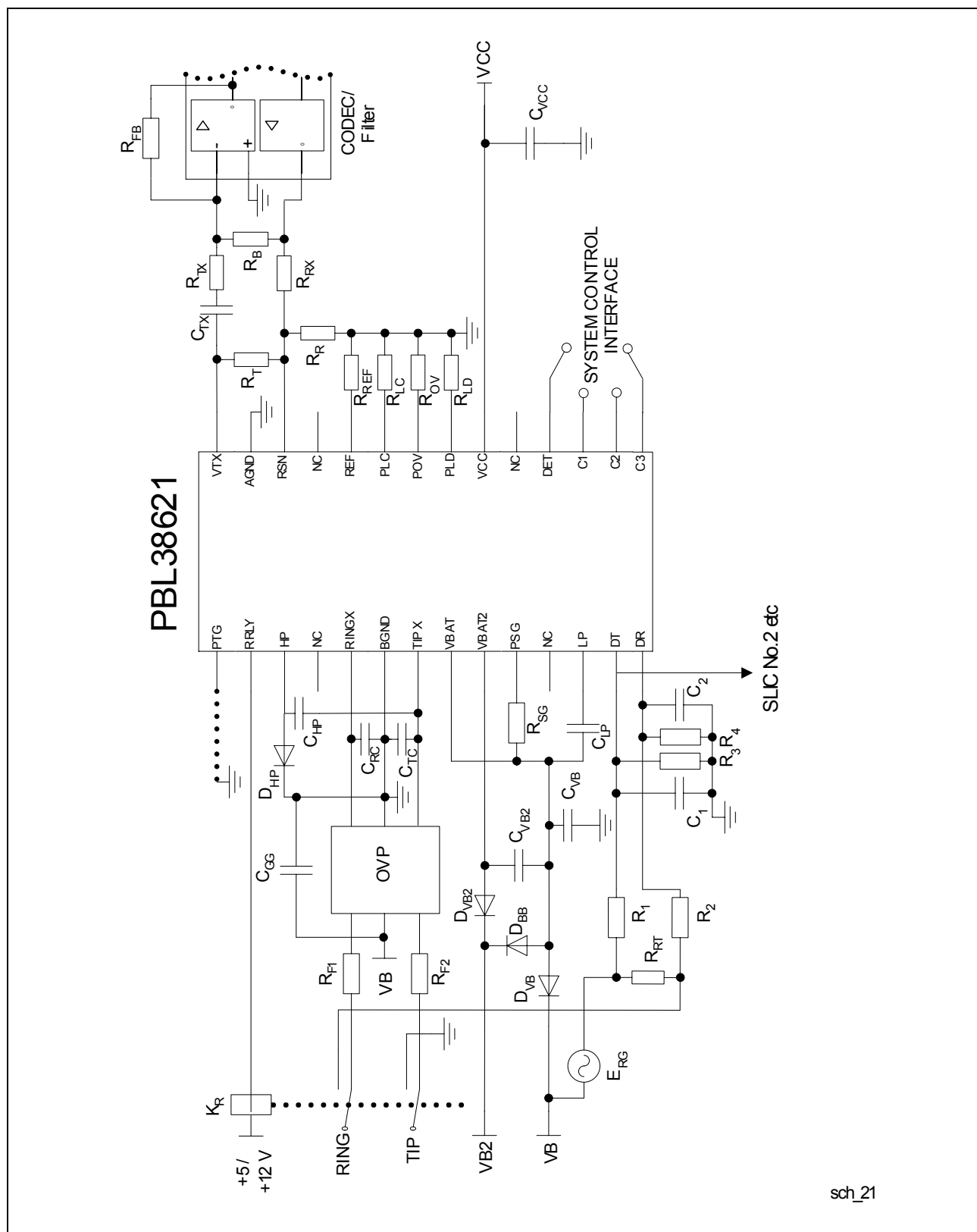


Figure 8 Application Example of PBL 38621/2 with CODEC/filter

## 4.1 Recommended Components

**Table 6**      **Resistors** (values according to IEC E96 series)

Resistor	Value	Tolerance	Specification
$R_{SG}$	0 $\Omega$	1%	1/10 W
$R_{LD}$	49.9 k $\Omega$	1%	1/10 W
$R_{OV}$	User programmable	—	—
$R_{LC}$	38.3 k $\Omega$	1%	1/10 W
$R_{REF}$	49.9 k $\Omega$	1%	1/10 W
$R_R$	64.9 k $\Omega$	1%	1/10 W
$R_T$	105 k $\Omega$	1%	1/10 W
$R_{RX}$	52.3 k $\Omega$	1%	1/10 W
$R_{TX}$	24.9 k $\Omega$	1%	1/10 W
$R_B$	22.1 k $\Omega$	1%	1/10 W
$R_{FB}$	depending on codec	—	—
$R_1$	604 k $\Omega$	1%	1/10 W
$R_2$	604 k $\Omega$	1%	1/10 W
$R_3$	249 k $\Omega$	1%	1/10 W
$R_4$	280 k $\Omega$	1%	1/10 W
$R_{RT}$	330 $\Omega$	5%	2 W
$R_{F1}, R_{F2}$	Line resistor, 40 $\Omega$	1%	—

**Table 7**      **Capacitors** (values according to IEC E96 series)

Capacitor	Value	Tolerance	Specification
$C_{VB}$	100 nF	10%	100 V
$C_{VB2}$	150 nF	10%	100 V
$C_{TC}$	2.2 nF	10%	100 V
$C_{RC}$	2.2 nF	10%	100 V
$C_{HP}$	47 nF	10%	100 V
$C_{VCC}$	100 nF	10%	10 V
$C_{LP}$	150 nF	10%	100 V
$C_{TX}$	100 nF	10%	10 V

**Table 7      Capacitors** (values according to IEC E96 series) (cont'd)

$C_{GG}$	220 nF	10%	100 V
$C_1$	330 nF	10%	63 V
$C_2$	330 nF	10%	63 V

**Table 8      Diodes**

Diode	Value	Tolerance	Specification
$D_{VB}$	1N4448		
$D_{VB2}$	1N4448		
$D_{BB}$	1N4448		
$D_{HP}$	1N4448 <sup>1)</sup>		

1) It is required to connect  $D_{HP}$  between terminals HP and ground if  $C_{HP} > 47$  nF

## OVP

Secondary protection (Bournes TISP PBL2). The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferably to a ground plane.

## 4.2 Design Supporting Tools

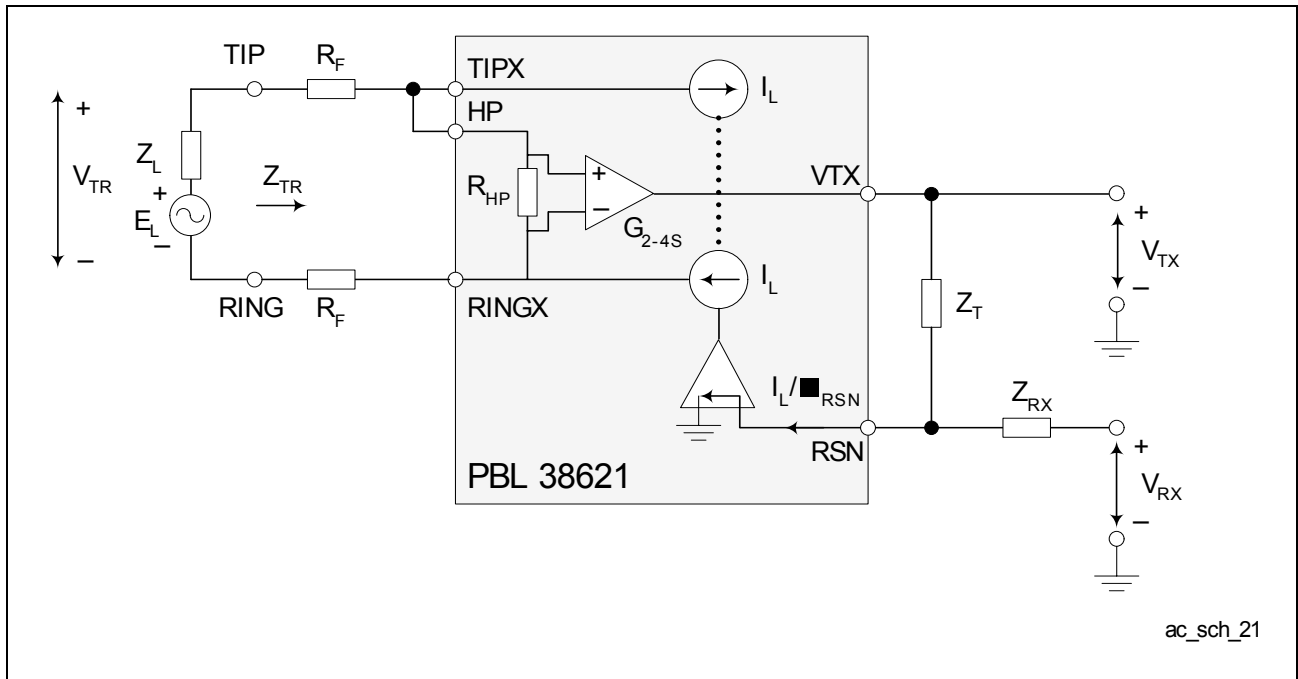
The following supporting tools are available for the PBL 38621/2:

- Test board TB 208 for PLCC package
- Test board TB 208SSOP for SSOP package
- Pspice model for PBL 38621/2

## 5 Transmission

### 5.1 General

A simplified AC model of the transmission circuit is shown in [Figure 9](#).



**Figure 9** Simplified AC Model of PBL 38621/2

Circuit analysis from the AC model in [Figure 9](#) yields following equations:

$$V_{TR} = \frac{V_{TX}}{G_{2-4S}} + I_L \times 2R_F \quad [1]$$

$$\frac{I_L}{\alpha_{RSN}} = \frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} \quad [2]$$

$$V_{TR} = E_L - I_L \times Z_L \quad [3]$$



where:

$V_{TX}$	Is the ground referenced version of the AC metallic voltage between the TIPX and RINGX terminals.
$V_{TR}$	Is the AC metallic voltage between TIP and RING.
$E_L$	Is the line open circuit AC metallic voltage.
$I_L$	Is the AC metallic current.
$R_F$	Is a fuse resistor.
$G_{2-4S}$	Is the programmable SLIC two-wire to four-wire gain (transmit direction) <sup>1)</sup> .
$Z_L$	Is the line impedance.
$Z_{RX}$	Controls four- to two-wire gain.
$Z_T$	Determines the SLIC TIPX to RINGX impedance at voice frequencies.
$V_{RX}$	Is the analog ground referenced receive signal.
$\alpha_{RSN}$	Is the receive summing node current to metallic loop current gain. $\alpha_{RSN} = 200$

1) The SLIC two-wire to four-wire gain,  $G_{2-4S}$ , is user programmable between two fixe values. See Table 5.

## 5.2 Two-Wire Impedance

To calculate  $Z_{TR}$ , the impedance presented to the two-wire line by the SLIC including the fuse resistor  $R_F$ , let  $V_{RX} = 0$ .

From [Equation \[1\]](#) and [Equation \[2\]](#):

$$Z_{TR} = \frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F \quad [4]$$

Thus with  $Z_{TR}$ ,  $G_{2-4S}$ ,  $\alpha_{RSN}$  and  $R_F$  known:

$$Z_T = \alpha_{RSN} \times G_{2-4S} \times (Z_{TR} - 2R_F) \quad [5]$$

## 5.3 Two-Wire to Four-Wire Gain

From [Equation \[1\]](#) and [Equation \[2\]](#) with  $V_{RX} = 0$ :

$$G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T / \alpha_{RSN}}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F} \quad [6]$$

## 5.4 Four-Wire to Two-Wire Gain

From [Equation \[1\]](#) to [Equation \[3\]](#) with  $E_L = 0$ :

$$G_{4-2} = \frac{V_{TR}}{V_{RX}} = - \frac{Z_T}{Z_{RX}} \times \frac{1}{G_{2-4S}} \times \frac{Z_L}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_F} \quad [7]$$

For applications where

$$\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F = Z_L \quad [8]$$

the expression for  $G_{4-2}$  simplifies to:

$$G_{4-2} = - \frac{Z_T}{Z_{RX}} \times \frac{1}{2 \times G_{2-4S}} \quad [9]$$

## 5.5 Four-Wire to Four-Wire Gain

From [Equation \[1\]](#) to [Equation \[3\]](#) with  $E_L = 0$ :

$$G_{4-4} = \frac{V_{TX}}{V_{RX}} = - \frac{Z_T}{Z_{RX}} \times \frac{Z_L + 2R_F}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_F} \quad [10]$$

## 5.6 Hybrid Function

The hybrid function can easily be implemented utilizing the uncommitted amplifier in conventional non software programmable codec/filters. Please, refer to [Figure 10](#). Via impedance  $Z_B$  a current proportional to  $V_{RX}$  is injected into the summing node of the combination codec/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain,  $G_{4-4}$ , a voltage proportional to  $V_{RX}$  is returned to  $V_{TX}$ . This voltage is converted by  $R_{TX}$  to a current flowing into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \quad (E_L = 0) \quad [11]$$

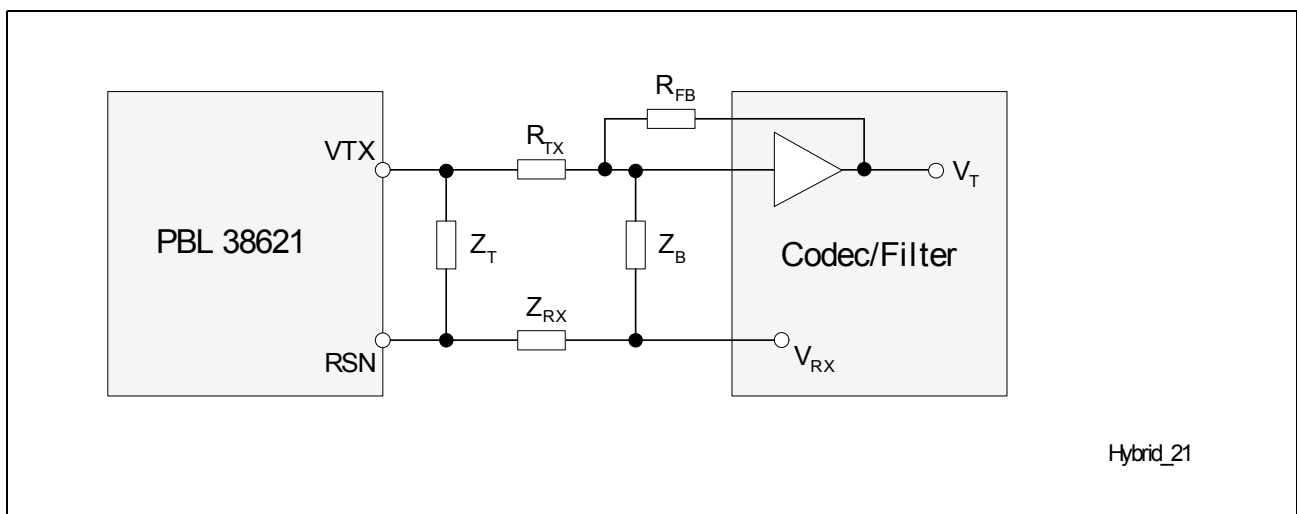
The four-wire to four-wire gain,  $G_{4-4}$ , includes the required phase shift and thus the balance network  $Z_B$  can be calculated from:

$$Z_B = -R_{TX} \times \frac{V_{RX}}{V_{TX}} = R_{TX} \times \frac{Z_{RX}}{Z_T} \times \frac{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_F}{Z_L + 2R_F} \quad [12]$$

When selecting the  $R_{TX}$  resistance value, make sure the load resistance on the  $V_{TX}$  terminal is at least 20 k $\Omega$ .

If calculation of the  $Z_B$  formula above yields a balance network containing an inductor, an alternate method is recommended.

The PBL 38621/2 SLIC may also be used together with programmable CODEC/filters. The programmable CODEC/filter allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the transmit and receive gain may be adjusted. Please, refer to the programmable CODEC/filter data sheets for design information.



**Figure 10 Hybrid Function**

## 5.7 Longitudinal Impedance

A feedback loop within the SLIC counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range.

The SLIC longitudinal impedance per wire,  $Z_{LOT}$  and  $Z_{LOR}$ , appears as typically  $20\ \Omega$  to longitudinal disturbances. It should be noted that longitudinal currents may exceed the DC loop current without disturbing the VF transmission.

## 5.8 Capacitors $C_{TC}$ and $C_{RC}$

The capacitors designated  $C_{TC}$  and  $C_{RC}$  in [Figure 8](#), connected between TIPX and ground as well as between RINGX and ground, can be used for RFI filtering. The recommended value for  $C_{TC}$  and  $C_{RC}$  is 2200 pF. Higher capacitance values may be used, but care must be taken to prevent degradation of either longitudinal balance or return loss.  $C_{TC}$  and  $C_{RC}$  contribute to a metallic impedance of  $1/(\pi \times f \times C_{TC}) = 1/(\pi \times f \times C_{RC})$ , a TIPX to ground impedance of  $1/(2\pi \times f \times C_{TC})$  and a RINGX to ground impedance of  $1/(2\pi \times f \times C_{RC})$ .

## 5.9 AC - DC Separation Capacitor, $C_{HP}$

The high pass filter capacitor connected between terminals HP and TIPX provides the separation of the AC and DC signals, such that only AC signals are forwarded to the VTX terminal.  $C_{HP}$  positions the low end frequency response break point of the AC feedback loop in the SLIC. The  $C_{HP}$  value of 47 nF will position the low end frequency response 3 dB break point of the AC loop at 5.6 Hz ( $f_{3dB}$ ) according to  $f_{3dB} = 1/(2\pi \times R_{HP} \times C_{HP})$  where  $R_{HP} = 600\ k\Omega$ .

## 5.10 High-pass Transmit Filter

The capacitor  $C_{TX}$  in [Figure 8](#) connected between the VTX output and the CODEC/filter forms, together with  $R_{TX}$  and/or the input impedance of a programmable CODEC/filter, a high-pass RC filter. It is recommended to position the 3 dB break point of this filter between 30 and 80 Hz to get a faster response for the DC steps that may occur at DTMF signalling.

## 5.11 Capacitor $C_{LP}$

The capacitor  $C_{LP}$ , which connects between the terminals LP and VBAT, positions the high end frequency break point of the low pass filter in the DC feedback loop (battery feed controlling loop) of the SLIC.  $C_{LP}$  together with  $C_{HP}$  and  $Z_T$  (see [Chapter 5.2](#)) forms the total two-wire output impedance of the SLIC. The choice of these programmable

components have an influence on the power supply rejection ratio (PSRR) from VBAT to the two-wire side at sub audio frequencies. At these frequencies  $C_{LP}$  also influences the transversal to longitudinal balance in the SLIC. **Table 9** suggests a suitable value on  $C_{LP}$ . The typical value of the transversal to longitudinal balance at 200 Hz is given in the table below, for the chosen value on  $C_{LP}$ .

**Table 9      Feeding Setup**

Symbol	Value	Unit	Specification
$R_{Feed}$	2x25	$\Omega$	—
$R_{SG}$	0	k $\Omega$	—
$C_{LP}$	150	nF	—
T-L bal. @ 200 Hz	-46	dB	—
$C_{HP}$	47	nF	—

## 6 Battery Feed

The PBL 38621/2 SLIC emulate a battery characteristic with current limitation adjustable. The open loop voltage measured between the TIPX and RINGX terminals is tracking the battery voltage  $V_{BAT}$ . The signalling headroom, or overhead voltage  $V_{TRO}$ , is programmable with a resistor  $R_{OV}$  connected between terminal POV on the SLIC and ground. Please refer to [Chapter 6.2](#). The battery voltage overhead,  $V_{OH}$ , depends on the programmed signal overhead voltage  $V_{TRO}$ .  $V_{OH}$  defines the TIP and RING voltage at open loop conditions according to

$$V_{TR}(\text{at } I_L = 0 \text{ mA}) = |V_{BAT}| - V_{OH}$$

Refer to the table below for the typical value on  $V_{OH}$ .

**Table 10 Battery Overhead**

Symbol	Value (typ)	Unit	Specification
$V_{OH}$	$2.5 + V_{TRO}$	V	—

The current limit (reference A - C in [Figure 12](#)) is adjusted by connecting a resistor,  $R_{LC}$ , between terminal PLC and ground according to the equation:

where  $R_{LC}$  is in  $k\Omega$  for  $I_{LProg}$  in mA.

$$I_{LProg} = \frac{1000}{R_{LC}} - 4, 0 \quad [13]$$

A second lower battery voltage may be connected to the device at terminal VBAT2 to reduce short loop power dissipation.

The SLIC automatically switches between the two battery supply voltages without need for external control. The silent battery switching occurs when the line voltage passes the value

$$|VB2| - 40 \times I_L - V_{TRO} = 3.6$$

For correct functionality it is important to connect the terminal VBAT2 to the second power supply via the diode  $D_{VB2}$ , see [Figure 8](#). An optional diode  $D_{BB}$  connected between terminal VBAT and the VB2 power supply, see [Figure 8](#), will make sure that the SLIC continues to work on the second battery even if the first battery voltage disappears. If a second battery voltage is not used, VBAT2 is connected to VBAT on the SLIC and  $C_{VB2}$ ,  $D_{BB}$  and  $D_{VB2}$  are removed.

### 6.1 CODEC Receive Interface

The PBL 38621/2 SLIC has got a receive interface at the four- wire side which makes it possible to reduce the number of capacitors in the applications and to fit both single and dual battery feed CODECs. The RSN terminal, connecting to the CODEC receive output via the resistor  $R_{RX}$ , is DC biased with +1.25 V. This makes it possible to compensate for

currents floating due to DC voltage differences between RSN and the CODEC output without using any capacitors. This is done by connecting a resistor  $R_R$  between the RSN terminal and ground. With current directions defined as in [Figure 11](#), current summation gives:

$$-I_{RSN} = I_{RT} + I_{RRX} + I_{RR} = \frac{1,25}{R_T} + \frac{1,25 - V_{CODEC}}{R_{RX}} + \frac{1,25}{R_R} \quad [14]$$

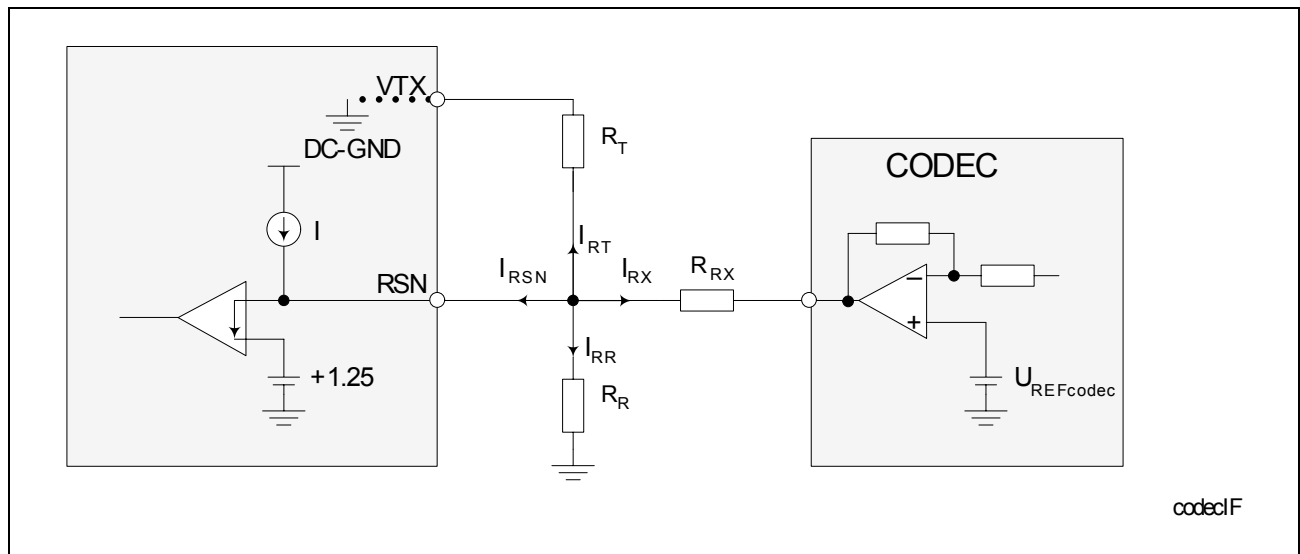
where  $V_{CODEC}$  is the reference voltage of the CODEC at the receive output. From this equation the resistor  $R_R$  can be calculated as

$$R_R = \frac{1,25}{-I_{RSN} - \frac{1,25}{R_T} - \frac{1,25 - V_{CODEC}}{R_{RX}}} \quad [15]$$

For the value on  $I_{RSN}$ , see table below. The resistor  $R_R$  has no influence in the AC transmission.

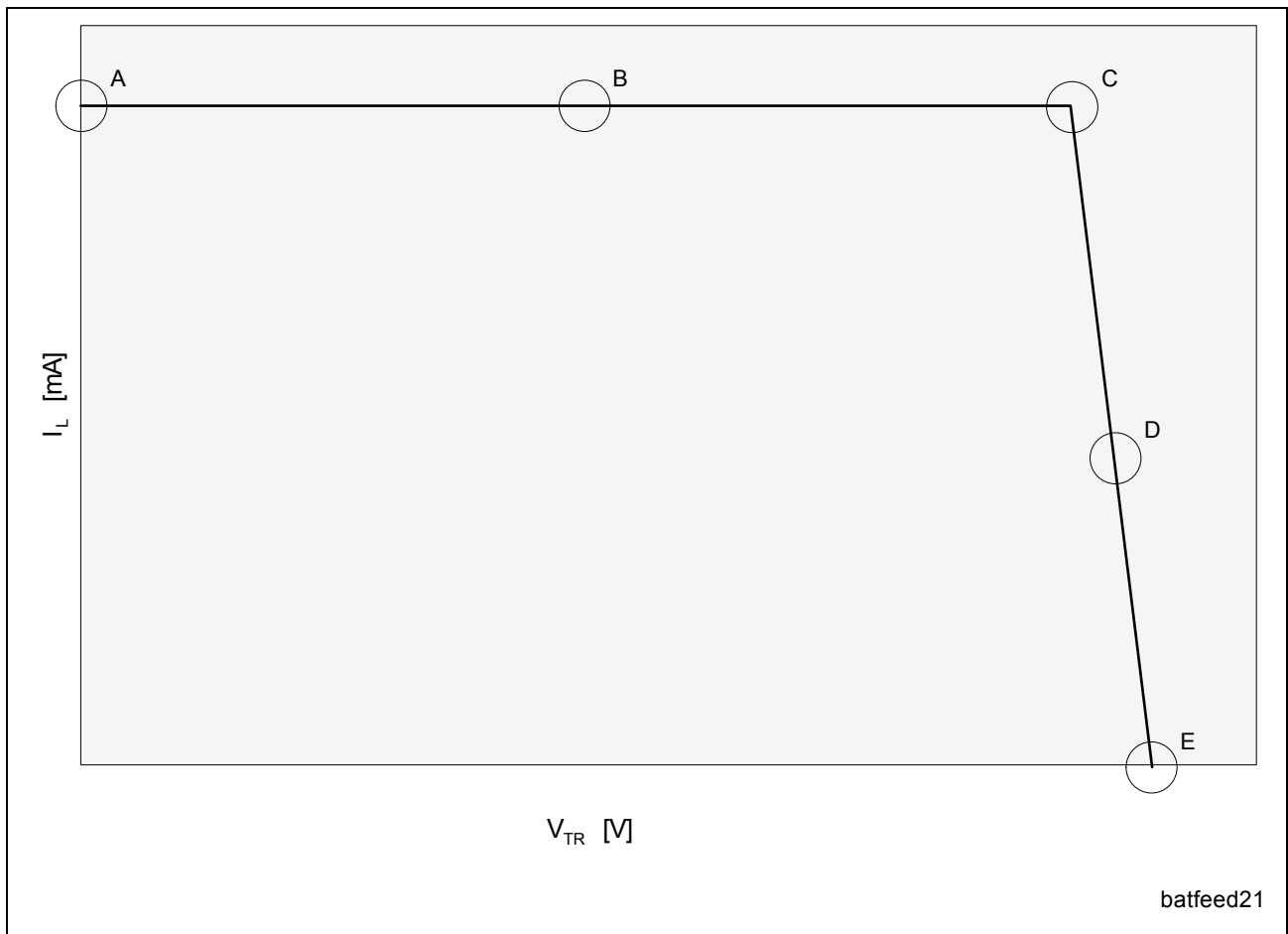
**Table 11 Internal bias current of RSN**

Symbol	Value (typ)	Unit
$I_{RSN}$	-55	$\mu A$



**Figure 11 Codec Receive Interface**





**Figure 12 Battery Feed Characteristics**

A	$I_L(@V_{TR} = 0) = I_{LProg}$
B	Constant current
C	$I_{LConst}(typ) = I_{LProg} = \frac{10^3}{R_{LC}} - 4 \times 10^{-3}$ $V_{TR} =  V_{BAT}  - V_{OH} - 50 \times I_{LProg}$
D	$R_{FEED} = 2 \times 25 \Omega$
E	$V_{TROpen} =  V_{BAT}  - V_{OH}$

## 6.2 Programmable Overhead Voltage (POV)

With the POV function the overhead voltage can be increased. If the POV pin is left open the overhead voltage is internally set to  $1.1 V_{Peak}$ . The overhead voltage is equal in on-hook and off-hook. If a resistor  $R_{OV}$  is connected between the POV pin and AGND, the overhead voltage can be set to higher values, typical values can be seen in [Figure 13](#). The  $R_{OV}$  and corresponding  $V_{TRO}$  (signal headroom) are typical values for THD < 1% and the signal frequency 1000 Hz.

Observe that the four-wire output terminal  $V_{TX}$  can not handle more than  $3.2 V_{Peak}$ . So if the two- to four-wire gain is 0 dB,  $3.2 V_{Peak}$  is maximum also for the two-wire side. Signal levels between  $3.2$  and  $6.4 V_{Peak}$  on the two-wire side can be handled with the PTG shorted so that the gain  $G_{2-4S}$  becomes -6.02 dB. Please note that:

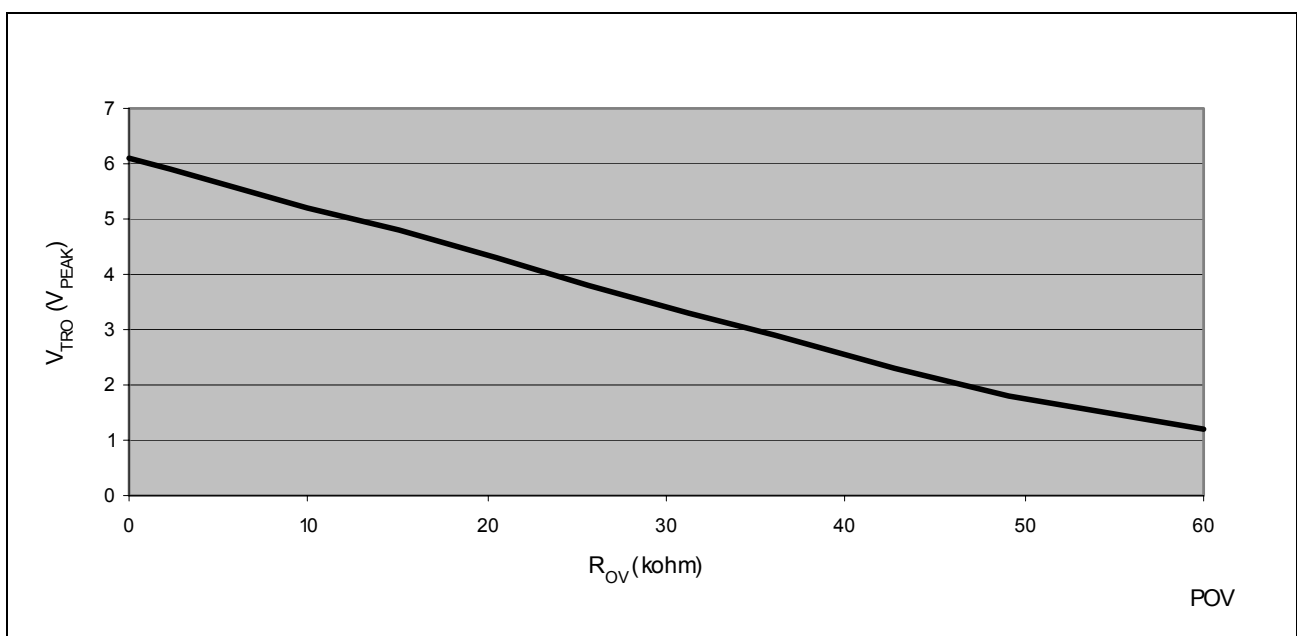
- $Z_T$
- $R_R$
- $G_{4-4}$

has to be recalculated if the PTG is shorted.

Please note that the maximum signal current at the two-wire side can not be greater than 9 mA.

How to use POV:

1. Decide what overhead voltage ( $V_{TRO}$ ) is needed. The POV function is only needed if the overhead voltage exceeds  $1.1 V_{Peak}$ .
2. In [Figure 13](#) the corresponding  $R_{OV}$  for the decided  $V_{TRO}$  can be found.
3. If the overhead voltage exceeds  $3.2 V_{Peak}$ , the  $G_{2-4S}$  gain has to be changed to -6.02 dB by connecting PTG pin to AGND



**Figure 13 Programmable Overhead Voltage (POV).  $R_L = 600 \Omega$  or Infinite**

### 6.3 Analog Temperature Guard

The widely varying environmental conditions in which SLICs operate may lead to the chip temperature limitations being exceeded. The PBL 38621/2 SLIC reduces the DC line current when the chip temperature reaches approximately 145 °C and increases line current again automatically when the temperature drops. Accordingly, transmission is not lost under high ambient temperature conditions.

The detector output, DET, is forced to a logic low level when the temperature guard is active.

## 7 Loop Monitoring Functions

The loop current, ground key and ring-trip detectors report their status through a common output, DET. The particular detector to be connected to the detector pin, DET, is selected via the three-bit control interface C1, C2 and C3. Please refer to Chapter 9 for a description of the control interface.

### 7.1 Loop Current Detector

The loop current detector indicates that the telephone is off-hook and that DC current is flowing in the loop by setting the output pin DET to a logic low level when selected. The loop current detector threshold value,  $I_{LTh}$ , where the loop current detector changes state, is programmable with the  $R_{LD}$  resistor.  $R_{LD}$  connects between pin PLD and ground and is calculated according to:

$$R_{LD} = \frac{500}{I_{LTh}} \quad [16]$$

The loop current detector is internally filtered and is not influenced by the AC signal at the two-wire side.

### 7.2 Ground Key Detector

The ground key detector is indicating when the ground key is pressed (active) by putting the output pin DET to a logical high level, when selected. The ground key detector circuit senses the difference between TIPX and RINGX currents. When the current at the RINGX side exceeds the current at the TIPX side with the threshold value, the detector is triggered. For threshold current values, please refer to the datasheet.

### 7.3 Ring Trip Detector

Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR. The ringing source can be balanced or unbalanced superimposed on  $V_B$  or GND. The unbalanced ringing source may be applied to either the ring lead or the tip lead with return via the other wire. A ring relay driven by the SLIC ring relay driver connects the ringing source to tip and ring.

The ring trip function is based on a polarity change at the comparator input when the line goes off-hook. In the on-hook state no DC current flows through the loop and the voltage at comparator input DT is more positive than the voltage at input DR. When the line goes off-hook, while ring relay is energized, DC current flows and the comparator input voltage reverses polarity.

**Figure 8** gives an example of a ring trip detector network. This network is applicable when the ring voltage is superimposed on  $V_B$  and is injected on the ring lead of the two-wire port. The DC voltage across sense resistor  $R_{RT}$  is monitored by the ring trip comparator input DT and DR via the network  $R_1, R_2, R_3, R_4, C_1$  and  $C_2$ .

When the line is on-hook (no DC current), DT is more positive than DR and the DET output will report logic level high, that is the detector is not tripped. When the line goes off-hook, while ringing, a DC current will flow through the loop including sense resistor  $R_{RT}$  and will cause input DT to become more negative than input DR. This changes output DET to logic level low, that is tripped detector conditions. The system controller (or line card processor) responds by de-energizing the ring relay, that is ring trip.

Complete filtering of the 20 Hz AC component at terminal DT and DR is not necessary. A toggling DET output can be examined by a software routine to determine the duty cycle. When the DET output is at logic level low for more than half the time, off-hook conditions is indicated.

## 8 Relay Driver

The PBL 38621/2 SLIC incorporates a ring relay driver designed as open collector (nnp), with a current sinking capability of 50 mA. The drive transistor emitter is connected to BGND. The relay driver has an internal zener diode clamp for inductive kick back voltages.

## 9 Control Inputs

The SLIC has three digital control inputs, C1, C2 and C3. A decoder in the SLIC interprets the control input condition and determining the commanded operating state. C1, C2 and C3 are internally pulled up.

### 9.1 Open Circuit (C3, C2, C1 = 0, 0, 0)

In the Open Circuit the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum and no detectors are active. DET output is set high.

### 9.2 Ringing (C3, C2, C1 = 0, 0, 1)

The ring relay driver and the ring trip detector are activated and the ring trip detector is indicating off-hook with a logic low level at the detector output.

As the SLIC do not have any stand by state the SLIC will remain in the active normal state.

### 9.3 Active States

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. VF signal transmission is normal. The loop current detector is activated. The loop current detector indicates off-hook with a logic low level and the ground key detector is indicating active ground key with a logic high level present at the detector output.

## 10 Overvoltage Protection

### 10.1 Overvoltage Protection - General

The SLIC must be protected against foreign voltages on the telephone line. Overvoltages can result from lightning, AC power contact, induction and other causes. Refer to [Table 3](#), TIPX and RINGX terminals, for maximum continuous and transient voltages that may be applied to the SLIC.

### 10.2 Secondary Protection

The circuit shown in [Figure 8](#) utilizes series resistors ( $R_{F1}$ ,  $R_{F2}$ ) together with a programmable overvoltage protector (OVP, for example Bournes TISP PBL2) as secondary protection.

The TISP PBL2 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to the negative supply

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**Power-Up Sequence**

voltage (that is the battery voltage,  $V_B$ ). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by a diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage and the protector will crowbar into a low voltage on-state condition, by firing an internal thyristor.

A gate decoupling capacitor,  $C_{GG}$ , is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector.  $C_{GG}$  should be placed close to the overvoltage protection device. Without the capacitor even the low inductance in the track to the  $V_B$  supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors  $R_F$  serve the dual purposes of being non-destructive energy dissipators when transients are clamped, and of being fuses when the line is exposed to a power cross. If a PTC is chosen for  $R_F$ , note that it is important to always use PTC's in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore will not protect the SLIC.

## **11 Power-Up Sequence**

No special power-up sequence is necessary, except that ground has to be present before all other power supply voltages.

## **12 Printed Circuit Board Layout**

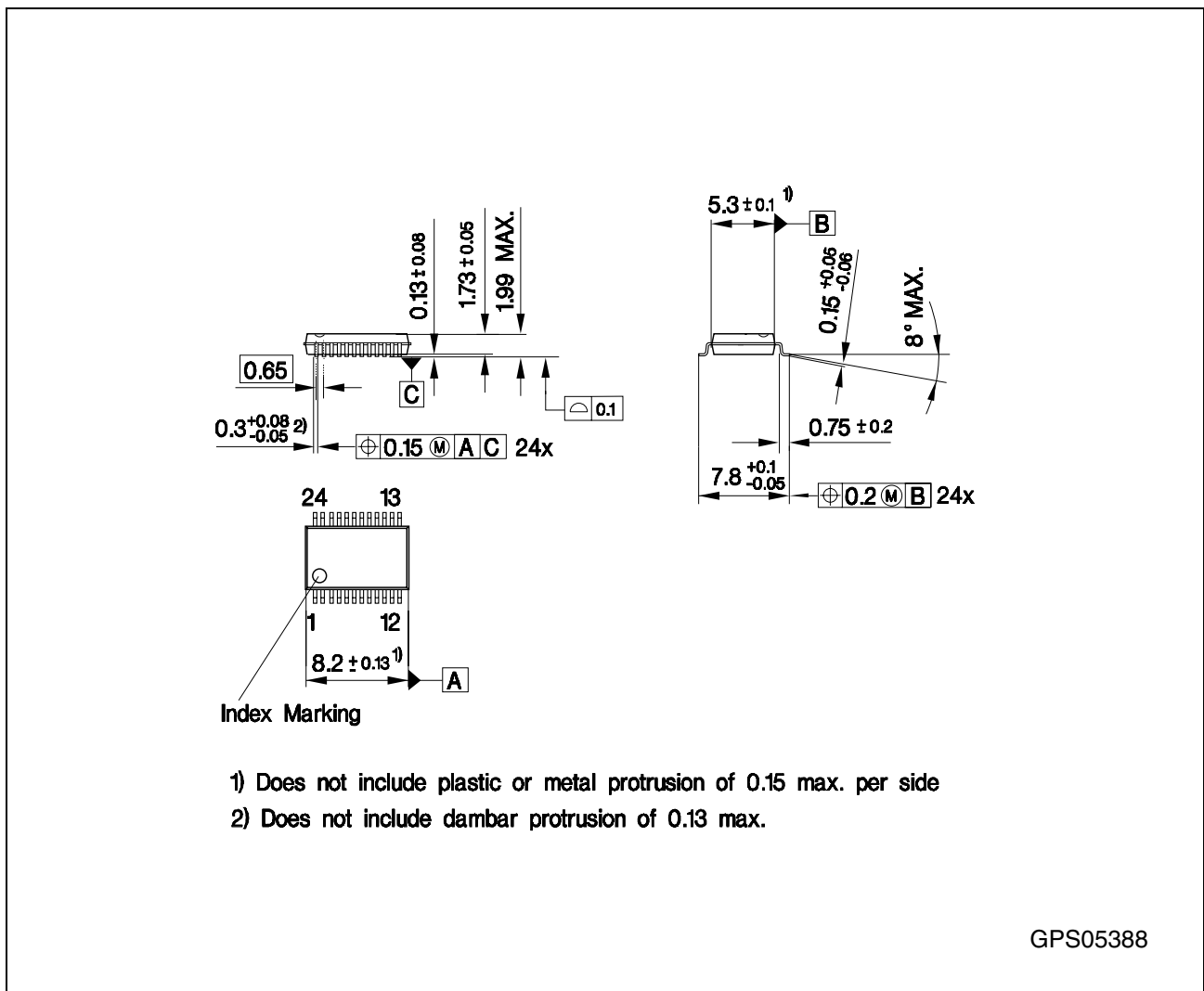
Care in Printed Circuit Board (PCB) layout is essential for proper function. The components connection to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the receive summing node (RSN). Ground plane surrounding the RSN pin is advisable.

Analog Ground (AGND) should be connected to Battery Ground (BGND) on the PCB, in one point. The capacitors for the battery should be connected with short wide leads of the same length.

## 13 Package Outlines

The SLIC is provided in three different packages: 24-pin SSOP, 24-pin SOIC and 28-pin PLCC.

### 13.1 24-pin SSOP Package



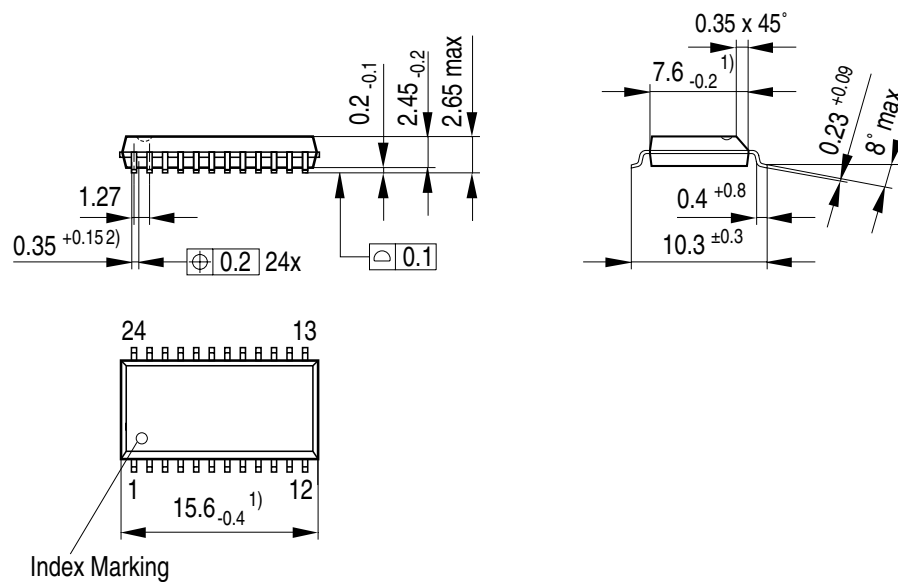
**Figure 14**    **P-SSOP-24-1** (Plastic Shrink Small Outline Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: <http://www.infineon.com/products>.

SMD = Surface Mounted Device

Dimensions in mm

## 13.2 24-pin SOIC Package



- 1) Does not include plastic or metal protrusions of 0.15 max per side  
2) Does not include dambar protrusion of 0.05 max per side

GPS05144

GPS05144

**Figure 15 P-DSO-24-1 (Plastic Dual Small Outline Package)**

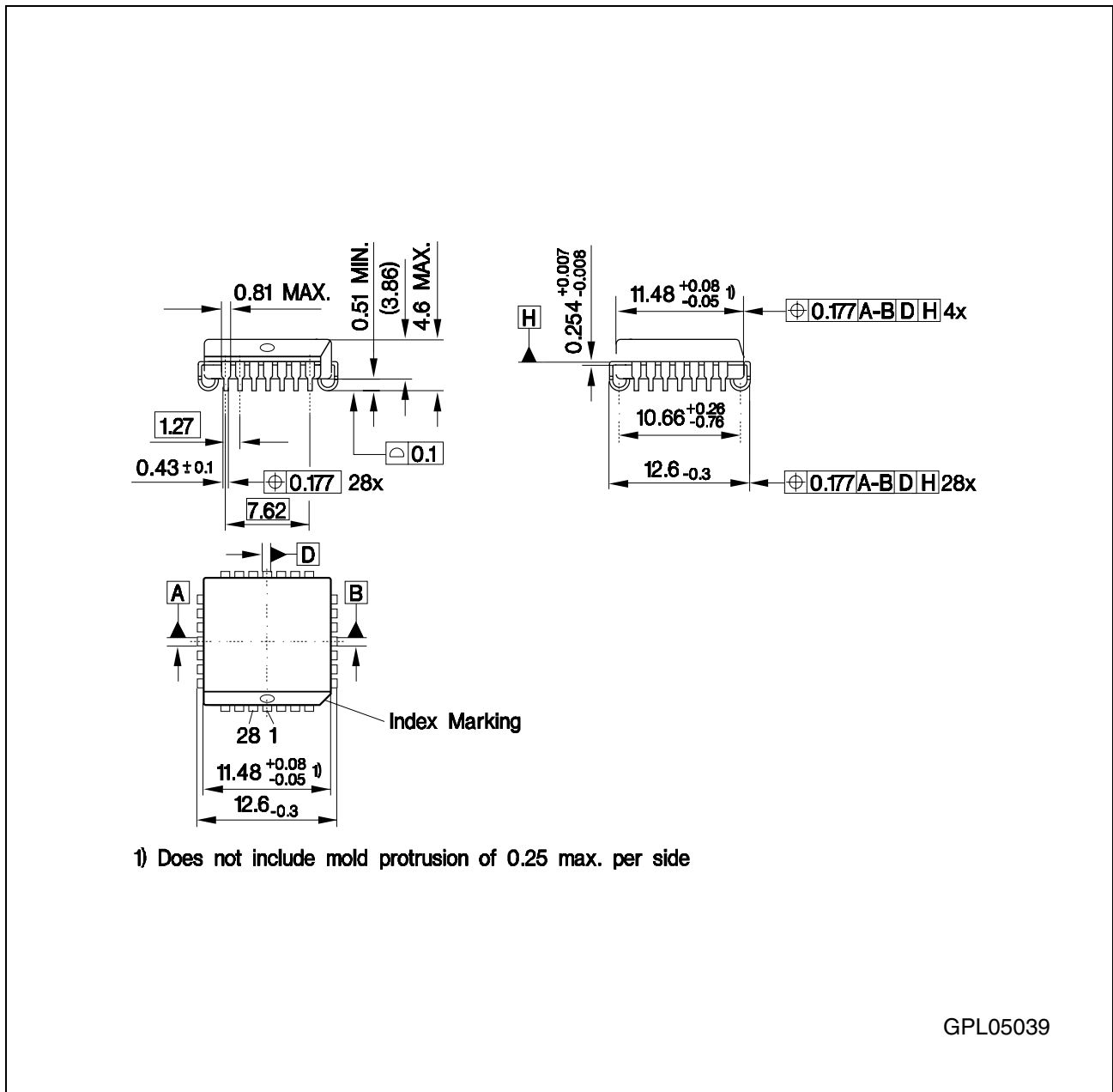
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SMD = Surface Mounted Device

Dimensions in mm



### 13.3 28-pin PLCC Package



**Figure 16 P-LCC-28-2 (Plastic Leaded Chip Carrier Package)**

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SMD = Surface Mounted Device

Dimensions in mm

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