

TBB1017

Twin Built in Biasing Circuit MOS FET IC UHF/VHF RF Amplifier

REJ03G1469-0100

Rev.1.00

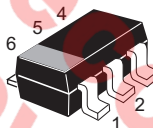
Aug 07, 2006

Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- Very useful for total tuner cost reduction.
- Suitable for World Standard Tuner RF amplifier.
- High gain
- Low noise
- Low output capacitance
- Power supply voltage: 5 V

Outline

RENESAS Package code: PTSP0006JA-A
(Package name: CMPAK-6)



1. Drain(1)
2. Source
3. Gate-1(1)
4. Gate-1(2)
5. Gate-2
6. Drain(2)

- Notes:
1. Marking is "SM".
 2. TBB1017 is individual type number of Renesas TWIN BBFET.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 -0	V
Gate2 to source voltage	V_{G2S}	+6 -0	V
Drain current	I_D	30	mA
Channel power dissipation	P_{ch} ^{Note3}	250	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 3. Value on the glass epoxy board (50mm × 40mm × 1mm).

Electrical Characteristics

• FET1

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200 \mu A$, $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10 \mu A$, $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	$I_{G2} = +10 \mu A$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5 V$, $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	$V_{G2S} = +5 V$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.8	1.1	V	$V_{DS} = 5 V$, $V_{G2S} = 4 V$, $I_D = 100 \mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.4	0.7	1.0	V	$V_{DS} = 5 V$, $V_{G1S} = 5 V$, $I_D = 100 \mu A$
Drain current	$I_{D(op)}$	12	16	20	mA	$V_{DS} = 5 V$, $V_{G1} = 5 V$ $V_{G2S} = 4 V$, $R_G = 100 k\Omega$
Forward transfer admittance	$ y_{fs} $	27	32	38	mS	$V_{DS} = 5 V$, $V_{G1} = 5 V$, $V_{G2S} = 4 V$, $f = 1 kHz$, $R_G = 100 k\Omega$
Input capacitance	C_{iss}	1.3	1.7	2.1	pF	$V_{DS} = 5 V$, $V_{G1} = 5 V$, $V_{G2S} = 4 V$, $f = 1 MHz$, $R_G = 100 k\Omega$
Output capacitance	C_{oss}	0.7	1.1	1.5	pF	
Power gain	PG	15	20	25	dB	$V_{DS} = 5 V$, $V_{G1} = 5 V$, $V_{G2S} = 4 V$, $R_G = 100 k\Omega$, $f = 900 MHz$
Noise figure	NF	—	1.95	2.7	dB	

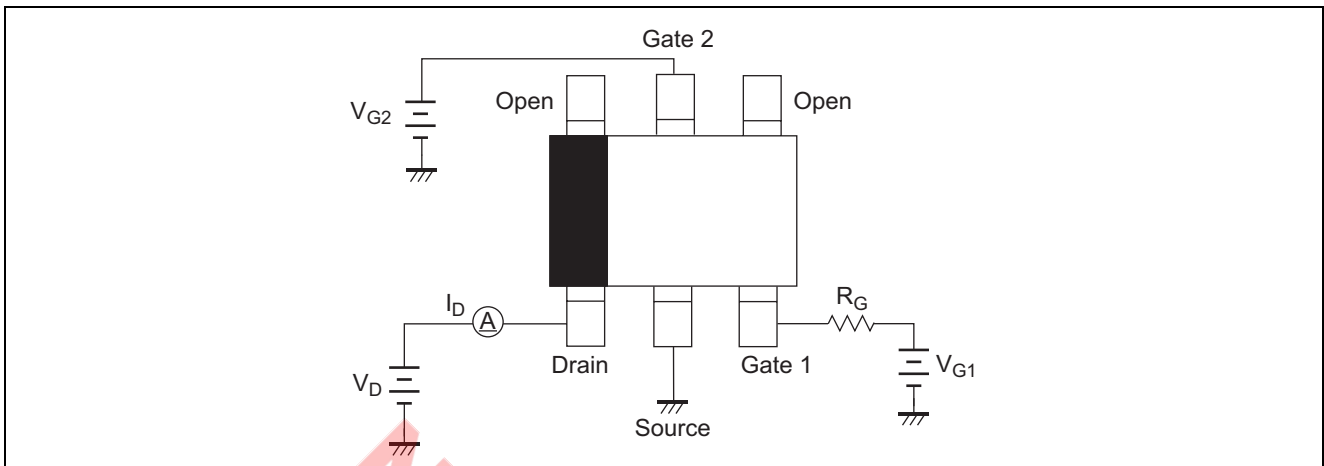
• FET2

(Ta = 25°C)

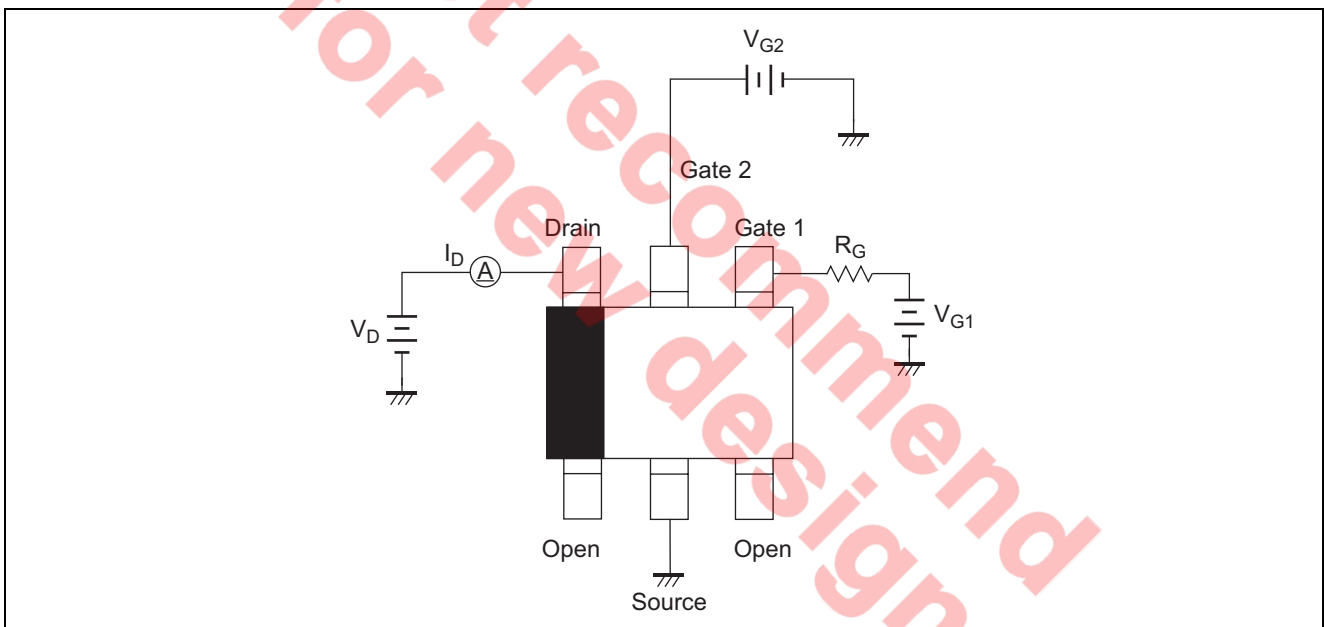
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200 \mu A$, $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10 \mu A$, $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	$I_{G2} = +10 \mu A$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5 V$, $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	$V_{G2S} = +5 V$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.8	1.1	V	$V_{DS} = 5 V$, $V_{G2S} = 4 V$, $I_D = 100 \mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.4	0.7	1.0	V	$V_{DS} = 5 V$, $V_{G1S} = 5 V$, $I_D = 100 \mu A$
Drain current	$I_{D(op)}$	13	17	21	mA	$V_{DS} = 5 V$, $V_{G1} = 5 V$ $V_{G2S} = 4 V$, $R_G = 82 k\Omega$
Forward transfer admittance	$ y_{fs} $	25	30	35	mS	$V_{DS} = 5 V$, $V_{G1} = 5 V$, $V_{G2S} = 4 V$, $f = 1 kHz$, $R_G = 82 k\Omega$
Input capacitance	C_{iss}	2.3	2.7	3.1	pF	$V_{DS} = 5 V$, $V_{G1} = 5 V$, $V_{G2S} = 4 V$, $f = 1 MHz$, $R_G = 82 k\Omega$
Output capacitance	C_{oss}	0.9	1.3	1.7	pF	
Power gain	PG	24	29	34	dB	$V_{DS} = 5 V$, $V_{G1} = 5 V$, $V_{G2S} = 4 V$, $R_G = 82 k\Omega$, $f = 200 MHz$
Noise figure	NF	—	1.0	1.6	dB	

DC Biasing Circuit for Operating Characteristic Items ($I_{D(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , NF , PG)

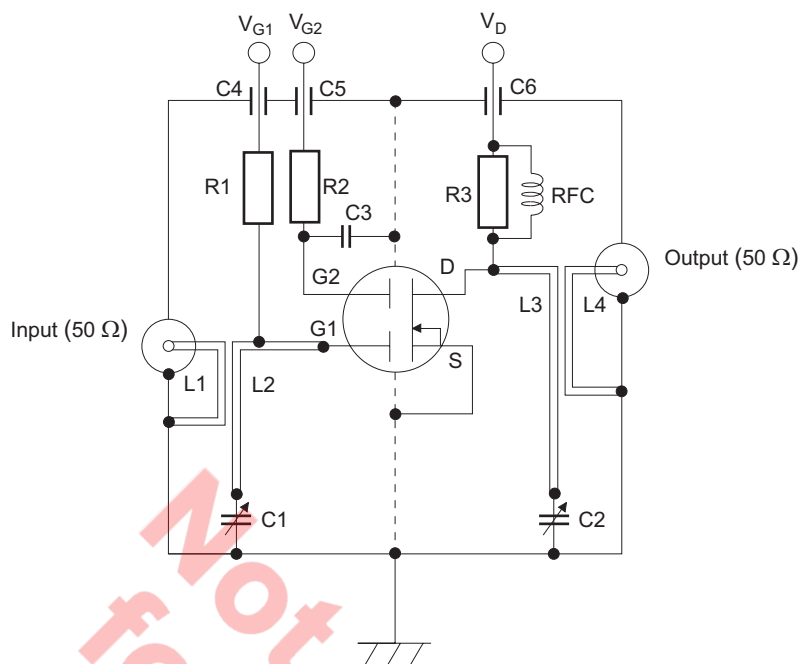
• Measurement of FET1



• Measurement of FET2

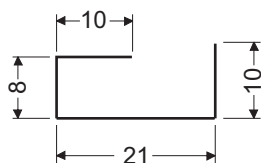


900 MHz Power Gain, Noise Figure Test Circuit



- C1, C2 : Variable Capacitor (10 pF MAX)
 C3 : Disk Capacitor (1000 pF)
 C4 ~ C6 : Air Capacitor (1000 pF)
 R1 : 100 k Ω
 R2 : 47 k Ω
 R3 : 4.7 k Ω

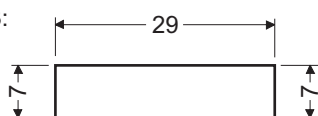
L1:



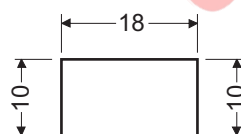
L2:



L3:

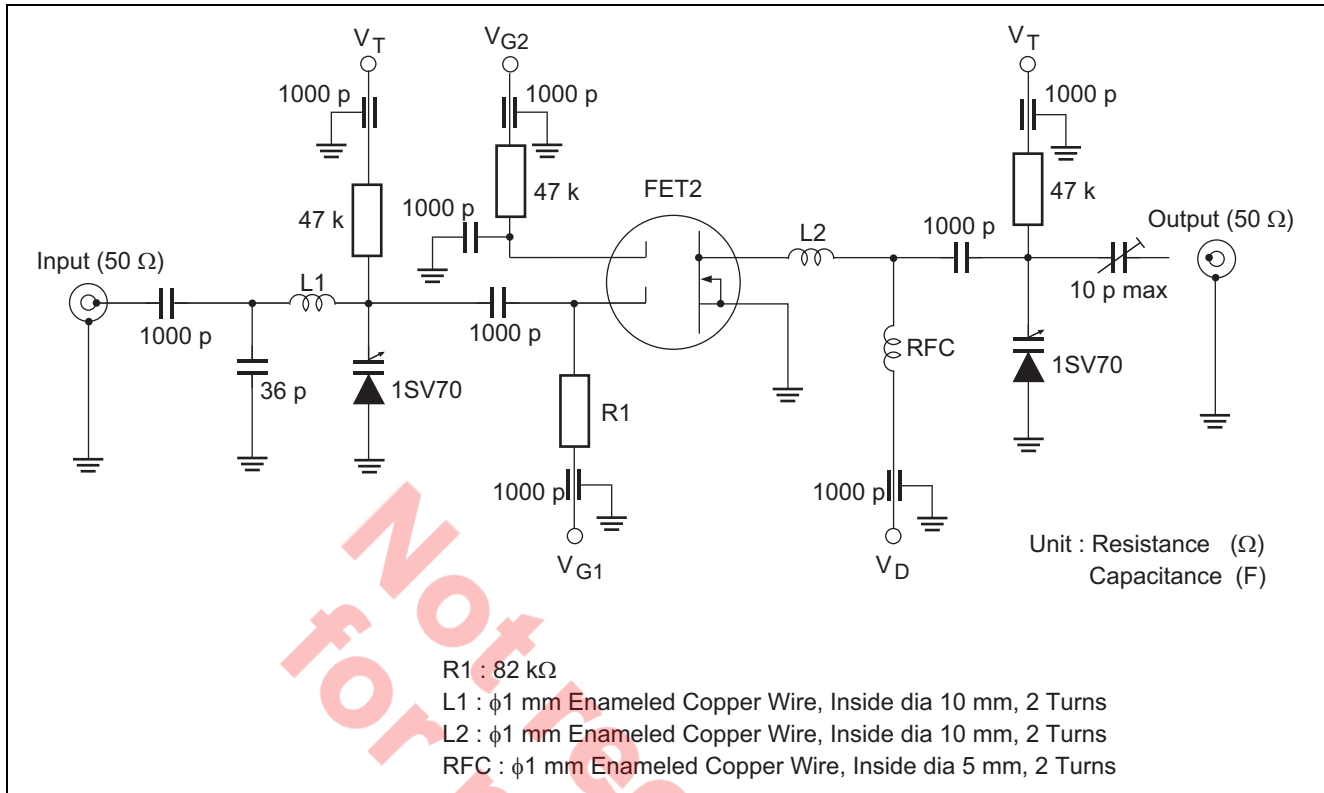


L4:



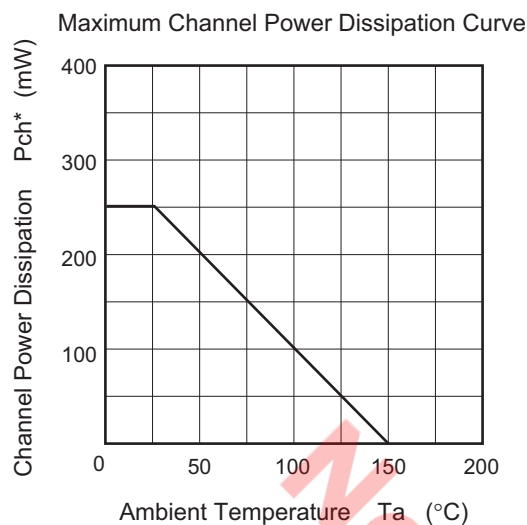
RFC : ϕ 1 mm Copper wire with enamel 4 turns inside dia 6 mm

200 MHz Power Gain, Noise Figure Test Circuit

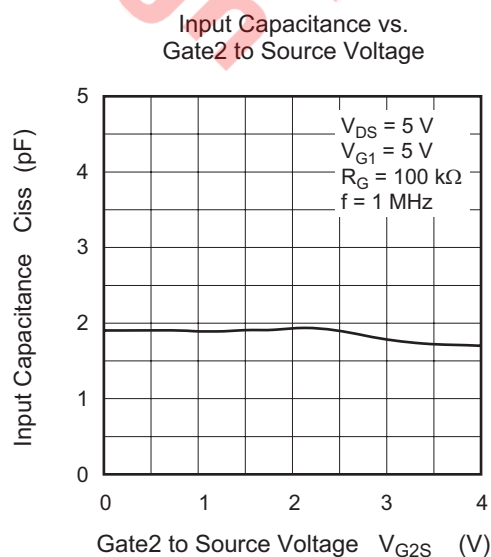
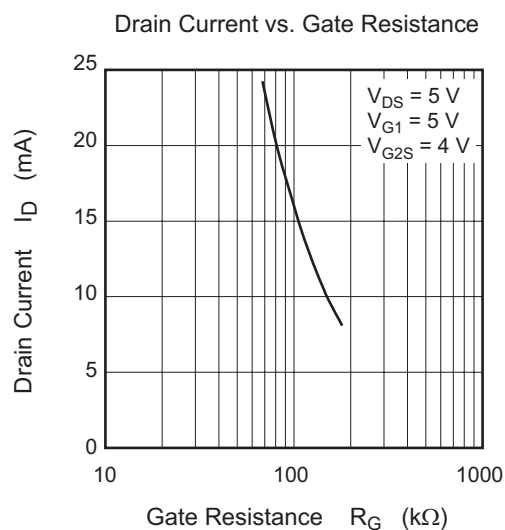
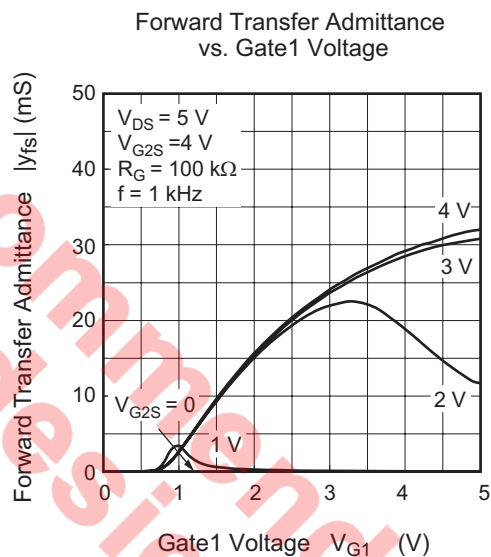
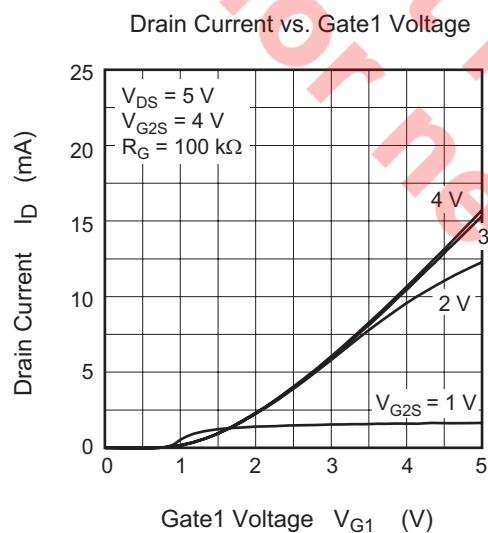
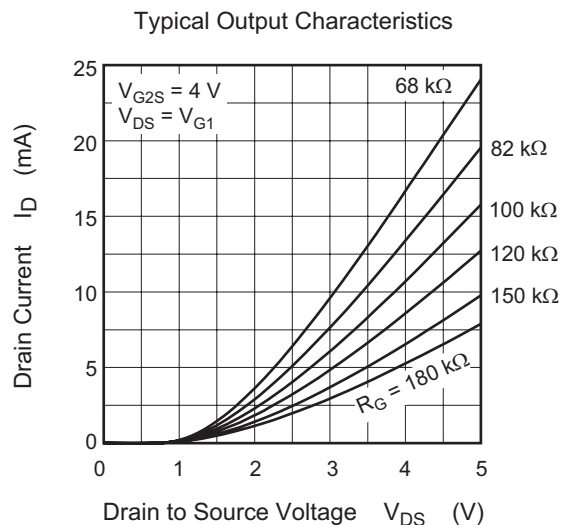


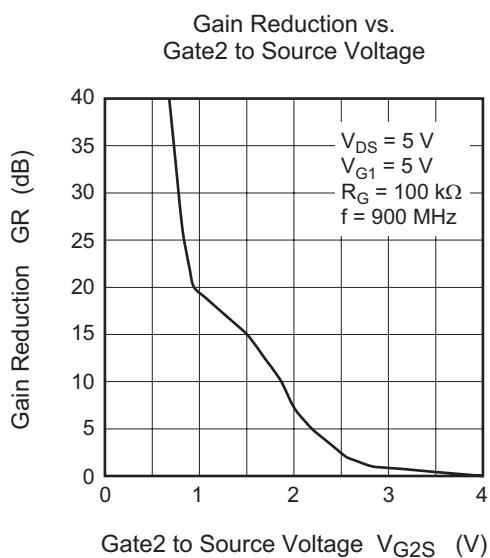
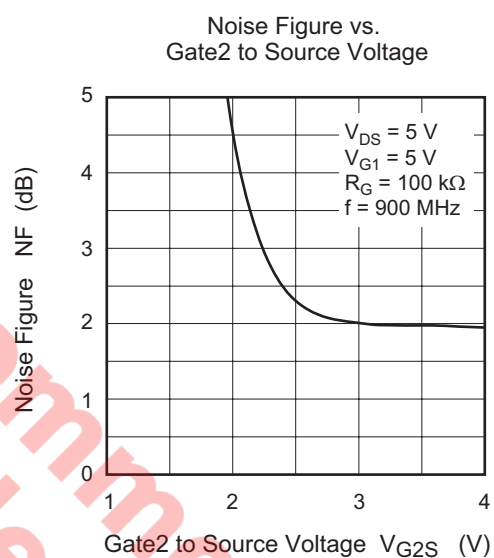
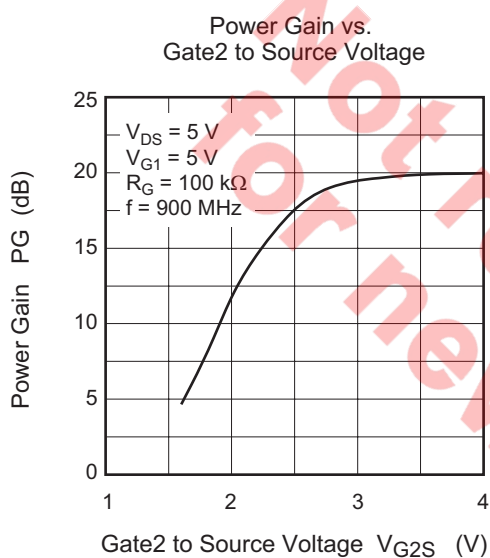
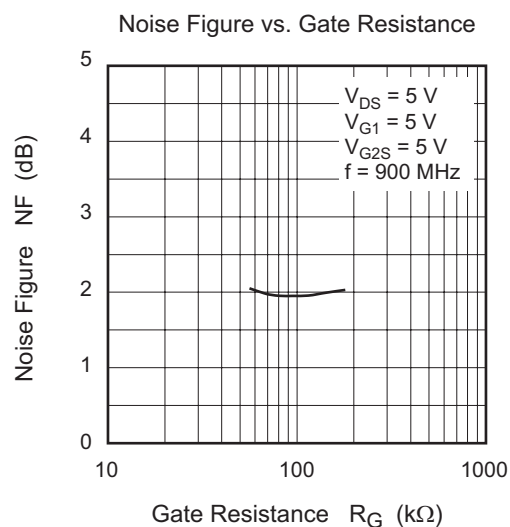
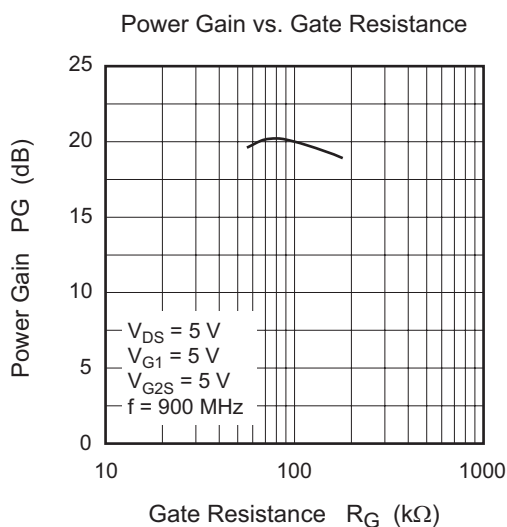
Main Characteristics

• FET1

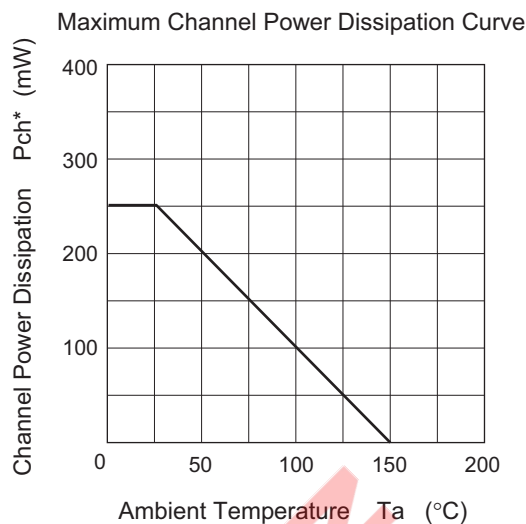


* Value on the glass epoxy board (50 mm × 40 mm × 1 mm)

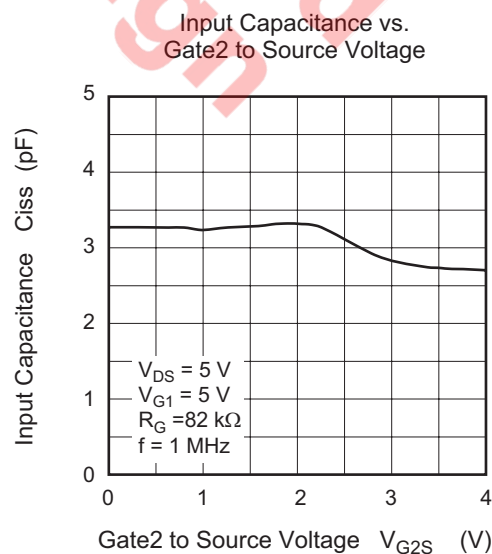
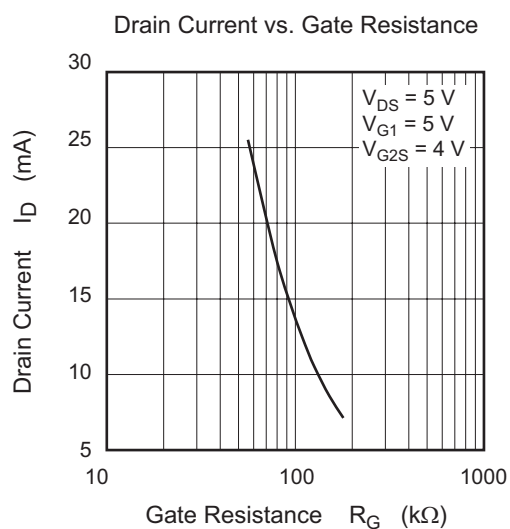
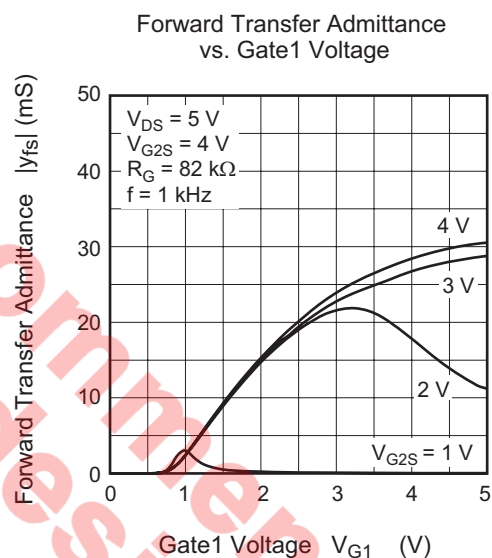
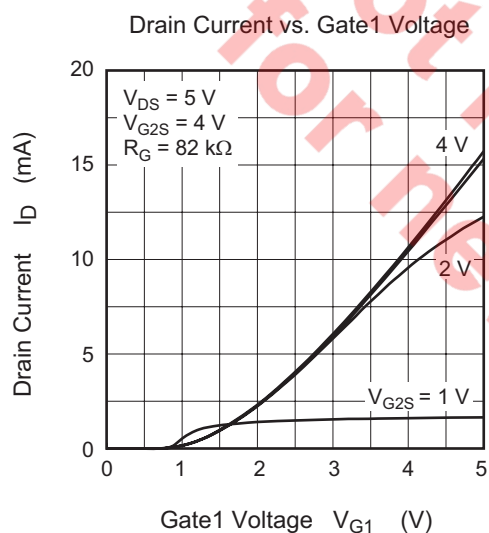
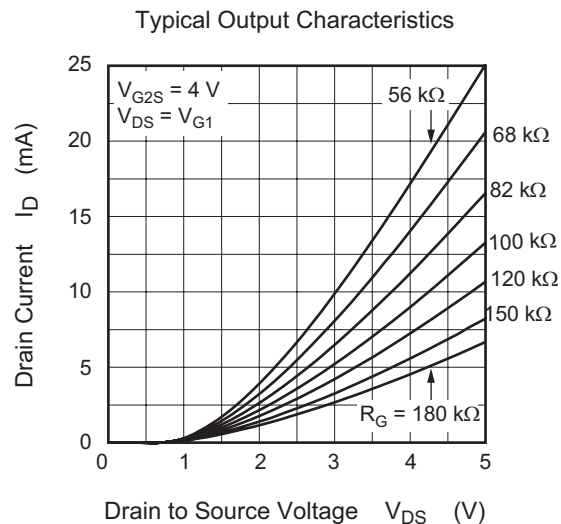


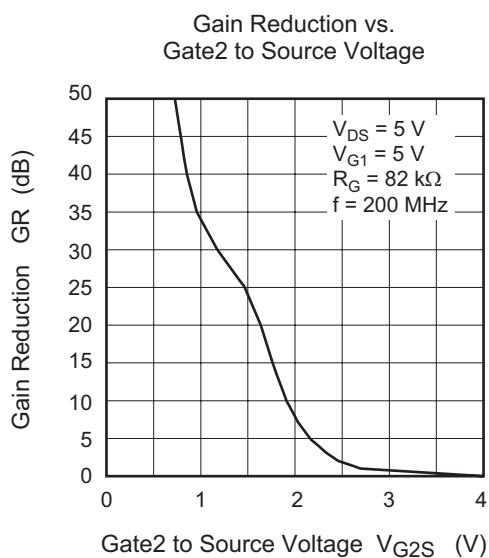
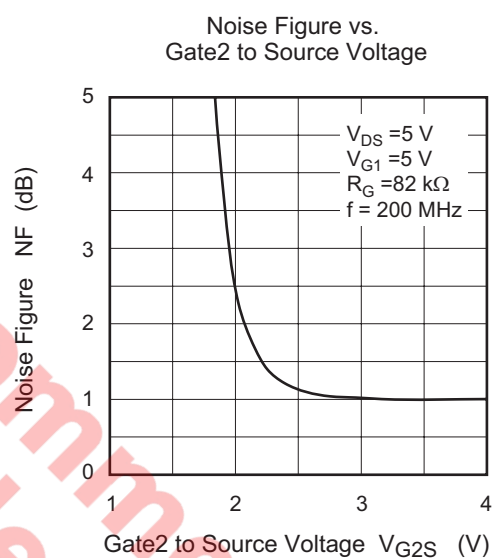
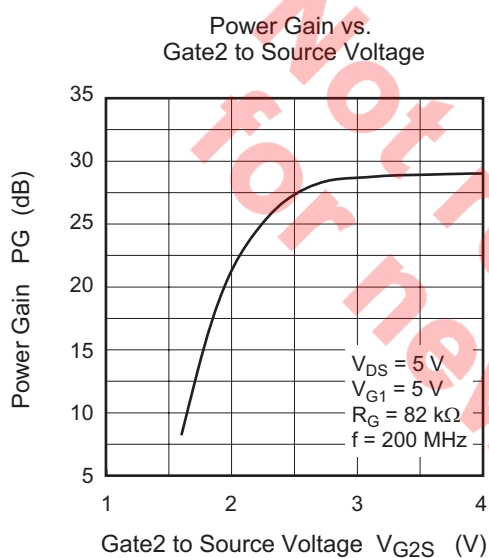
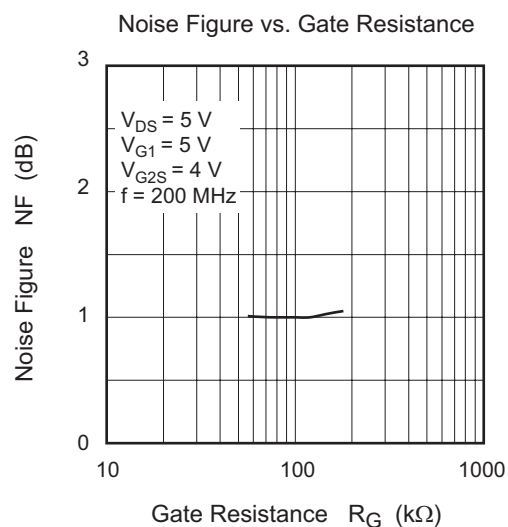
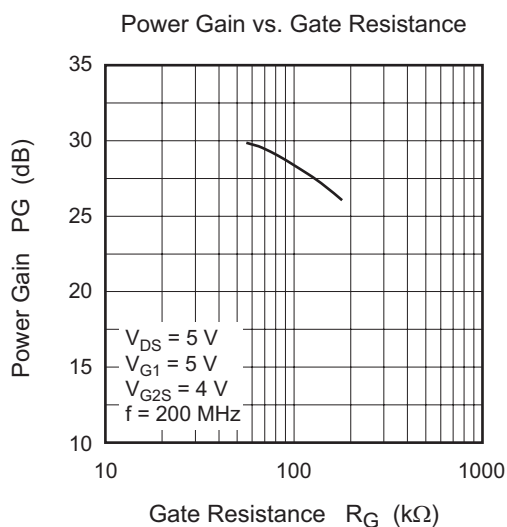


• FET2

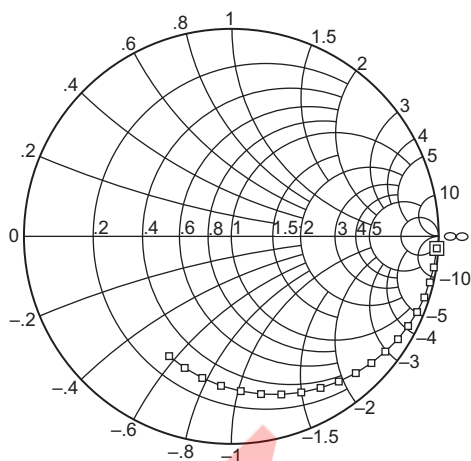


* Value on the glass epoxy board (50 mm × 40 mm × 1 mm)

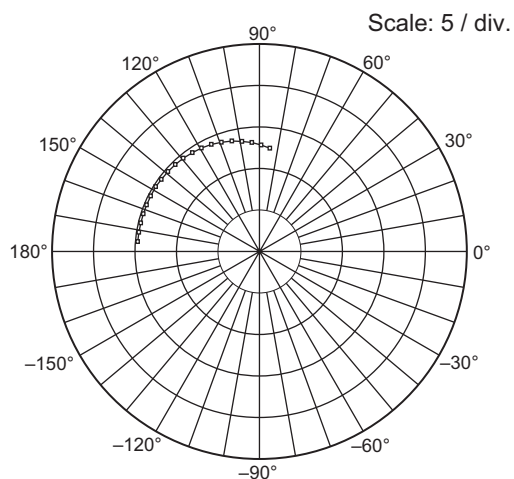




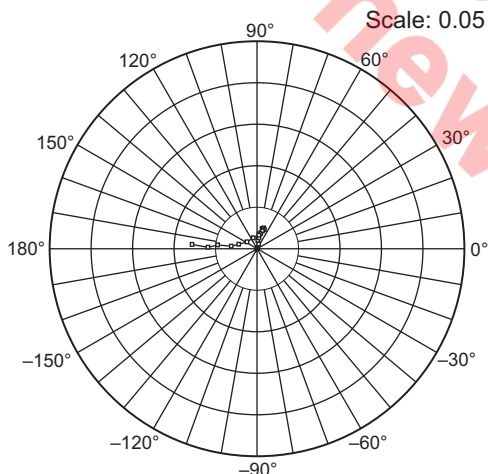
• FET1

S₁₁ Parameter vs. Frequency

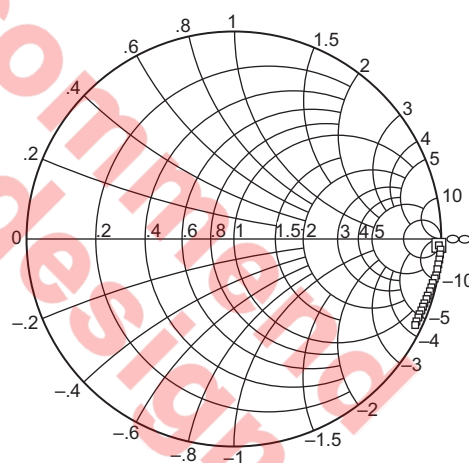
Test condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$,
 $V_{G2S} = 4\text{ V}$, $R_G = 100\text{ k}\Omega$
 0.05 to 1.05 GHz (0.05 GHz step)

S₂₁ Parameter vs. Frequency

Test condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$,
 $V_{G2S} = 4\text{ V}$, $R_G = 100\text{ k}\Omega$
 0.05 to 1.05 GHz (0.05 GHz step)

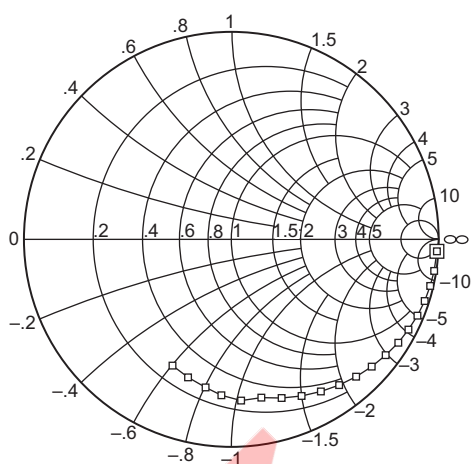
S₁₂ Parameter vs. Frequency

Test condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$,
 $V_{G2S} = 4\text{ V}$, $R_G = 100\text{ k}\Omega$
 0.05 to 1.05 GHz (0.05 GHz step)

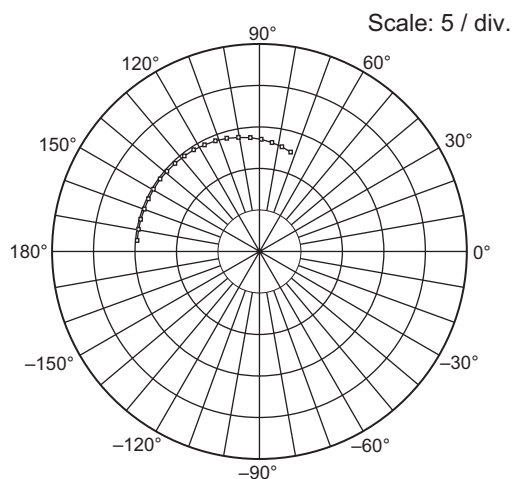
S₂₂ Parameter vs. Frequency

Test condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$,
 $V_{G2S} = 4\text{ V}$, $R_G = 100\text{ k}\Omega$
 0.05 to 1.05 GHz (0.05 GHz step)

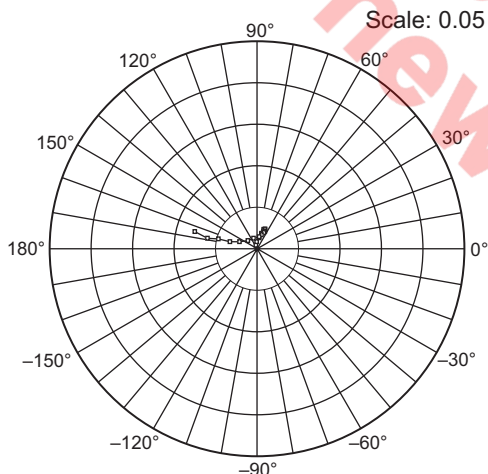
• FET2

S₁₁ Parameter vs. Frequency

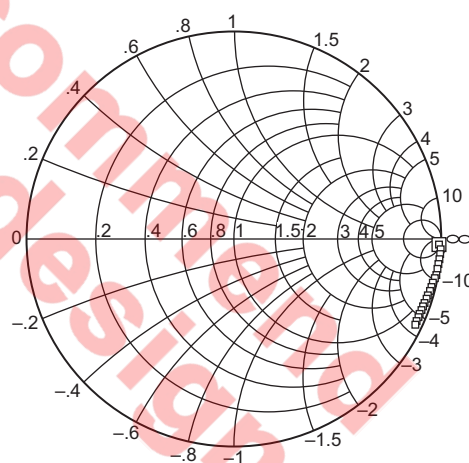
Test condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$,
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 0.05 to 1.05 GHz (0.05 GHz step)

S₂₁ Parameter vs. Frequency

Test condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$,
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 0.05 to 1.05 GHz (0.05 GHz step)

S₁₂ Parameter vs. Frequency

Test condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$,
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 0.05 to 1.05 GHz (0.05 GHz step)

S₂₂ Parameter vs. Frequency

Test condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$,
 $V_{G2S} = 4\text{ V}$, $R_G = 82\text{ k}\Omega$
 0.05 to 1.05 GHz (0.05 GHz step)

S parameter

• FET1

(V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V, R_G = 100 kΩ, Z_o = 50 Ω)

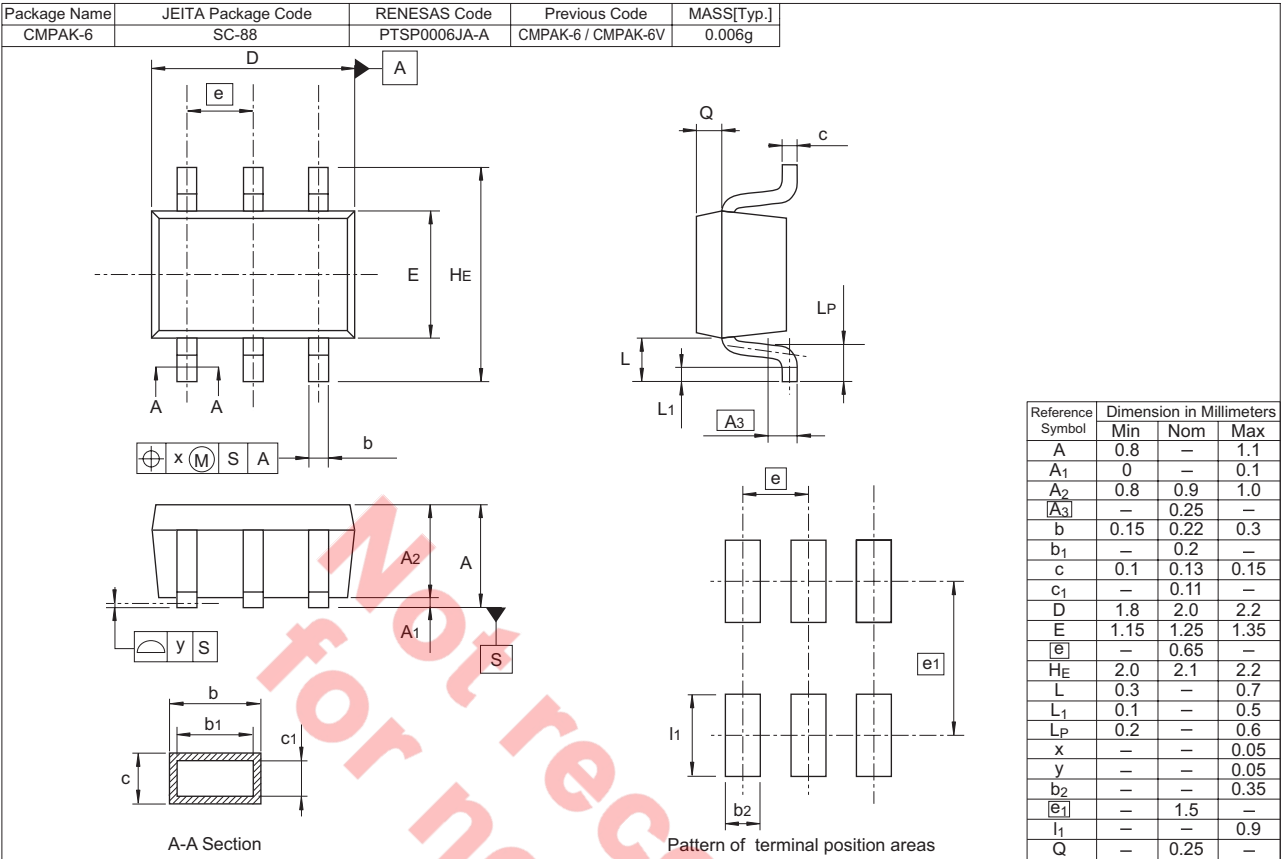
Freq. (MHz)	S11		S21		S12		S22	
	Mag	Deg	Mag	Deg	Mag	Deg	Mag	Deg
50	0.994	-4.2	2.97	175.6	0.001	74.5	0.999	-1.3
100	0.992	-8.8	2.97	171.1	0.002	89.6	0.998	-2.8
150	0.987	-13.1	2.97	166.7	0.002	81.5	0.997	-4.2
200	0.980	-17.6	2.97	162.2	0.003	81.6	0.996	-5.6
250	0.972	-22.2	2.97	157.8	0.004	77.8	0.994	-7.0
300	0.960	-26.9	2.96	153.1	0.005	76.9	0.993	-8.3
350	0.948	-31.7	2.97	148.1	0.005	73.8	0.992	-10.1
400	0.932	-36.8	2.96	143.8	0.005	72.9	0.988	-11.0
450	0.915	-42.1	2.95	139.0	0.005	69.4	0.983	-12.4
500	0.896	-47.7	2.94	134.2	0.004	73.3	0.981	-13.6
550	0.875	-53.4	2.93	129.4	0.004	73.7	0.979	-14.8
600	0.852	-59.5	2.92	124.3	0.003	78.4	0.974	-16.2
650	0.828	-65.8	2.89	119.4	0.003	83.8	0.973	-17.2
700	0.803	-72.4	2.85	114.4	0.003	113.5	0.970	-18.5
750	0.777	-79.2	2.81	109.4	0.003	151.7	0.969	-19.6
800	0.751	-86.4	2.77	104.3	0.005	169.5	0.968	-20.7
850	0.725	-93.8	2.71	99.3	0.006	176.7	0.966	-22.0
900	0.700	-101.4	2.66	94.4	0.010	176.0	0.967	-22.9
950	0.676	-109.3	2.59	89.4	0.012	179.6	0.966	-24.2
1000	0.653	-117.2	2.52	84.7	0.016	177.3	0.968	-25.3

• FET2

(V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V, R_G = 82 kΩ, Z_o = 50 Ω)

Freq (MHz)	S11		S21		S12		S22	
	Mag	Deg	Mag	Deg	Mag	Deg	Mag	Deg
50	0.986	-4.8	2.96	175.0	0.001	109.6	0.999	-1.8
100	0.983	-10.1	2.96	169.9	0.002	93.5	0.997	-4.0
150	0.980	-14.9	2.96	165.0	0.003	77.5	0.997	-5.9
200	0.972	-20.0	2.95	159.9	0.004	73.2	0.994	-8.0
250	0.964	-25.2	2.96	154.7	0.004	72.4	0.993	-9.9
300	0.952	-30.4	2.96	149.6	0.004	69.1	0.991	-11.9
350	0.938	-35.9	2.96	143.9	0.005	70.2	0.990	-14.2
400	0.924	-41.6	2.95	139.0	0.005	67.3	0.986	-15.7
450	0.906	-47.4	2.95	133.8	0.005	66.2	0.981	-17.7
500	0.888	-53.7	2.93	128.2	0.004	64.6	0.980	-19.5
550	0.869	-60.0	2.92	122.9	0.004	65.8	0.976	-21.4
600	0.844	-66.6	2.90	117.3	0.003	71.3	0.972	-23.3
650	0.822	-73.6	2.88	111.6	0.003	79.4	0.971	-25.0
700	0.797	-80.6	2.85	106.1	0.003	109.7	0.968	-26.9
750	0.770	-88.1	2.80	100.5	0.003	139.9	0.966	-28.6
800	0.745	-95.9	2.76	94.7	0.004	159.6	0.965	-30.3
850	0.720	-103.8	2.71	89.2	0.007	166.6	0.963	-32.2
900	0.693	-112.2	2.65	83.6	0.010	166.5	0.964	-33.7
950	0.670	-120.7	2.58	78.0	0.012	168.6	0.963	-35.6
1000	0.647	-130.1	2.51	72.8	0.015	165.0	0.965	-37.3

Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
TBB1017SMTL-E	3000 pcs	φ178 mm reel, 8 mm emboss taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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