



# CYPRESS

## B9947

### 3.3V, 160-MHz, 1:9 Clock Distribution Buffer

#### Product Features

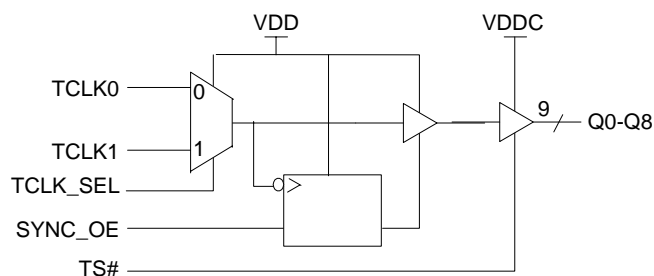
- 160-MHz Clock Support
- LVC MOS/LVTTL Compatible Inputs
- 9 Clock Outputs: Drive up to 18 Clock Lines
- Synchronous Output Enable
- Output Three-state Control
- 350-ps Maximum Output-to-Output Skew
- Pin Compatible with MPC947
- Industrial Temp. Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- 32-Pin TQFP Package

#### Description

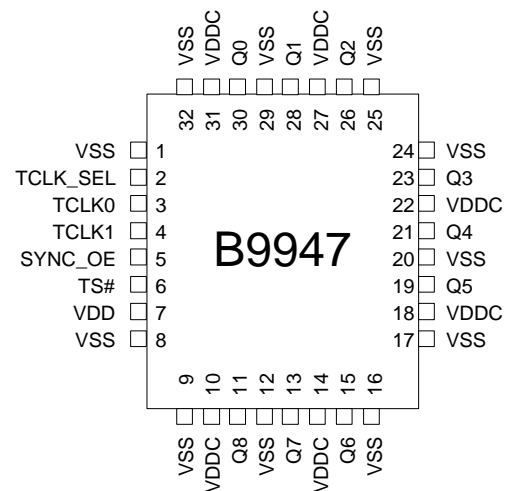
The B9947 is a low-voltage clock distribution buffer with the capability to select one of two LVC MOS/LVTTL compatible clock inputs. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVC MOS/LVTTL compatible. The nine outputs are 3.3V LVC MOS or LVTTL compatible and can drive two series terminated  $50\Omega$  transmission lines. With this capability the B9947 has an effective fanout of 1:18. The outputs can also be three-stated via the three-state input TS#. Low output-to-output skews make the B9947 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

The B9947 also provides a synchronous output enable input for enabling or disabling the output clocks. Since this input is internally synchronized to the input clock, potential output glitching or runt pulse generation is eliminated.

#### Block Diagram



#### Pin Configuration



## Pin Description

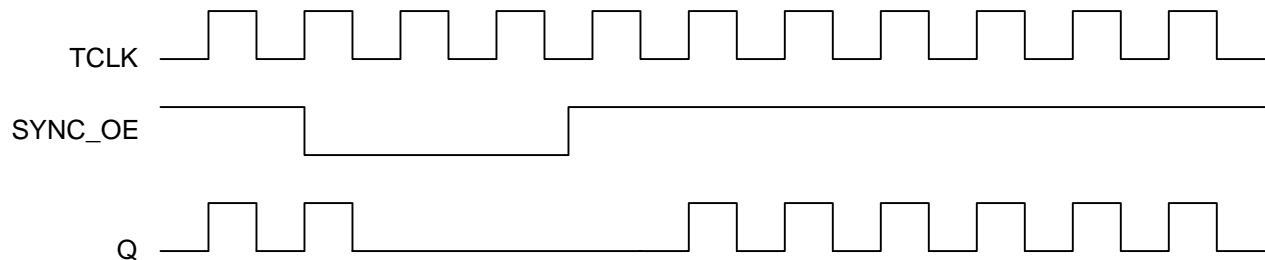
Pin	Name	PWR	I/O	Description
3	TCLK0		I, PU	Test Clock Input
4	TCLK1		I, PU	Test Clock Input
2	TCLK_SEL		I, PU	Test Clock Select Input. When LOW, TCLK0 is selected. When asserted HIGH, TCLK1 is selected.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q(8:0)	VDDC	O	Clock Outputs
5	SYNC_OE		I, PU	Output Enable Input. When asserted HIGH, the outputs are enabled and when set LOW the outputs are disabled in a LOW state.
6	TS#		I, PU	Three-state Control Input. When asserted LOW, the output buffers are three-stated. When set HIGH, the output buffers are enabled.
10, 14, 18, 22, 27, 31	VDDC			3.3V Power Supply for Output Clock Buffers
7	VDD			3.3V Power Supply
1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	VSS			Common Ground

**Note:**

1. PU = Internal Pull-Up.

## Output Enable/Disable

The B9947 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC\_OE is asserted LOW, the outputs are disabled in a LOW state. When SYNC\_OE is set HIGH, the outputs are enabled as shown in *Figure 1*.



**Figure 1. SYNC\_OE Timing Diagram**

## Maximum Ratings[2]

Maximum Input Voltage Relative to  $V_{SS}$ : .....  $V_{SS} - 0.3V$   
 Maximum Input Voltage Relative to  $V_{DD}$ : .....  $V_{DD} + 0.3V$   
 Storage Temperature: .....  $-65^{\circ}C$  to  $+150^{\circ}C$   
 Operating Temperature: .....  $-40^{\circ}C$  to  $+85^{\circ}C$   
 Maximum ESD protection ..... 2 KV  
 Maximum Power Supply: ..... 5.5V  
 Maximum Input Current: .....  $\pm 20$  mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

**DC Parameters:**  $V_{DDC} = 3.3V \pm 10\%$ ,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
	Input Low Voltage		$V_{SS}$		0.8	V
	Input High Voltage		2.0		$V_{DD}$	V
$I_{IL}$	Input Low Current (@ $V_{IL} = V_{SS}$ )	Note 3			-100	$\mu A$
$I_{IH}$	Input High Current (@ $V_{IL} = V_{DD}$ )				10	$\mu A$
$V_{OL}$	Output Low Voltage	$I_{OL} = 20$ mA, Note 4			0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -20$ mA, $V_{DDC} = 3.3V$ , Note 4	2.5			V
$I_{DD}$	Quiescent Supply Current	All $V_{DDC}$ and $V_{DD}$		1	2	mA
$C_{in}$	Input Capacitance				4	pF

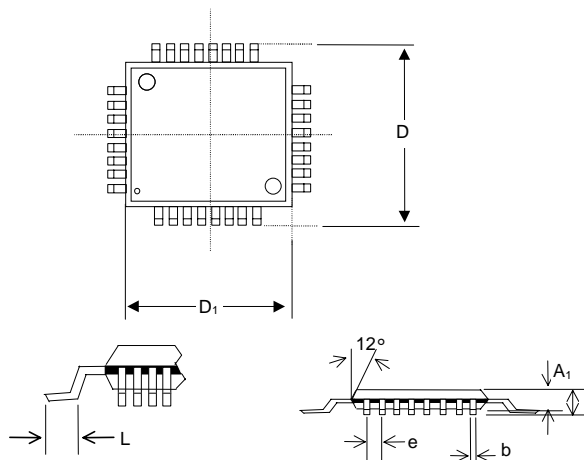
**AC Parameters**<sup>[5]</sup>:  $V_{DDC} = 3.3V \pm 10\%$ ,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Maximum Input Frequency <sup>[6]</sup>		160			MHz
Tpd	TCLK to Q Delay <sup>[6]</sup>		4.75		9.25	ns
FoutDC	Output Duty Cycle <sup>[6,7]</sup>	Measured at $V_{DDC}/2$	TCYCLE/2 - 800		TCYCLE/2 + 800	ps
tpZL, tpZH	Output Enable Time (all outputs)		2		10	ns
tpLZ, tpHZ	Output Disable Time (all outputs)		2		10	ns
Tskew	Output-to-Output Skew <sup>[6,9]</sup>				350	ps
Tskew (pp)	Part to Part Skew <sup>[10]</sup>				2.0	ns
Ts	Set-up Time <sup>[6,8]</sup>	SYNC_OE to TCLK	0.0			ps
Th	Hold Time <sup>[6,8]</sup>	TCLK to SYNC_OE	1.0			ps
Tr/Tf	Output Clocks Rise/Fall Time <sup>[9]</sup>	0.8V to 2.0V	0.20		1.0	ns

**Notes:**

2. The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up resistors that effect input current.
4. Driving series or parallel terminated 50 $\Omega$  (or 50 $\Omega$  to  $V_{DD}/2$ ) transmission lines.
5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving 50 $\Omega$  transmission lines.
7. 50% input duty cycle.
8. Set-up and Hold times are relative to the falling edge of the input clock
9. Outputs loaded with 30pF each
10. Part to Part Skew at a given temperature and voltage

## Package Drawing and Dimensions



## 32-Pin TQFP Outline Dimensions

Symbol	Inches			Millimeters		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A <sub>1</sub>	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.354	-	-	9.00	-
D <sub>1</sub>	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80 BSC		
L	0.018	-	0.030	0.45	-	0.75

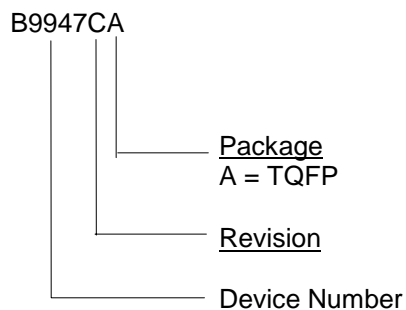
## Ordering Information

Part Number <sup>[11]</sup>	Package Type	Production Flow
B9947CA	32-Pin TQFP	Industrial, -40°C to +85°C

### Note:

11. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

**Marking:** Example: Cypress  
B9947CA  
Date Code, Lot #



<b>Document Title: B9947 3.3V, 160-MHz, 1:9 Clock Distribution Buffer</b> <b>Document Number: 38-07078</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	107114	06/06/01	IKA	Convert from IMI to Cypress
*A	108058	07/03/01	NDP	Changed Commercial to Industrial (See page 6)
*B	109804	01/31/02	DSG	Convert from Word to Frame
*C	122763	12/22/02	RBI	Add power up requirements to maximum ratings information