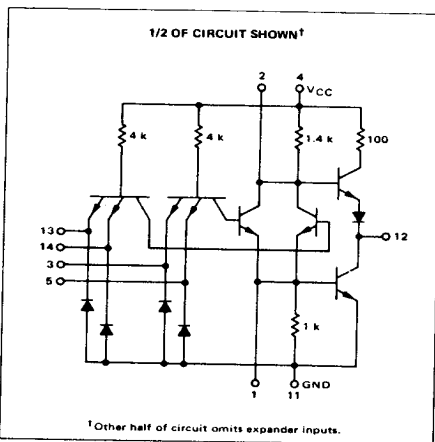


EXPANDABLE DUAL
2-WIDE 2-INPUT
"AND-OR-INVERT" GATE

MTTL MC5400F/7400F series

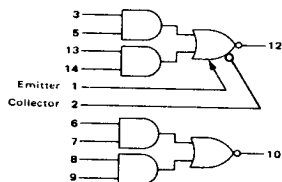
MC5450F*
MC7450F*



*F suffix = TO-85 ceramic package (Case 609).

See General Information section for package outline dimensions.

This device consists of two AND-OR-INVERT gates, one of which is OR expandable. Each gate is made up of two 2-input AND gates ORed together and inverted. Up to four MC5460/7460 expander gates may be ORed with the device at the expander points.



Positive Logic:

$$12 = (3 + 5) + (13 + 14) + (\text{Expanders})$$

Negative Logic:

$$3 + 5 = (13 + 14) + (\text{Expanders})$$

Input Loading Factor = 1

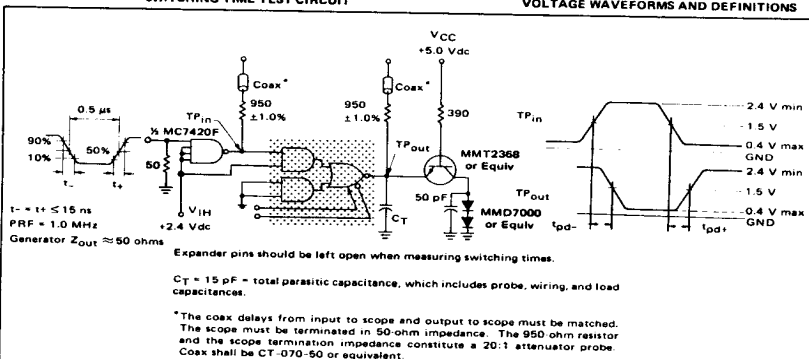
Output Loading Factor = 10

Total Power Dissipation = 28 mW typ/pkg

Propagation Delay Time = 13 ns typ

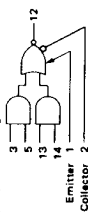
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Emitter Collector		TEST CURRENT/VOLTAGE VALUES (All Temperatures)																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																														
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		I_{C1}	I_{C2}	I_{C3}	I_{C4}	$R_{C1,2}$	$V_{C1,3}$	V_{C4}	V_{C5}	V_{C6}	V_{C7}	V_{C8}	V_{C9}	V_{C10}	V_{C11}																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
		16	-0.4	0.27	-0.27	0.2	138	0.4	5.5	2.4	5.5	4.5	5.0	2.0	0.8	5.0	5.5	2.7																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																														

*Consult input or gate pin under test.

**Tested only at 25°C.

3 See Figure 3

2 See Figure 2

1 See Figure 1

MC5450F, MC7450F (continued)

FIGURE 1 - I_{EX} TEST CIRCUIT

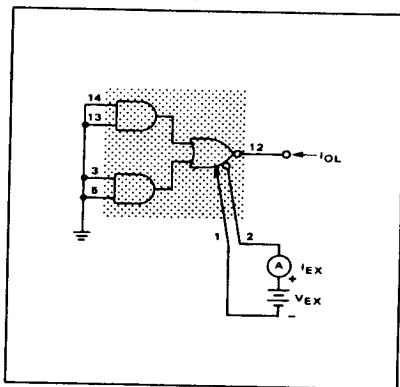


FIGURE 2 - V_{BE} TEST CIRCUIT

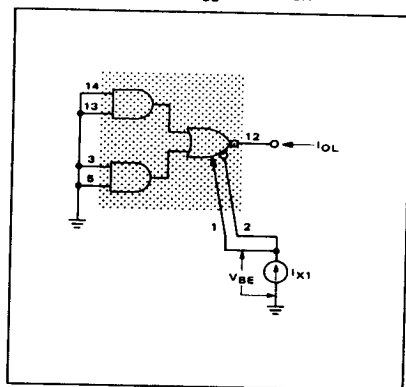


FIGURE 3 - V_{OL} TEST CIRCUIT

