8-bit microcontrollers with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM

PCD3756x

CONTENTS

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8-bit microcontrollers with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM

PCD3756x

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; in a single 28-lead or 32-lead package
- 8 kbytes user-programmable ROM (One-Time Programmable)
- 128 bytes RAM
- 128 bytes Electrically Erasable Programmable Read-Only Memory (EEPROM)
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- 3 single-level vectored interrupts:
  - external
  - Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Wake-up via external or Port 0 interrupt
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Operating temperature: –25 to 70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCD3756x are One-Time Programmable (OTP) microcontrollers oriented towards telephony applications. The different types differ in the Port and Power-on-reset configurations. All types include an on-chip dual tone multifrequency (DTMF) generator. In addition to dialling, generated frequencies can be made available as square waves (P1.7/MDY) for melody generation, providing ringer operation (in which case the tone output is disabled). A wake-up function via Port 0 interrupt facilitates keyboard interfacing.

The PCD3756x also incorporate 128 bytes of EEPROM. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family. This data sheet details the specific properties of the PCD3756x. The shared characteristics of the PCD33xxA family of microcontrollers are described in the:

"PCD33xxA Family" data sheet or

"Data Handbook IC03; Section PCD33xxA Family",

which should be read in conjunction with this publication.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3756xP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3756xT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3756xH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

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4 BLOCK DIAGRAM

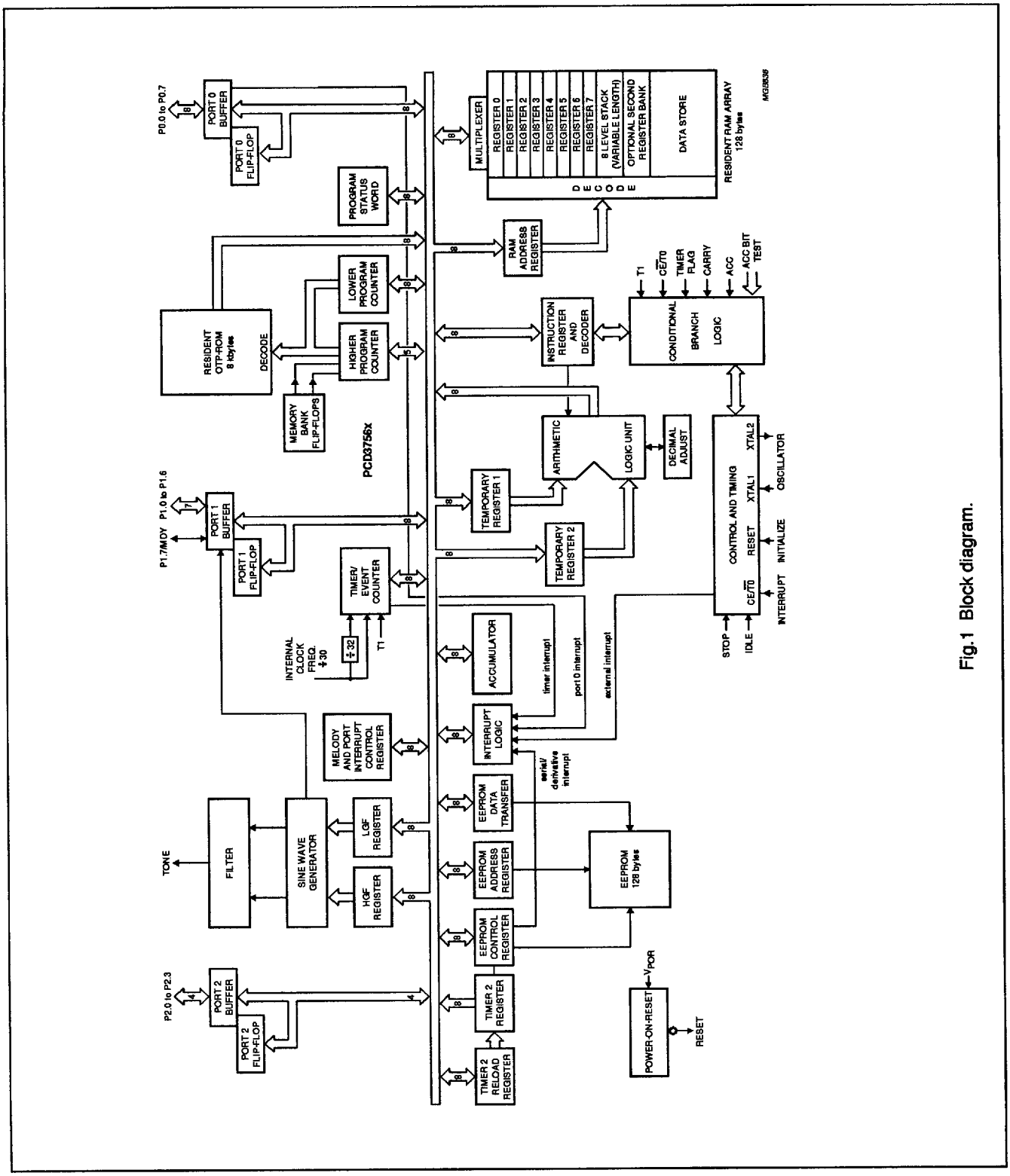

Fig.1 Block diagram.

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5 PINNING INFORMATION

5.1 Pinning

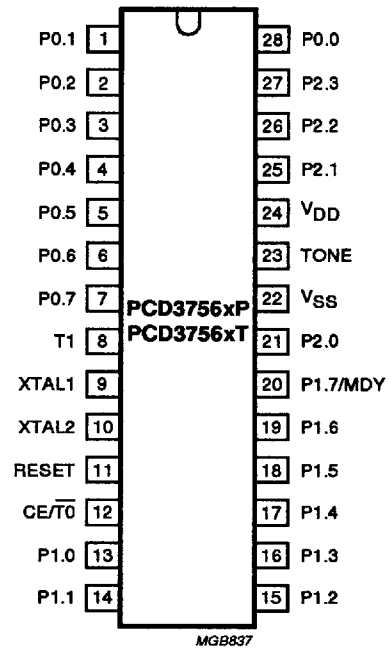

Fig.2 Pin configuration (SOT117-1 and SOT136-1).

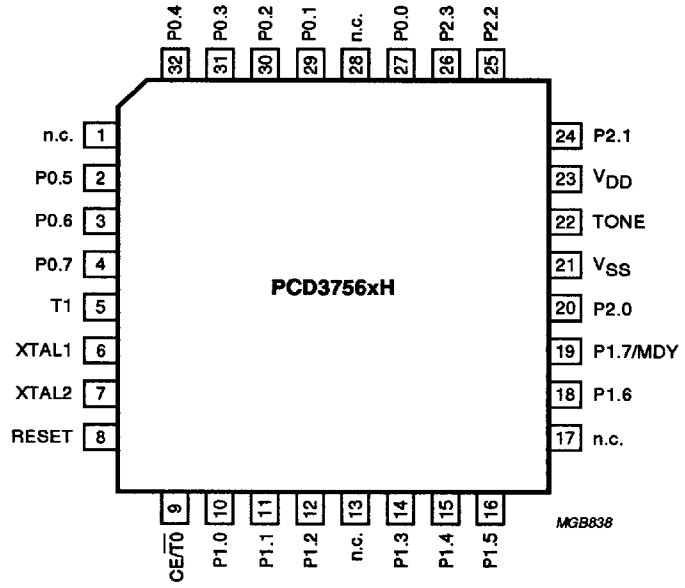

Fig.3 Pin configuration (SOT358-1).

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5.2 Pin description

Table 1 SOT117-1 and SOT136-1 packages (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
P0.0 to P0.7	28, 1 to 7	Port 0: 8 quasi-bidirectional I/O lines or wake-up interrupts
T1	8	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	crystal oscillator or external clock input
XTAL2	10	crystal oscillator output
RESET	11	reset input
CE/$\overline{T0}$	12	Chip Enable or Test 0
P1.0 to P1.6	13 to 19	Port 1: 7 quasi-bidirectional I/O lines
P1.7/MDY	20	Port 1: quasi-bidirectional I/O line or melody output
P2.0 to P2.3	21, 25 to 27	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	22	ground
TONE	23	DTMF output
V_{DD}	24	positive supply voltage

Table 2 SOT358-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
T1	5	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	6	crystal oscillator or external clock input
XTAL2	7	crystal oscillator output
RESET	8	reset input
CE/$\overline{T0}$	9	Chip Enable or Test 0
P1.0 to P1.6	10 to 12, 14 to 16, 18	Port 1: 7 quasi-bidirectional I/O lines
P1.7/MDY	19	Port 1: quasi-bidirectional I/O line or melody output
P2.0 to P2.3	20, 24 to 26	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	21	ground
TONE	22	DTMF output
V_{DD}	23	positive supply voltage
P0.0 to P0.7	27, 29 to 32, 2 to 4	Port 0: 8 quasi-bidirectional I/O lines or wake-up interrupts
n.c.	1, 13, 17, 28	not connected

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6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.4). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.Their frequencies are provided in purely sinusoidal form on the TONE output or as square waves on the P1.7/MDY output.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

In case no tones are generated, or the melody function is used, the TONE output is in tri-state mode.

6.1 Frequency generator derivative registers

6.1.1 High and Low Group Frequency registers

Table 3 gives the derivative addresses, mnemonics and access types of the frequency generator derivative registers HGF (High Group Frequency) and LGF (Low Group Frequency); access type W.

Table 3 Addresses of the frequency generator derivative registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
11H	HGF	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 Melody and Port Interrupt Control Register (MDYCON)

The Melody and Port Interrupt Control Register has two functions: bit 0 defines the behaviour of the melody output; bits 4 to 7 individually enable/disable specific pairs of Port 0 interrupts. MDYCON is a R/W register.

Table 4 Melody and Port Interrupt Control Register (address 13H)

7	6	5	4	3	2	1	0
EPI3	EPI2	EPI1	EPI0	0	0	0	EMO

Table 5 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 4	EPI3 to EPI0	Enable Port 0 interrupts. Bits 7 to 4 individually enable/disable specific pairs of Port 0 interrupts; see Table 6 and Section 8.2 for details.
3 to 1	–	These bits are set to a logic 0.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line and the TONE output is enabled. If bit EMO = 1, then P1.7/MDY is the melody output and the TONE output is disabled (tri-state). EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the logic HIGH state.

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Table 6 Port 0 Interrupts control bits

BIT	STATE	INTERRUPTS			
		P0.0 AND P0.1	P0.2 AND P0.3	P0.4 AND P0.5	P0.6 AND P0.7
EPI0	1	enabled	–	–	–
	0	disabled	–	–	–
EPI1	1	–	enabled	–	–
	0	–	disabled	–	–
EPI2	1	–	–	enabled	–
	0	–	–	disabled	–
EPI3	1	–	–	–	enabled
	0	–	–	–	disabled

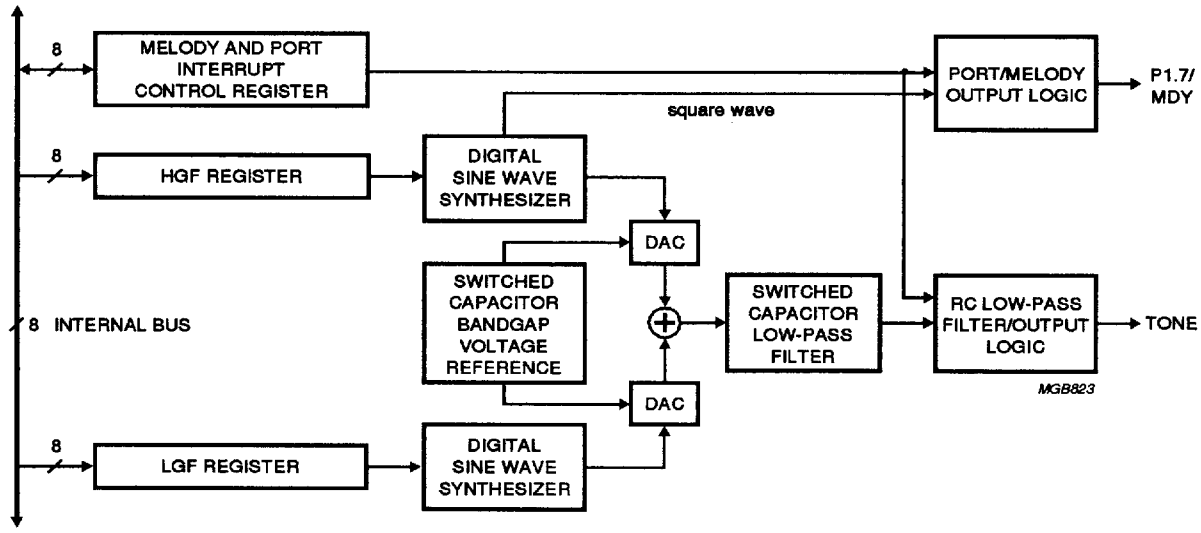

Fig.4 Block diagram of the frequency generator and melody output (P1.7/MDY) section.

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6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

If bit EMO = 1 in the Melody and Port Interrupt Control Register the TONE output is disabled (tri-state) and a square wave with the frequency defined by the HGF contents is output on line P1.7/MDY. The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 3). However, even higher frequency notes may be produced since the limitation $60 \leq x \leq 255$ is relaxed to $2 \leq x \leq 255$ in this application; x = decimal value of the HGF register contents. Due to the low-pass filters, the simultaneous signal on the TONE output is not useful for $x < 60$.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY; see Chapter 14, Table 25.

6.3 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves.

Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature.

The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave. The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated is dependent upon the decimal value 'x' held in the frequency registers (HGF and LGF), and this may be calculated as follows:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]}; \text{ where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

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6.4 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 7.

The relationship between telephone keyboard symbols and the frequency register contents are given in Table 8.

Table 7 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 8 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.5 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequency pairs summarized in Table 9 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 9 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

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6.6 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 10). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low Group Frequency generation.

Table 10 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD3756x types have 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM relies on the fact that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase access complements the read and write accesses in an EEPROM.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses take 5 ms each. To make these operations more efficient, several provisions are available in the PCD3756x.

First, the EEPROM array is structured into 32 four-byte pages (see Fig.5) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes. Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. Besides for EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

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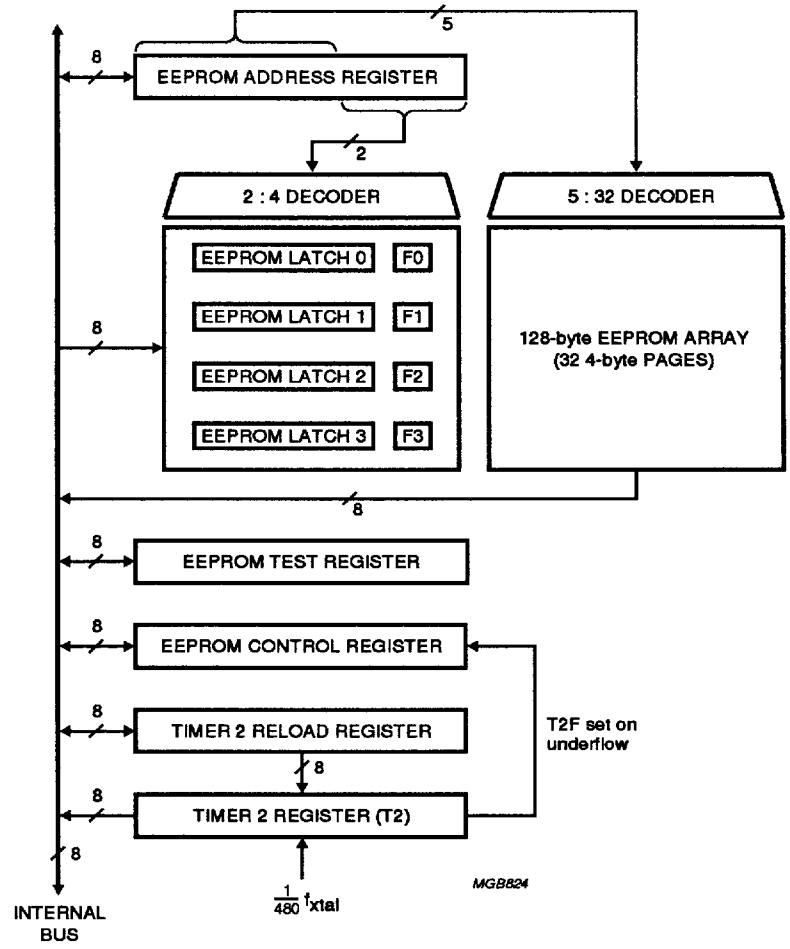

Fig.5 Block diagram of the EEPROM and Timer 2.

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7.1 EEPROM registers

7.1.1 EEPROM CONTROL REGISTER (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. The register access type is R/W.

Table 11 EEPROM Control Register (address 04H)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 12 Description of EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 13.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 13 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

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7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed. The register access type is R/W.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 14 EEPROM Address Register (address 01H)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 15 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 13) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 16 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 17 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.5) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

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7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.5) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.5) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 24). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the SIO/derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 11.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 14), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.5) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.5) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect. Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 18).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 13) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 19.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

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From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 18 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 19 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 20 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 21.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 21 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 22 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

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7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 23 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $1/480 \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $1/480 \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 24 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 24 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE[1] (HEX)
1	0A
2	14
3.58	25
6	3E
10	68
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times 1/480 \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer Register T2 (see Table 27) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

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8 INTERRUPTS

8.1 Derivative Interrupt

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 11 and 12).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

8.2 Port 0 Wake-up Interrupts

In addition to the external interrupt CE, the PCD3756x contains 8 level-sensitive external interrupt sources on Port 0. This function generates an interrupt request if any of the enabled lines of Port 0 (P0.0 to P0.7) is pulled LOW. Like the external interrupt (and contrary to the derivative interrupt) the Port 0 interrupt operates also in Stop mode and forces the CPU to exit the Stop mode.

The Port 0 Wake-up interrupts are controlled by the Enable Port 0 Interrupt bits EPI3 to EPI0 in the Melody and Port Interrupt Control Register MDYCON. Pairs of Port 0 interrupts are individually enabled/disabled via bits 4, 5, 6 and 7. For details see Section 6.1.2. As the Port 0 interrupt is directly linked to the external interrupt, it uses the same flag (EIF), enable instructions (EN I, DIS I) and interrupt vector.

A Port 0 Wake-up interrupt is serviced if:

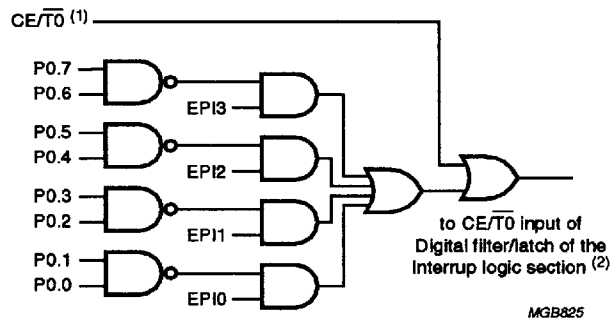
- No interrupt routine is in progress
- The external interrupt is enabled
- It's corresponding enable bit in register MDYCON is set to a logic 1.

If a Port 0 interrupt is to be used, the port flip-flop must first be set to a logic 1 (set to input mode) before it's corresponding EPIn bit is set.

If only a portion of the Port 0 interrupts are used, the remaining port lines may still be used as normal I/O.

In order to configure an I/O as an input, a logic 1 must first be written to it. If a logic 0 is written to one of these port lines (e.g. ANL P0, 00H) while it's corresponding interrupt is enabled, a Port 0 interrupt will be generated.

For more details see data sheet *"PCD33XXA Family; Section External Interrupt"*.



(1) From pin CE/T0.
(2) See the *"PCD33XXA Family"* data sheet.

Fig.6 Simplified External/Port 0 interrupt structure.

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9 TIMING

Although the PCD3756x types operate over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33XXA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode.

This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{T0}$, Timer 2 proceeds from the held state.

The Port 0 Wake-up interrupt function remains operative during Stop mode (depending only on the EPIn bits in register MDYCON). In addition to the description in the *"PCD33XXA Family"* data sheet, Stop mode may be left by a Port 0 Wake-up interrupt event (see Section 8.2).

13 INSTRUCTION SET RESTRICTIONS

RAM space is restricted to 128 bytes, care should be taken to avoid accesses to non-existing RAM locations.

14 OVERVIEW OF FAMILY MEMBERS

Table 25 Port and Power-on-reset configuration

See notes 1 and 2.

TYPE	PORT 0								PORT 1								PORT 2				V_{POR}
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	
PCD3756A	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1R	1R[3]	2S	2S	2S	2S	1.3 V

Notes

1. Port output drive:1 = standard I/O; 2 = open-drain I/O, see *"PCD33xxA Family"* data sheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).
3. The melody output drive type is push-pull.

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15 OTP PROGRAMMING

The programming of the PCD3755x and PCD3756x OTPs is based on the OM4260 programmer (Ceibo MP-51), available from Philips. The OM4260 works in conjunction with various adapters supporting the different package types available as listed in Table 26.

The low-voltage OTP program memory used is of Anti-Fuse-PROM type and can not be erased after programming.

Thus, the complete OTP memory cannot be tested by the factory, but only partially via a special test array. The average expected yield is 97%.

Detailed information on the OTP programming is available in the *"PCD3755x Application Note"*, being available via your Philips Sales office.

Table 26 OTP programming overview

DEVICE	PHILIPS TYPE NUMBER	CEIBO TYPE NUMBER	SUPPORTED PACKAGE
Ceibo MP-51	OM4260	MP-51 programmer base	–
PCD3755x/56x	OM5007	PCD3755A/56A adapter DIP	DIP28
PCD3755x/56x	OM5030	PCD3755A/56A adapter SO	SO28
PCD3755x/56x	OM5037[1]	PCD3755A/56A adapter QFP32	LQFP32

Note

1. As the OM5037 is only a socket converter, the OM5007 is also needed to program the PCD3755x/56x in the LQFP32 package.

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16 SUMMARY OF DERIVATIVE REGISTERS

Table 27 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Melody Control Register (MDYCON)	0	0	0	0	0	0	0	EMO	R/W
14 to FF	not used									

17 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	−10	+10	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	−	90	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

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18 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

19 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 8 to 12)						
V_{DD}	supply voltage operating; note 1 RAM data retention in Stop mode		 1.8 1.0	 – –	 6 6	 V V
I_{DD}	operating supply current; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.5	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	2.4	6.0	mA
$I_{DD(ID)}$	supply current Idle mode; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.1	3.4	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 3	–	1.0	5.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C; note 3	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	1	µA
Port outputs (see Figs 13 to 15)						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	–	mA
I_{OH}	HIGH level port pull-up source current	V_{DD} = 3 V; V_O = 2.7 V	−10	−30	–	µA
		V_{DD} = 3 V; V_O = 0 V	–	−140	−300	µA
I_{OH}	HIGH level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	−0.7	−3.5	–	mA
TONE output (see Fig.7; notes 1 and 4)						
V_{HGrms}	HGF voltage (RMS)		158	181	205	mV
V_{LGrms}	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		−0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB

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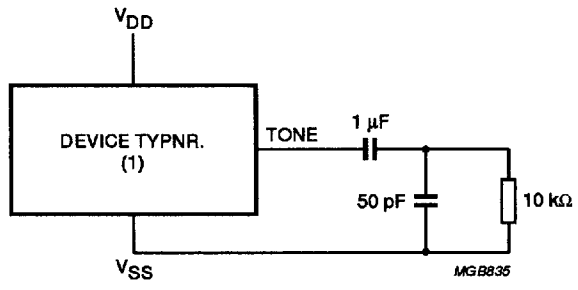
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EEPROM (notes 1 and 6)						
$CY_{t/w}$	endurance (erase/write cycles)	note 7	10^5	–	–	
t_{ret}	data retention time		10	–	–	years
Power-on-reset						
V_{POR}	Power-on-reset level PCD3756A		0.8	1.3	1.8	V

Notes

1. TONE output, EEPROM erase and write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/T0 at V_{SS}; crystal connected between XTAL1 and XTAL2; pins T1 and CE/$\overline{T0}$ at V_{SS}.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is a logic 1, but this cannot be guaranteed after board assembly.
7. Verified on sampling basis.



(1) Device typenr.: PCD3756x.

Fig.7 TONE output test circuit.

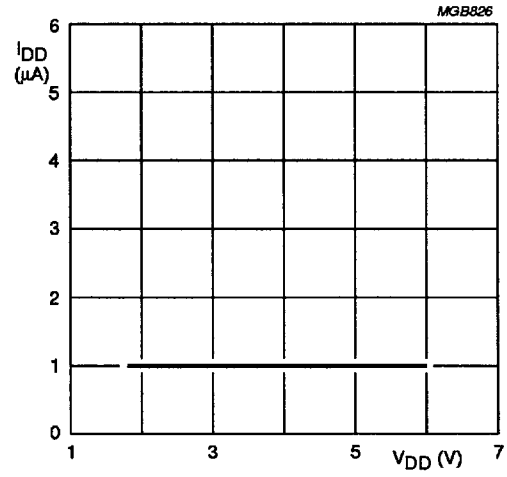


Fig.8 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).

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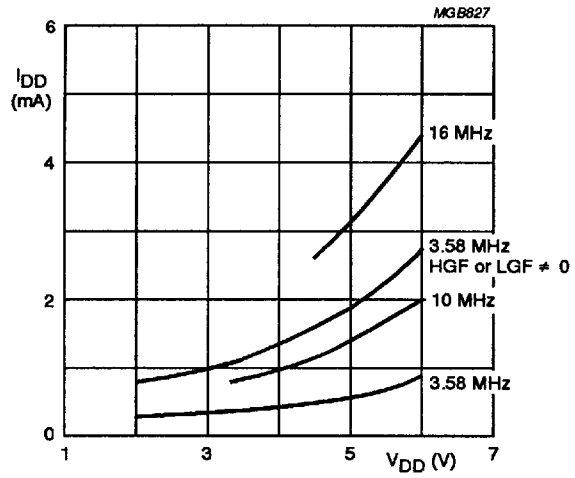
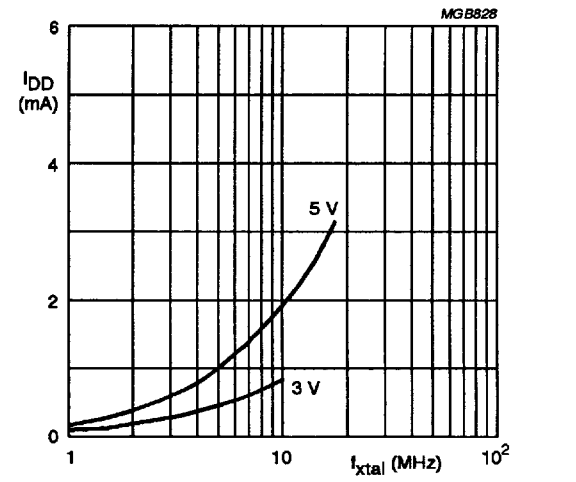


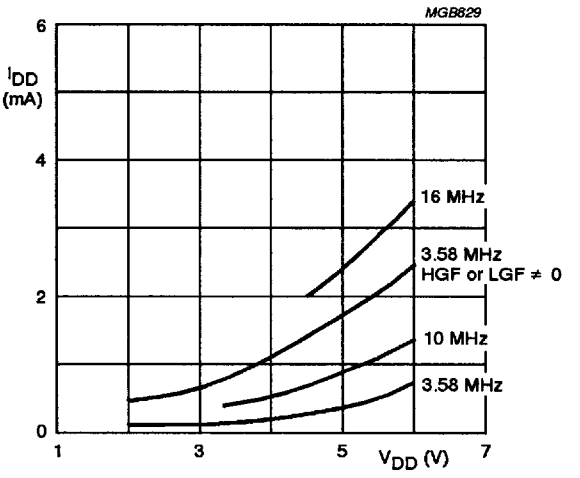
Measured with crystal between XTAL1 and XTAL2.

Fig.9 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



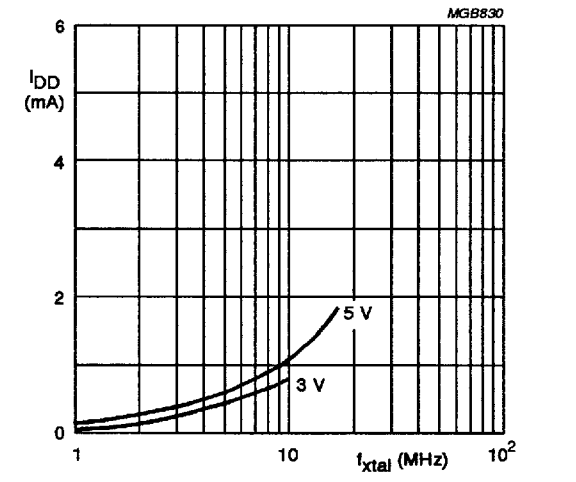
Measured with function generator on XTAL1.

Fig.10 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



Measured with crystal between XTAL1 and XTAL2.

Fig.11 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.12 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).

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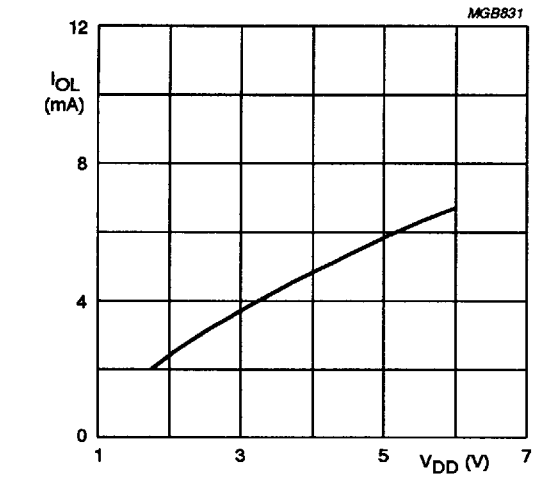


V_O = 0.4 V.

Fig.13 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

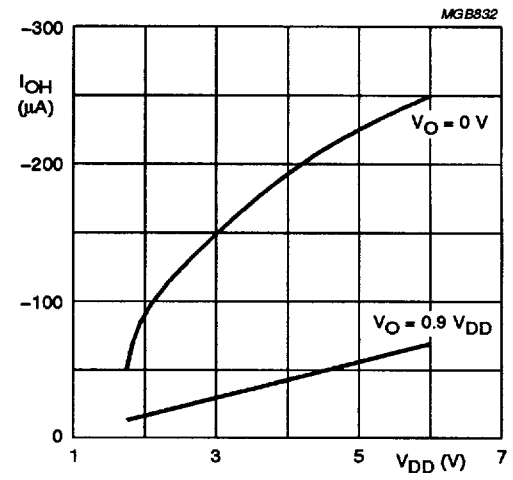
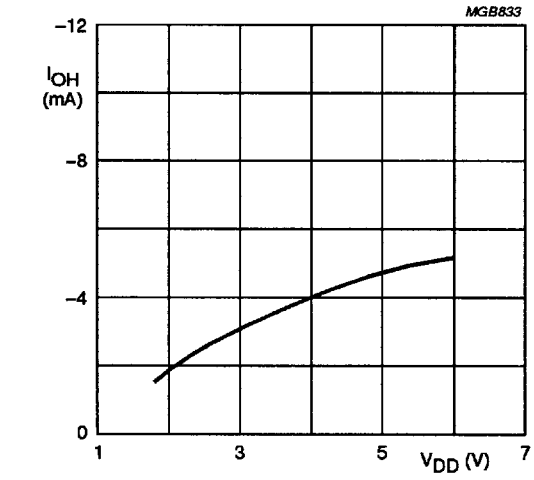


Fig.14 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.15 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

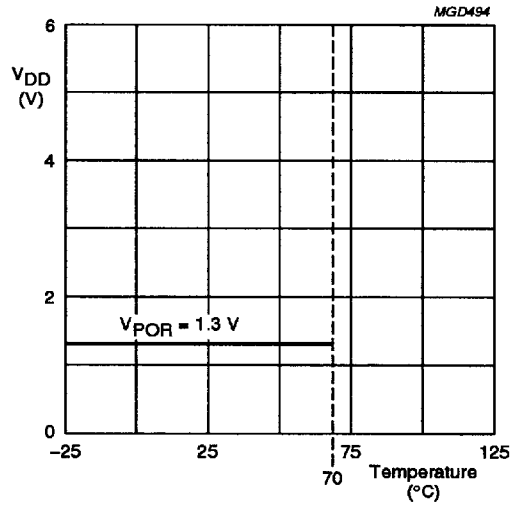


Fig.16 Typical Power-on-reset level (V_{POR}) as function of temperature.

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20 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.17	1	–	16	MHz
Oscillator (see Fig.18)						
g_m	transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

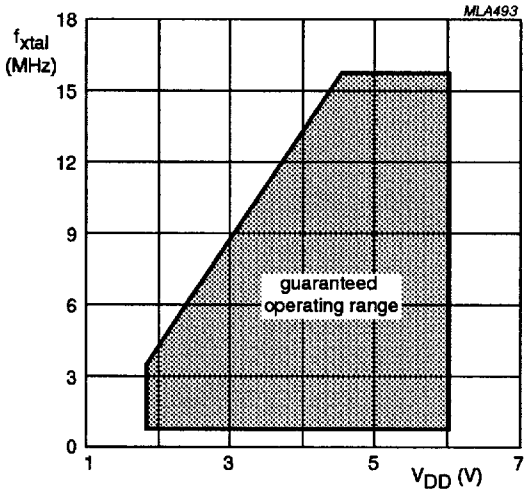

Fig.17 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

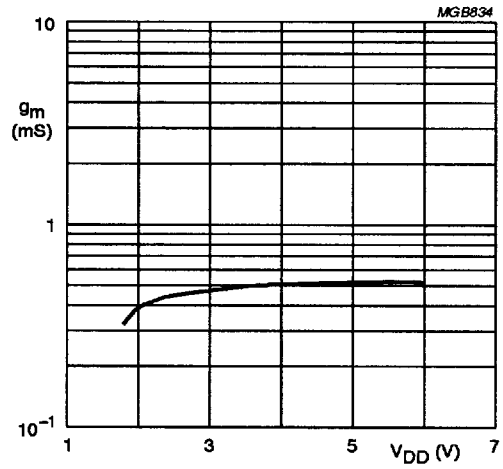

Fig.18 Typical transconductance as a function of supply voltage (V_{DD}).

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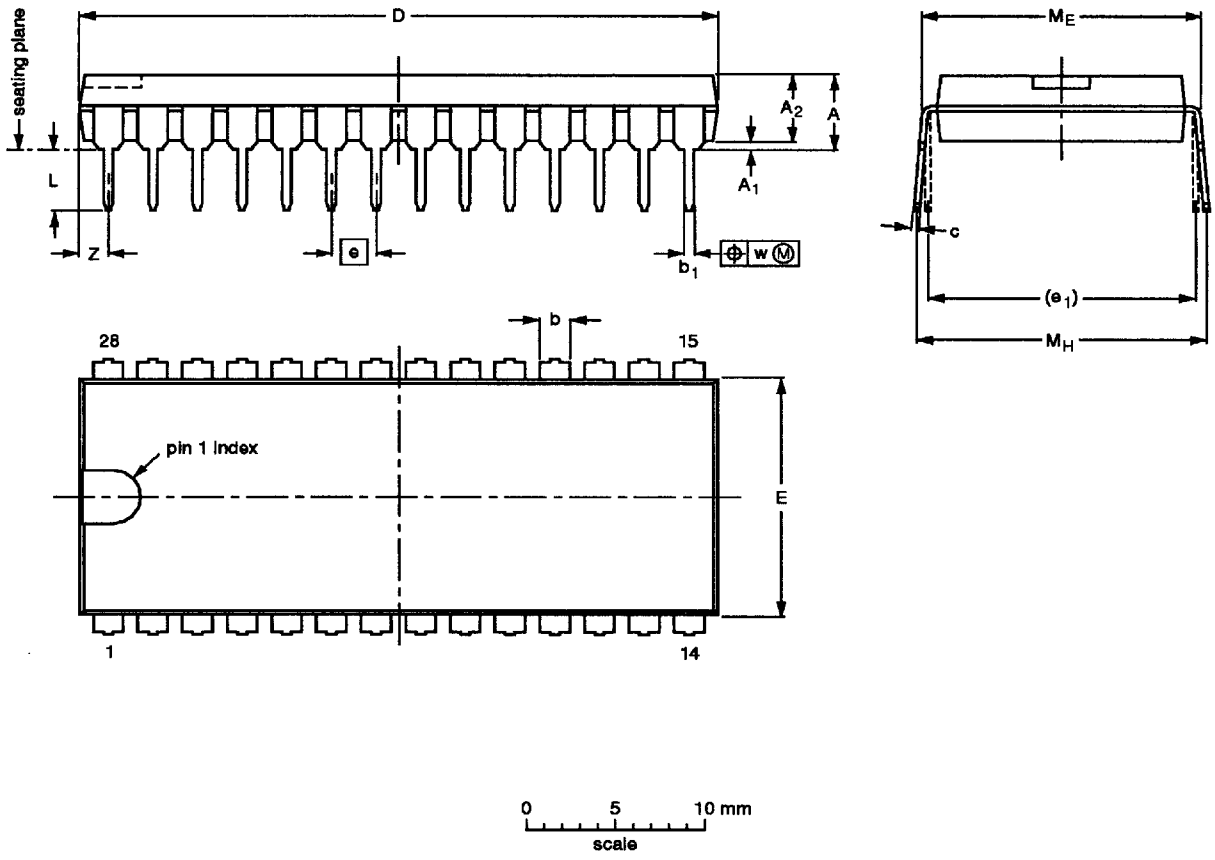
21 PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

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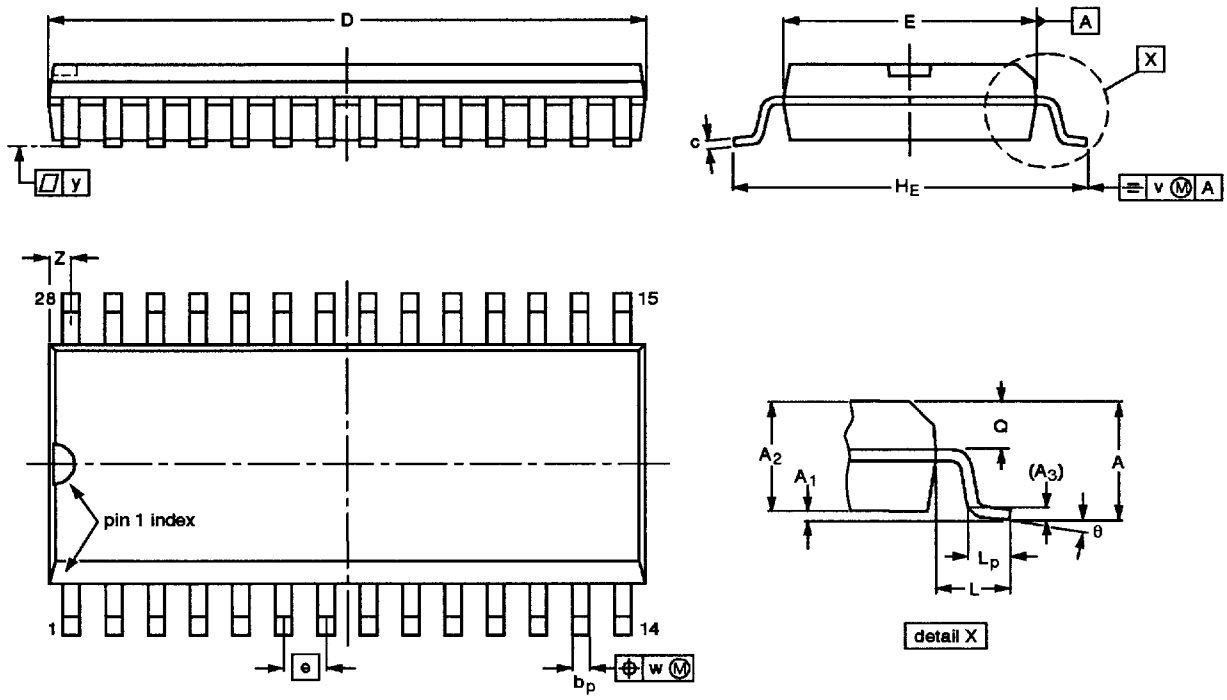
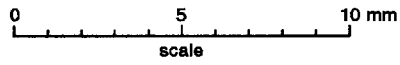
SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

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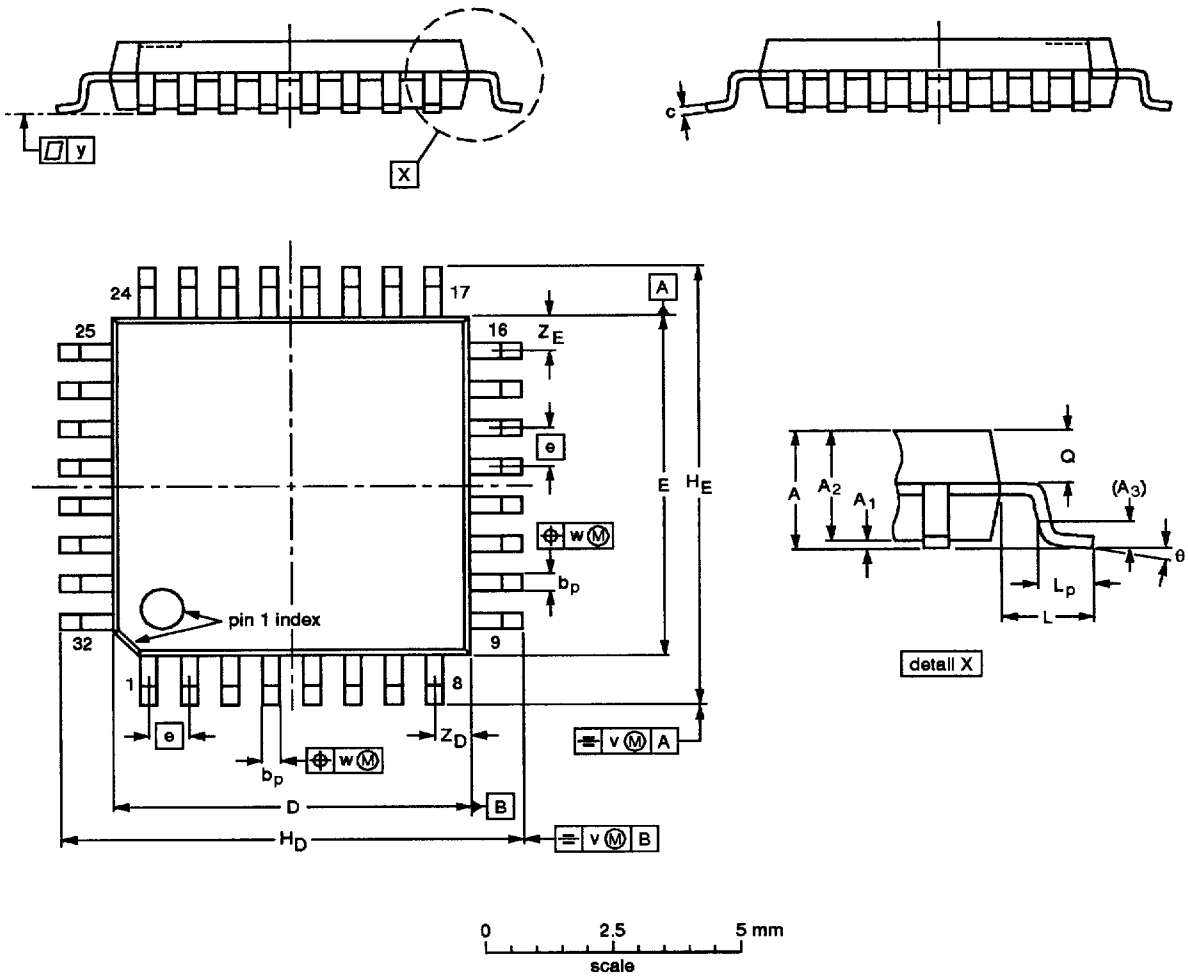
LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358-1						~~93-06-29~~ 95-12-19

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22 SOLDERING

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

22.1 Reflow soldering

Reflow soldering techniques are suitable for all LQFP and SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 mins at 45 °C.

22.2 Wave soldering

22.2.1 LQFP

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP32 (SOT401-1), LQFP48 (SOT313-2), LQFP64 (SOT314-2 and SOT414-1), LQFP80 (SOT315-1) or LQFP100 (SOT407-1).

22.2.2 SO

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

22.2.3 METHOD (LQFP AND SO)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

22.3 DIP

22.3.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

22.4 Repairing soldered joints

Fix LQFP and SO by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

For DIP, apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

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