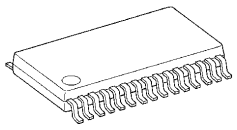
CMOS 8-Bit Microcontroller

TMP86C408DM, TMP86C808DM

The TMP86C408/808 are high speed and high performance 8-bit single chip microcomputers with small package. The MCU contain CPU core, ROM, RAM, multirole timer counter, SEI and UART, 8-bit AD converter, and two clock generators on a chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP86C408DM	4 K × 8 bits	256 × 8 bits	P-SSOP30-56-0.65	TMP86P808DM
TMP86C808DM	8 K × 8 bits			

P-SSOP30-56-0.65



TMP86C408DM
TMP86C808DM

Features

- 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.25 μs (fc = 16 MHz)
  122 μs (fs = 32.768 kHz)
- 132 types and 731 basic instructions
- Interrupt sources: 18 factors (External: 5, Internal: 13)
- Input/Output ports: 24 pins
- 16-bit timer/counter: 1 ch
  - Timer, PPG output, Pulse width measurement, Pulse duty measurement, Event counter
- 8-bit timer/counter: 2 ch
  - Timer, PDO output, Event counter, PWM output, PPG modes
- Time Base Timer
- Divider output function
- Watchdog Timer
  - Interrupt source/Internal Reset (programmable)

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
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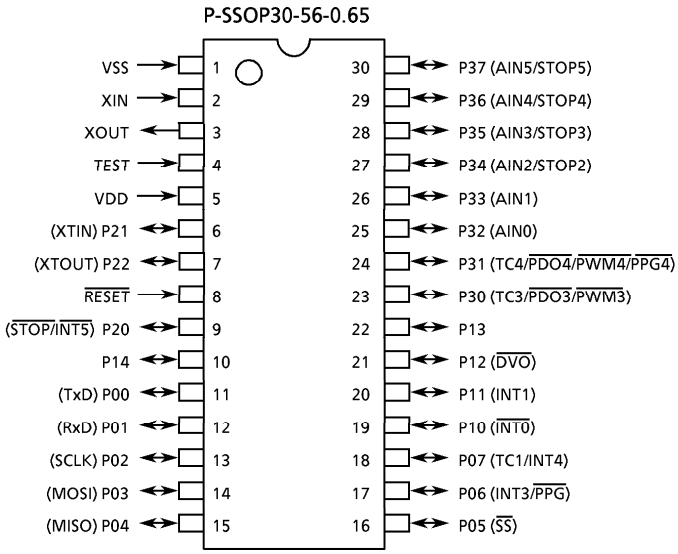
- The information contained herein is subject to change without notice.

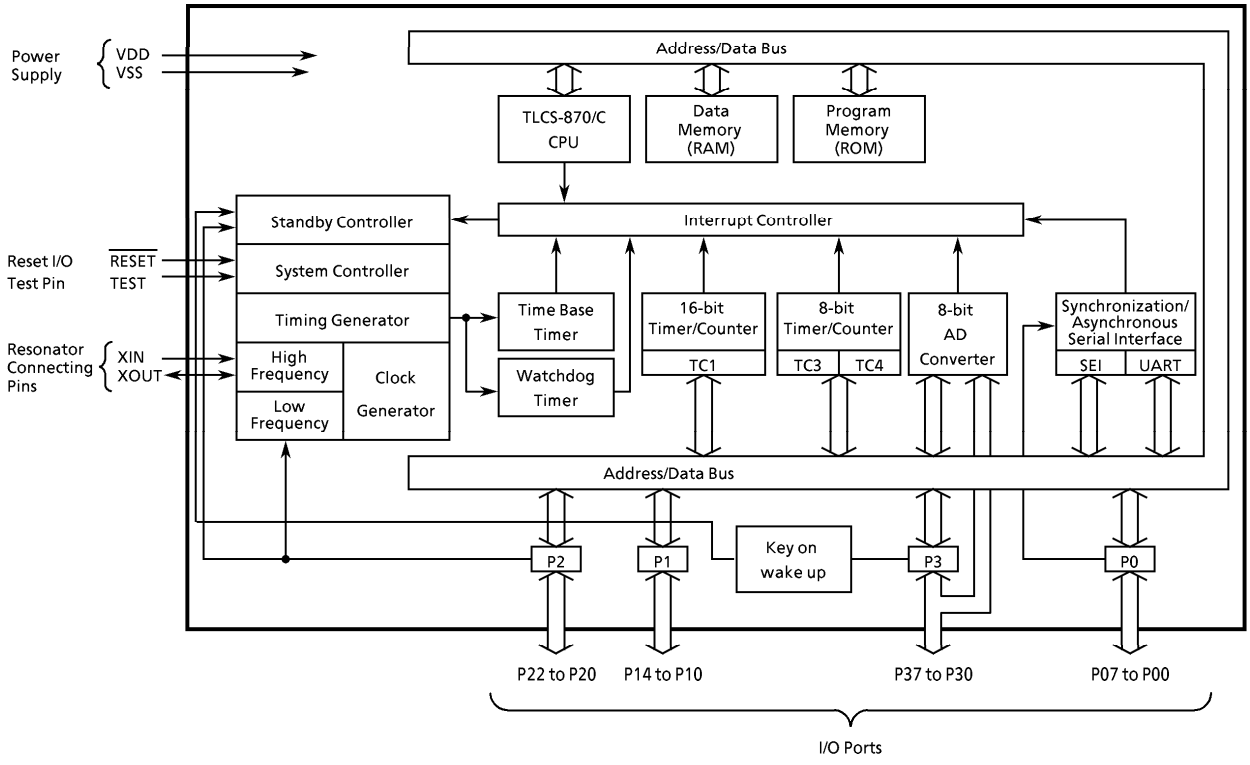
- Serial interface
  - SEI (MSB/LSB Max: 4 Mbps at 16 MHz)
  - 8-bit UART: 1ch
- 8-bit successive approximate type AD converter
  - Analog input: 6 ch
- Key-On Wake-Up: 4 ch
- Power saving operating modes (9 modes)
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
  - SLOW 1 mode: Low power consumption operation using low-frequency clock (High-frequency stop)
  - SLOW 2 mode: Low power consumption operation using low-frequency clock (High-frequency run)
  - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by INTTBT interrupt.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interrupts.
  - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
  - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer. Release by INTTBT interrupt.
  - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
  - SLEEP 2 mode: CPU stops, and peripherals operate using high and low-frequency clock. Release by interrupts.
- Dual clock operation
- Wide operating voltage: 2.7 to 5.5 V at 8 MHz/32.768 kHz,
  4.5 to 5.5 V at 16 MHz/32.768 kHz

Pin Assignments (Top View)

P-SSOP30-56-0.65



Block Diagram



Pin Function

Pin Name	Input/Output	Function		
P07 (TC1, INT4)	I/O (I/O)	8-bit programmable input/output ports. Each bit of these ports can be individually configured as an input or output under software control. When used as function, the latch must be set to 1. Nch O.D output function.	Timer/Counter 1 input/External interrupt input 4	
P06 (INT3, $\overline{PPG}$)	I/O (I/O)		External interrupt input 3/$\overline{PPG}$ output	
P05 ($\overline{SS}$)	I/O (Input)		SEI master slave change input	
P04 (MISO)	I/O (I/O)		SEI master input, slave output	
P03 (MOSI)	I/O (I/O)		SEI master output, slave input	
P02 (SCLK)	I/O (I/O)		SEI serial clock input/output pin	
P01 (RxD)	I/O (Input)		UART data input	
P00 (TxD)	I/O (Output)		UART data output	
P14	I/O (I/O)	5-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or output under software control. When used as function, the latch must be set to 1.		
P13	I/O (I/O)			
P12 ($\overline{DVO}$)	I/O (Output)		Divider output	
P11 (INT1)	I/O (Input)		External interrupt input 1	
P10 ($\overline{INT0}$)	I/O (Input)		External interrupt input 0	
P22 (XTOUT)	I/O (Output)	3-bit programmable input/output ports. When used as input port and function, the latch must be set to 1.	Resonator connecting pins (32.768 kHz) For inputting external clock, XTIN is used and XTOUT is opened.	
P21 (XTIN)	I/O (Input)			
P20 ($\overline{INT5}$, $\overline{STOP5}$)	I/O (Input)		External interrupt input 5 or STOP mode release signal input	
P37 (AIN5, STOP5)	I/O (Input)	8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or output under software control. When used as function and analog inputted latch must be set to 1.	STOP mode release signal input 5	AD converter analog input
P36 (AIN4, STOP4)	I/O (Input)		STOP mode release signal input 4	
P35 (AIN3, STOP3)	I/O (Input)		STOP mode release signal input 3	
P34 (AIN2, STOP2)	I/O (Input)		STOP mode release signal input 2	
P33 (AIN1)	I/O (Input)			
P32 (AIN0)	I/O (Input)			
P31 (TC4, $\overline{PDO4}$, $\overline{PWM4}$, $\overline{PPG4}$)	I/O (I/O)		Timer/Counter 4 input, $\overline{PDO}$, $\overline{PWM}$, $\overline{PPG}$ output	
P30 (TC3, $\overline{PDO3}$, $\overline{PWM3}$)	I/O (I/O)		Timer/Counter 3 input, $\overline{PDO}$, $\overline{PWM}$ output	
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.		
$\overline{RESET}$	Input	RESET signal input		
TEST	Input	TEST pin for out-going test. Be fixed to low.		
VDD, VSS	Power Supply	+ 5 V, 0 (GND)		

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86C408/808 memory consist of 3 blocks: ROM, RAM and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86C408/808 memory address map. The general-purpose register banks are not assigned to the RAM address space.

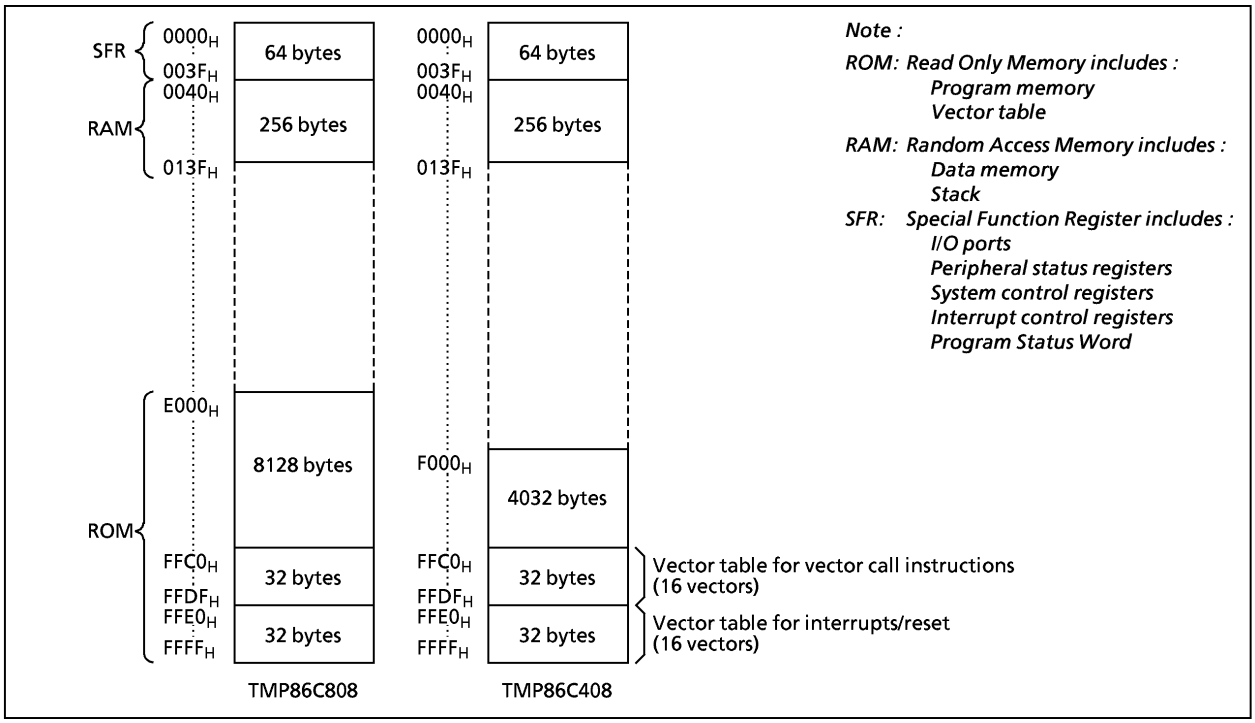


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86C408 has a 4 K×8 bits (address $F000_H$ to $FFFF_H$), TMP86C808 has a 8 K×8 bits (address $E000_H$ to $FFFF_H$) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address Trap).

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT1}	P21, P22, $\overline{RESET}$, Tri-state Port	– 0.3 to V_{DD} + 0.3	
	V_{OUT2}	P20, Sink Open Drain Port	– 0.3 to 5.5	
Output Current (Per 1 pin)	I_{OUT1} I_{OH}	P0, P1, P3 Port	– 1.8	mA
	I_{OUT2} I_{OL}	P1, P2, P3 Port	3.2	
	I_{OUT3} I_{OL}	P0 Port	30	
Output Current (Total)	ΣI_{OUT1}	P0, P1, P3 Port	– 30	
	ΣI_{OUT2}	P1, P2, P3 Port	60	
	ΣI_{OUT3}	P0 Port	80	
Power Dissipation [T_{opr} = 85°C]	PD		145	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 150	
Operating Temperature	Topr		– 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE0, 1, 2 mode			
			fc = 8 MHz	NORMAL1, 2 mode	2.7		
				IDLE0, 1, 2 mode			
			fs = 32.768 kHz	SLOW1, 2 mode			
				SLEEP0, 1, 2 mode			
				STOP mode			
Input high Level	V_{IH1}	Except Hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input low Level	V_{IL1}	Except Hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 2.7 to 5.5 V		1.0	8.0	MHz
			V_{DD} = 4.5 to 5.5 V			16.0	
	fs	XTIN, XTOUT	V_{DD} = 2.7 to 5.5 V		30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Standard

DC Characteristics (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tri-state Port					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN1}	TEST Pull-Down		–	70	–	kΩ
	R_{IN2}	$\overline{RESET}$ Pull-Up		100	220	450	
Output Leakage Current	I_{LO}	Sink Open Drain, Tri-state Port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	± 2	μA
Output High Voltage	V_{OH}	P0, P1, P3 Port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	P1, P2, P3 Port	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	
Output Low Current	I_{OL}	High Current Port (P0 Port)	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply Current in NORMAL 1, 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3/0.2 V fc = 16.0 MHz fs = 32.768 kHz	–	7.5	9.0	
Supply Current in IDLE 0, 1, 2 mode				–	5.5	6.5	
Supply Current in SLOW 1 mode			V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz	–	14.0	25.0	μA
Supply Current in SLEEP 1 mode				–	7.0	15.0	
Supply Current in SLEEP 0 mode				–	6.0	15.0	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	10.0	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V
Note 2: Input current (I_{IN1}, I_{IN3}); The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} does not include I_{REF} current.
Note 4: The power supply current in STOP2 and SLEEP2 modes each are the same as in IDLE0, 1, and 2 modes.

AD Conversion Characteristics (V_{SS} = 0.0 V, 4.5 V ≦ V_{DD} ≦ 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{DD}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = 5.5 V V_{SS} = 0.0 V	–	0.6	1.0	mA
Non linearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

(V_{SS} = 0.0 V, 2.7 V ≦ V_{DD} < 4.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{DD}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = 4.5 V V_{SS} = 0.0 V	–	0.5	0.8	mA
Non linearity Error		V_{DD} = 2.7 V, V_{SS} = 0.0 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to "2.10.2 Register Configuration".
Note 3: Please use input voltage to AIN input Pin in limit of V_{DD} - V_{SS}.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
Note 4: The relevant pin for I_{REF} is V_{DD}, so that the current flowing into V_{DD} is the power supply current I_{DD} + I_{REF}.

SEI Operating Conditions (Slave mode) (V_{SS} = 0.0 V, 2.7 V ≦ V_{DD} ≦ 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Transfer Rate			15.625 k	–	fc/4	bps

AC Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.25	–	4	μs
		IDLE 0, 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 0, 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 16 MHz	25	–	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	twcL					

(V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V, Topr = – 40 to 85°C)

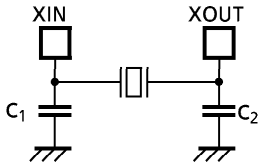
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.5	–	4	μs
		IDLE 0, 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 0, 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	twcL					

Recommended Oscillation Conditions-1 (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = − 40 to 85°C)

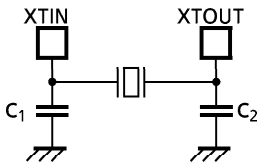
Parameter	Resonator	Oscillating Frequency	Recommended Resonator		Recommended Constant	
					C_1	C_2
High-frequency oscillation	Ceramic resonator	16 MHz	MURATA	CSA16.00MXZ040	10 pF	10 pF
		8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)
Low-frequency oscillation	Crystal resonator	32.768 kHz	SII	VT-200	6 pF	6 pF

Recommended Oscillation Conditions-2 (V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, T_{opr} = − 40 to 85°C)

Parameter	Resonator	Oscillating Frequency	Recommended Resonator		Recommended Constant	
					C_1	C_2
High-frequency oscillation	Ceramic resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.

Note 2: To ensure stable oscillation, the resonator position, load capacitance, etc. must be appropriate. Because there factors are greatly affected by board patterns, please be sure to evaluate operation on the board on which the device will actually be mounted.

Note 3: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
http://www.murata.co.jp/search/index.html