

MITSUBISHI LSIs

**M58659P****512-BIT(32-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM**

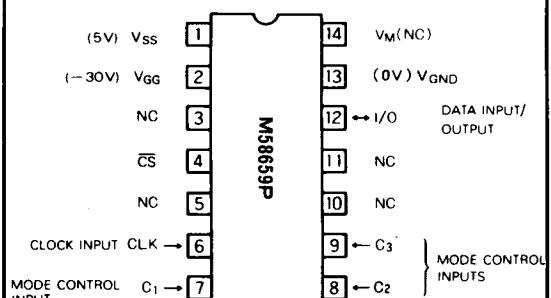
## DESCRIPTION

The M58659P is a serial input/output 512 bit electrically erasable and reprogrammable ROM organized as 32 words of 16 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

## FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . . 10 years (min)
- Write/erase time . . . . . 20ms word
- Typical power supply voltages . . . . . -30V, +5V
- Number of erase-write cycles . . . . .  $10^5$  times (min)
- Number of read access unrefreshed. . .  $10^9$  times (min)
- 5V I/O interface

## PIN CONFIGURATION (TOP VIEW)

**Outline 14P4**

NC: NO CONNECTION

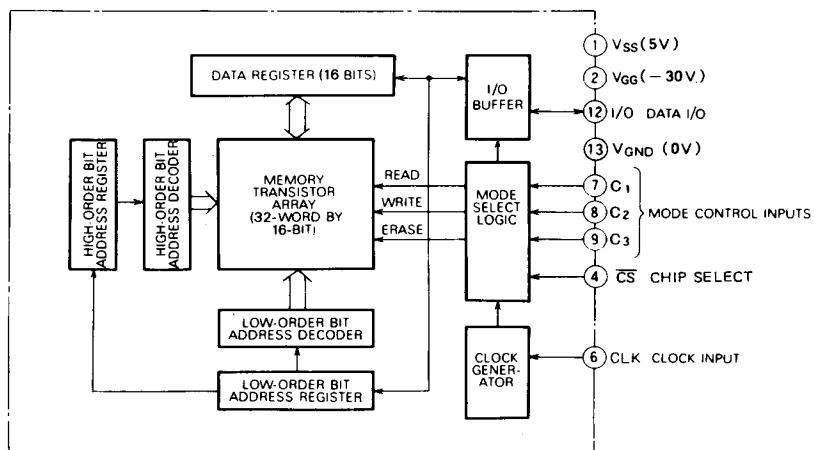
## APPLICATION

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

## FUNCTION

The address is designated by one-of-four and one-of-eight coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C<sub>1</sub>, C<sub>2</sub>, and C<sub>3</sub>. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO<sub>2</sub>—Si<sub>3</sub>N<sub>4</sub> interface of the gate insulators of the MNOS memory transistors.

## BLOCK DIAGRAM



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**PIN DESCRIPTION**

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input. In the shift data output mode, used for output In the standby, read, erase and write modes, this pin is in a floating state
V <sub>M</sub>	Test	Used for testing purposes only. It should be left unconnected during normal operation
V <sub>SS</sub>	Chip substrate voltage	Normally connected to +5V
V <sub>GG</sub>	Power supply voltage	Normally connected to -30V
CLK	Clock input	Required for all operating modes, when CS is low
C <sub>1</sub> ~ C <sub>3</sub>	Mode control input	Used to select the operation mode
V <sub>GND</sub>	Ground voltage	Connected to ground (0V)
CS	Chip select	Used for chip selection in "L"

**OPERATION MODES**

C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	Functions
H	H	H	Standby mode. The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state
H	H	L	Not used
H	L	H	Erase mode. The word stored at the addressed location is erased. The data bits after erasing are all low-level
H	L	L	Accept address mode. Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by one-of-four and one-of-eight-coded digits. 32-word address is assigned in this mode.
L	H	H	Read mode. The addressed word is read from the memory into the data register
L	H	L	Shift data output mode. The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse
L	L	H	Write mode. The data contained in the data register is written into the location designated by the address registers
L	L	L	Accept data mode. The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>GG</sub>	Supply voltage	With respect to V <sub>SS</sub>	0.3 ~ -40	V
V <sub>I</sub>	Input voltage		0.3 ~ -20	V
V <sub>O</sub>	Output voltage		0.3 ~ -20	V
T <sub>stg</sub>	Storage temperature		-40 ~ 125	°C
T <sub>opr</sub>	Operating temperature		-10 ~ 70	°C

**RECOMMENDED OPERATING CONDITIONS** (T<sub>a</sub> = -10 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>GG</sub> -V <sub>SS</sub>	Supply voltage	-32.2	-35	-37.8	V
V <sub>SS</sub> -V <sub>GND</sub>	Supply voltage	4.75	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>SS</sub> -1		V <sub>SS</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage	V <sub>SS</sub> -6.5		V <sub>SS</sub> -4.25	V

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**ELECTRICAL CHARACTERISTICS** (  $T_a = -10 \sim 70^\circ\text{C}$ ,  $V_{GG} - V_{SS} = -35V \pm 8\%$ ,  $V_{SS} - V_{GND} = 5V \pm 5\%$ , unless otherwise noted )

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{IH}$	High-level input voltage		$V_{SS} - 1$		$V_{SS} + 0.3$	V
$V_{IL}$	Low-level input voltage		$V_{SS} - 6.5$		$V_{SS} - 4.25$	V
$I_{IL}$	Low-level input current CLK, C1, C2, C3, I/O	$V_I - V_{SS} = -6.5V$	-10		+10	$\mu\text{A}$
$R_I$	Input pull-up resistance, $\overline{CS}$			30		$\text{k}\Omega$
$I_{OZL}$	Off-state output current, low-level voltage applied	$V_O - V_{SS} = -6.5V$	-10		+10	$\mu\text{A}$
$V_{OH}$	High-level output voltage	$I_{OH} = 200\mu\text{A}$	$V_{SS} - 1$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 80\mu\text{A}$			$V_{GND} + 0.5$	V
$I_{GG}$	Supply current from $V_{GG}$	$I_G = 0\mu\text{A}$		5.5	8.8	mA

Note 1: Typical values are at  $T_a = 25^\circ\text{C}$  and  $V_{GG} - V_{SS} = -35V$ .

**TIMING REQUIREMENTS** (  $T_a = -10 \sim 70^\circ\text{C}$ ,  $V_{GG} - V_{SS} = -35V \pm 8\%$ ,  $V_{SS} - V_{GND} = 5V \pm 5\%$ , unless otherwise noted )

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$T_L(\phi)$	Negative clock pulse width		30			$\mu\text{s}$
$T_H(\phi)$	Positive clock pulse width		33			$\mu\text{s}$
$T(\phi)$	Clock period				300	$\mu\text{s}$
$t_w$	Write time		16	20	24	ms
$t_E$	Erase time		16	20	24	ms
$t_r, t_f$	Risetime, fall time				1	$\mu\text{s}$
$t_{su}$	Control setup time before the fall of the clock pulse		1			$\mu\text{s}$
$t_h$	Control hold time after the rise of the clock pulse		0			$\mu\text{s}$
$t_{ss}$	Clock control setup time before the fall of $\overline{CS}$		1			$\mu\text{s}$
$t_{hs}$	Clock control hold time after the rise of $\overline{CS}$		1			$\mu\text{s}$

**SWITCHING CHARACTERISTICS** (  $T_a = -10 \sim 70^\circ\text{C}$ ,  $V_{GG} = -35V \pm 8\%$ , unless otherwise noted )

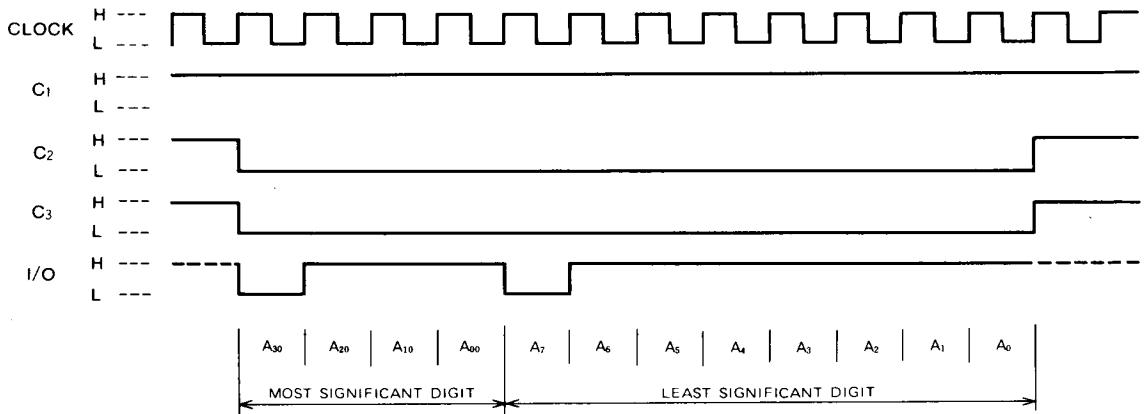
Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{a(c)}$	Read access time	$t_{PW}$	$C_L = 100\text{pF}$ $V_{OH} = V_{SS} - 2V$ $V_{OL} = V_{GND} + 1.5V$			20	$\mu\text{s}$
$t_s$	Unpowered nonvolatile data retention time	$T_s$	$N_{EW} = 10^4$ , $t_{w(w)} = 20\text{ms}$ $t_{w(E)} = 20\text{ms}$	10			Year
		$T_s$	$N_{EW} = 10^5$ , $t_{w(w)} = 20\text{ms}$ $t_{w(E)} = 20\text{ms}$	1			
$N_{EW}$	Number of erase/write cycles	$N_w$		$10^5$			Times
$N_{RA}$	Number of read access unrefreshed	$N_{RA}$		$10^9$			Times
$t_{dv}$	Data valid time	$t_{PW}$				20	$\mu\text{s}$

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**TIMING DIAGRAM**

Accept Address Mode (12 clocks)

CS : L

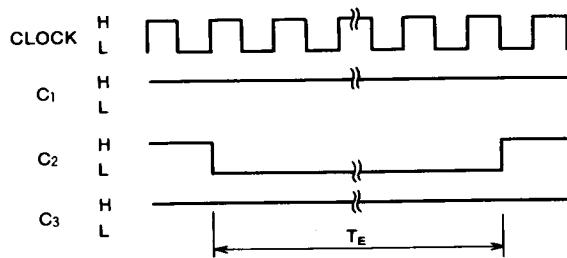


Note 2: The addresses from A<sub>30</sub> to A<sub>37</sub> are designated by one-of-four and one-of-eight coded digits. The above figure shows designation of address A<sub>37</sub>.

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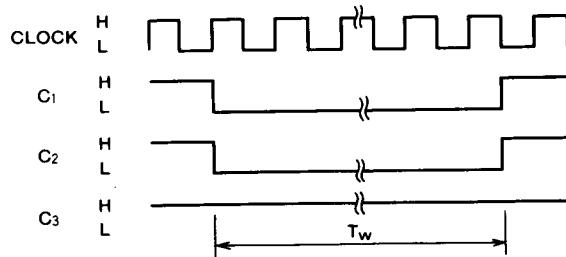
Erase Mode

$\overline{CS} : L$



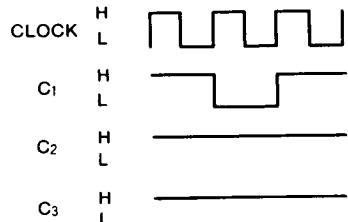
Write Mode

$\overline{CS} : L$



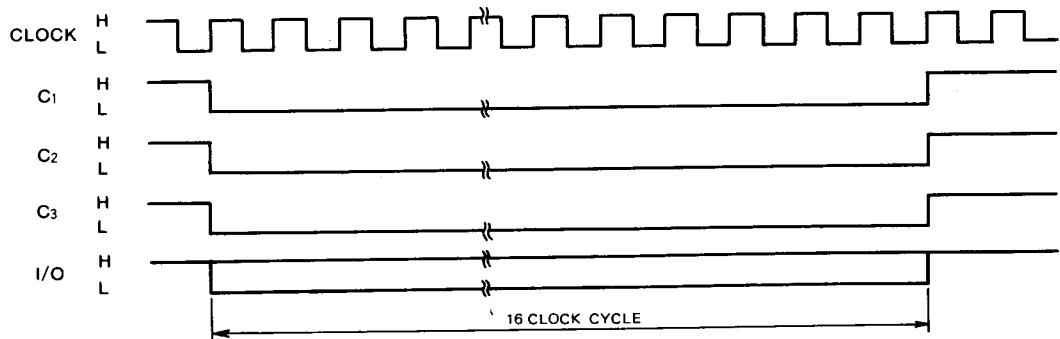
Read Mode (1 clock)

$\overline{CS} : L$



Accept Data (16 clocks)

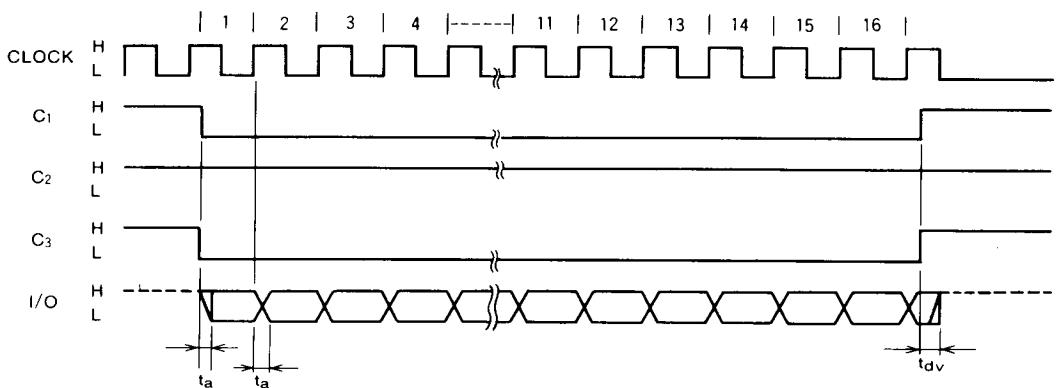
$\overline{CS} : L$



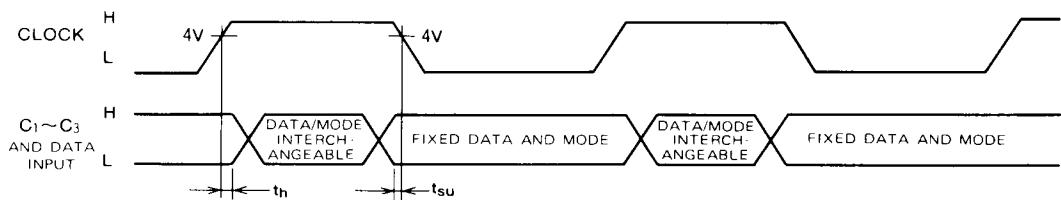
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Shift Data Output Mode (16 clocks)

$\overline{CS} : L$

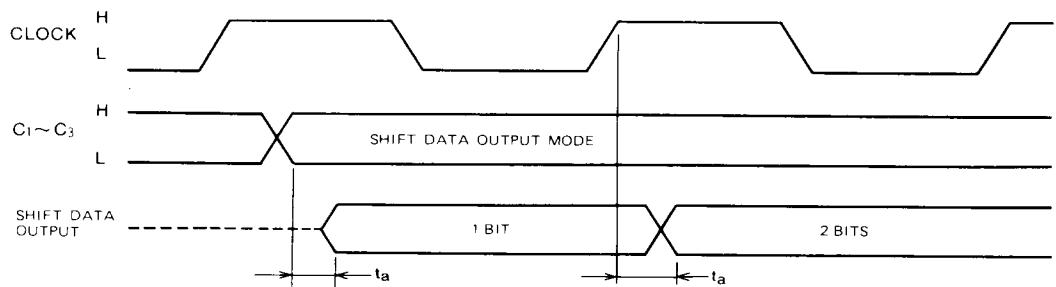


Timing of clock,  $C_1$ ,  $C_2$ ,  $C_3$ , and data input



Note 3  $C_1 \sim C_3$  and accept data are interchangeable while the clock is set high.

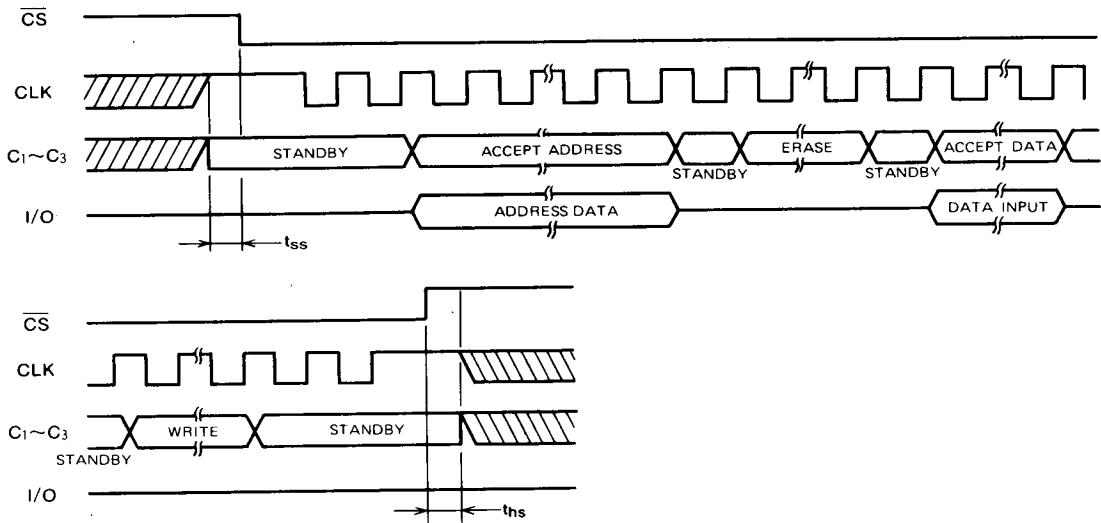
Timing of clock,  $C_1$ ,  $C_2$ ,  $C_3$ , and data input



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Operation flowchart

Rewriting flowchart

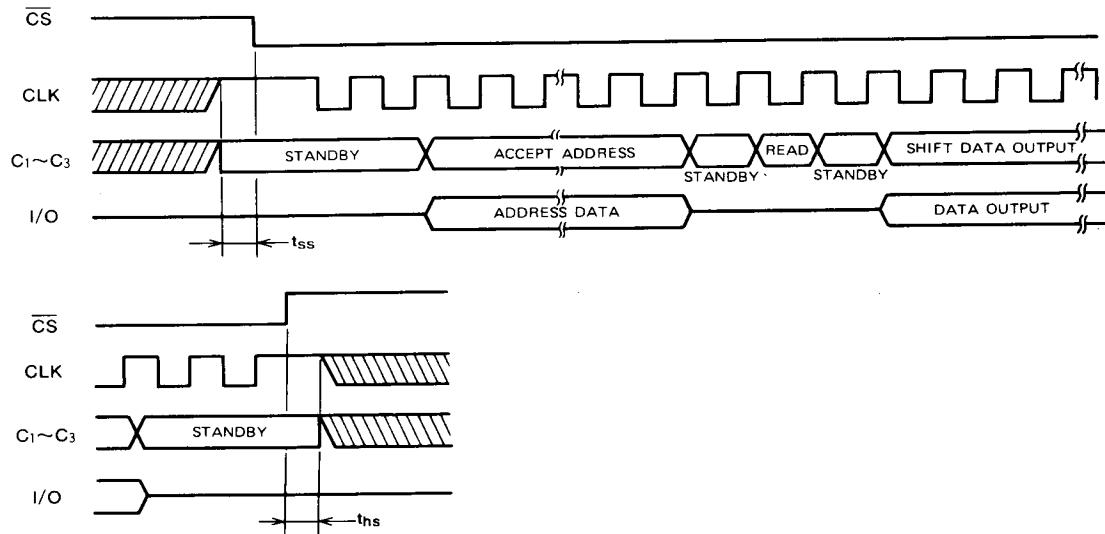


Note 4: One or more clock are required for standby between modes.

5: Set CS to the low level after the lapse of  $t_{ss}$  and CLK has been set high and C<sub>1</sub> ~ C<sub>3</sub> have been set to the standby mode.

6: Keep CLK to the high level and C<sub>1</sub> ~ C<sub>3</sub> to "standby" from the time when CS is set high to the lapse of  $t_{hs}$ .

Read Flowchart



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**Power-on/off Conditions**

With power-on,  $V_{GG}$  is applied after  $V_{SS}$  has been applied. With power-off,  $V_{SS}$  is cut after  $V_{GG}$  has been cut. For power-on and off, hold  $\bar{CS}$  in  $V_{SS}$  or floating state. The recommended timing chart for power-on and off is as follows.

