

FEATURES

- Programmable Supply Current 500nA to 2mA
- Single Supply Operation +3V to +30V
- Dual Supply Operation $\pm 1.5V$ to $\pm 15V$
- Low Input Offset Voltage 100 μV
- Low Input Offset Voltage Drift 0.5 $\mu V/^{\circ}C$
- High Common-Mode Input Range V_- to V_+ ($-1.5V$)
- High CMRR and PSRR 115dB
- High Open-Loop Gain 2000V/mV
- $\pm 30V$ Input Overvoltage Protection
- Fast 1V/ μs @ $I_{SY} = 300\mu A$
- LM4250 Pinout
- Compensated for Minimum Gain of 10
- Available in Die Form

ORDERING INFORMATION [†]

$T_A = 25^{\circ}C$ $V_{OS} \text{ MAX}$ (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	CERDIP 8-PIN	PLASTIC 8-PIN	
300	—	OP32AZ*	MIL
300	OP32EP	OP32EZ	IND
500	OP32FP	OP32FZ	IND
1000	OP32GP	OP32GZ	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[†] Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The OP-32 is a high-speed, high-gain programmable operational amplifier. Both offset voltage and offset current are low, and both are stable with changes in temperature, supply voltage, and set current. High CMRR and PSRR ensure

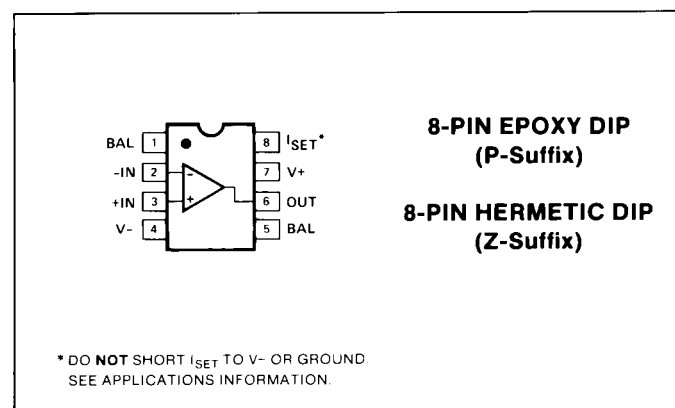
precision performance when the OP-32 is used with an unregulated battery or vehicular electrical system.

The wide input voltage range, including the negative supply or ground, allows use in single-battery applications. The OP-32 is characterized over a wide supply range of $\pm 1.5V$ to $\pm 15V$. This guarantees predictable performance with any commonly available supply.

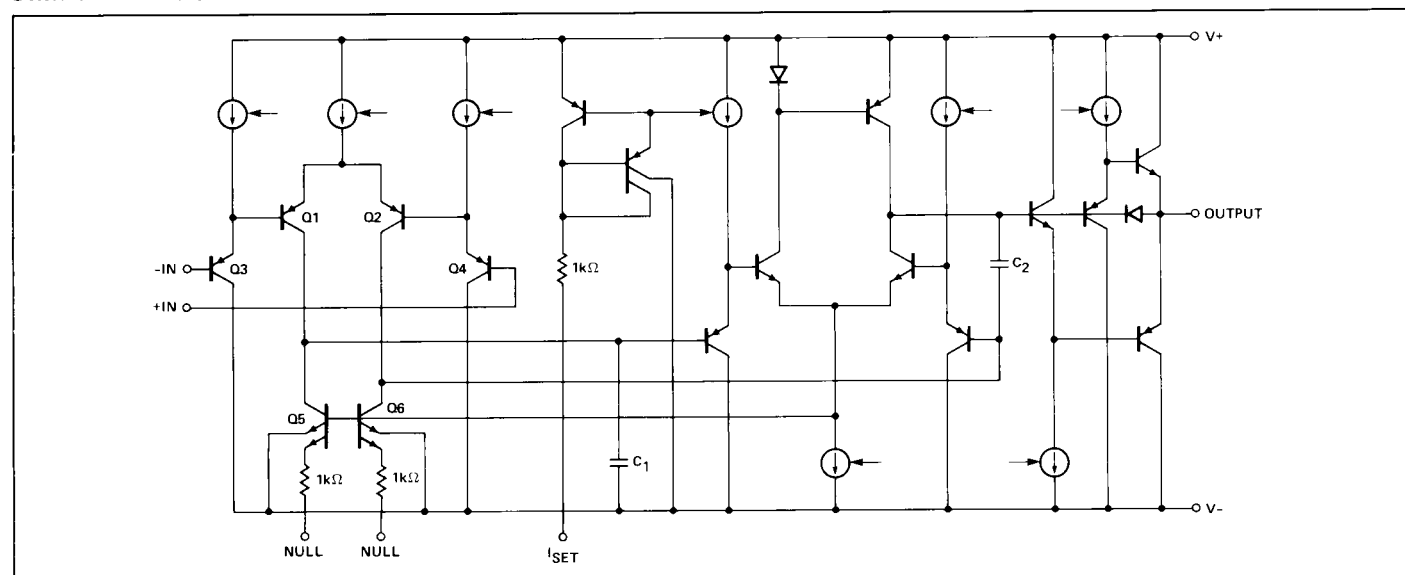
The ability to operate at relatively high speed with low power consumption makes this amplifier ideal for remote applications where power is limited. The programmability allows each amplifier in a system to be set for the minimum power consumption necessary for each specific application. Programmability also makes it possible to adjust the bandwidth and phase shift.

The OP-32 pinout is identical to the LM4250 and many other micropower operational amplifiers. This allows easy upgrading of system performance.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



OP-32

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±18V
Differential Input Voltage	±30
Input Voltage	Supply Voltage
Storage Temperature Range	
Z Package	–65°C to +150°C
P Package	–55°C to +125°C
Operating Temperature Range	
OP-32A	–55°C to +125°C
OP-32E, F, G	–25°C to +85°C

Lead Temperature Range (Soldering, 60 sec)	300°C
Junction Temperature	–65°C to +150°C

PACKAGE TYPE	θ_{JA} (Note 2)	θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32A/E			OP-32F			OP-32G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	100	300	—	200	500	—	400	1000	μV
Input Offset current	I_{OS}	$V_{CM} = 0$	—	—	2	—	—	2	—	—	3	nA
Input Bias Current (Note 1)	I_B	$I_{SY} = 15\mu A$	—	3	5	—	5	7.5	—	5	10	nA
		$I_{SY} = 150\mu A$	—	20	35	—	24	35	—	30	50	
		$I_{SY} = 450\mu A$	—	60	90	—	70	100	—	80	125	
Input Voltage Range	IVR	$V_S = \pm 15V$	–15.0/13.5	—	—	–15.0/13.5	—	—	–15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 2)	CMRR	$V_S = \pm 15V$ $-15V \leq V_{CM} \leq +13.5V$	100	115	—	95	110	—	85	100	—	dB
Power Supply Rejection Ratio (Note 2)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$; and $V_- = 0V$, $V_+ = 3V$ to $30V$.	—	1	6	—	3	12	—	10	25	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	1000	2000	—	750	1500	—	500	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	± 0.8	± 0.88	—	± 0.8	± 0.88	—	± 0.75	± 0.85	—	V
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	± 14	± 14.2	—	± 14	± 14.2	—	± 13.8	± 14.2	—	V
Gain-Bandwidth Product		$I_{SY} = 15\mu A$, $R_L = 100k\Omega$	—	100	—	—	100	—	—	100	—	kHz
		$I_{SY} = 450\mu A$, $R_L = 10k\Omega$	—	4500	—	—	4500	—	—	4500	—	
Slew Rate	SR	$V_S = \pm 15V$, $I_{SY} = 450\mu A$, $R_L = 10k\Omega$	—	1.5	—	—	1.5	—	—	1.5	—	V/ μs
Supply Current No Load (Note 3)	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	15	17	—	15	19	—	15	21	μA
		$I_{SET} = 10\mu A$	—	150	170	—	150	190	—	150	200	
		$I_{SET} = 30\mu A$	—	450	525	—	450	600	—	450	650	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	10.5	12.5	—	11	15	—	11	18	μA
		$I_{SET} = 10\mu A$	—	105	125	—	110	150	—	110	180	
		$I_{SET} = 30\mu A$	—	350	400	—	350	450	—	350	500	

NOTES:

1. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. PSRR and CMRR measured with V_{OS} unnullled and I_{SET} held constant.
3. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V_+) - (V_-)}{6}$$

The range of I_{SY}/I_{SET} is approximately 10.5 to 15 over the specified operating range of $V_S = \pm 1.5V$ to $V_S = \pm 15V$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

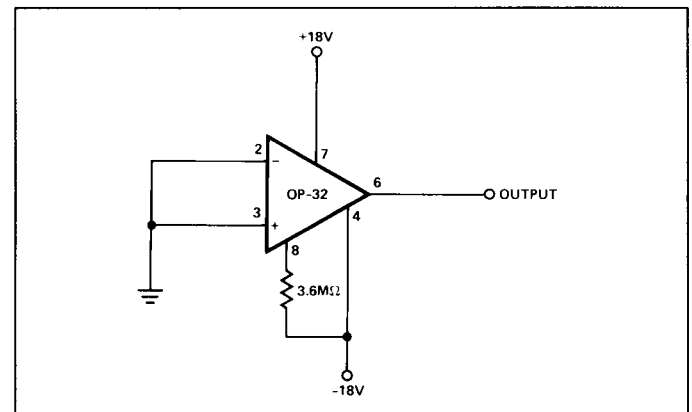
PARAMETER	SYMBOL	CONDITIONS	MIN	OP-32A TYP	MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnullled	—	0.5	2.0	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	175	400	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	—	2	nA
Average Input Offset Current Drift	TCI_{OS}	(Notes 1, 2)	—	1	10	$pA/^\circ C$
Input Bias Current (Note 2)	I_B	$I_{SY} = 15\mu A$	—	3	5	nA
		$I_{SY} = 150\mu A$	—	20	35	
		$I_{SY} = 450\mu A$	—	60	90	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 3)	CMRR	$V_S = \pm 15V$				dB
		$-15V \leq V_{CM} \leq +13.5$				
		$I_{SET} = 10\mu A$ $I_{SET} = 1\mu A$	90 80	110 90	— —	
Power Supply Rejection Ratio (Note 3)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V_- = 0V$, $V_+ = 3V$ to $30V$ ($V_{CM} = 1.5V$)	—	2	10	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	200	400	—	V/mV
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	500	1000	—	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 0.65	± 0.75	—	V
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$				
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 13.6	± 14.0	—	V
Supply Current No Load (Note 4)	I_{SY}	$V_S = \pm 15V$	—	—	—	μA
		$I_{SET} = 1\mu A$	—	16	18	
		$I_{SET} = 10\mu A$	—	160	180	
		$I_{SET} = 30\mu A$	—	450	550	μA
		$V_S = \pm 1.5V$	—	—	—	
		$I_{SET} = 1\mu A$	—	12	14	
		$I_{SET} = 10\mu A$	—	120	140	μA
		$I_{SET} = 30\mu A$	—	360	450	μA

NOTES:

1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.
3. PSRR and CMRR measured with V_{OS} unnullled and I_{SET} held constant.
4. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V_+) - (V_-)}{6}$$

BURN-IN CIRCUIT*



*Other circuits may apply at ADI's discretion.

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ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $-25^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32E			OP-32F			OP-32G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnull'd	—	0.5	1.5	—	1.0	2.0	—	1.5	3.0	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	100	400	—	200	600	—	500	1200	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	—	2	—	—	2	—	—	3	nA
Average Input Offset Current Drift	TCI_{OS}	(Notes 1, 2)	—	2	10	—	3	15	—	5	25	$pA/^\circ C$
Input Bias Current (Note 2)	I_B	$I_{SY} = 15\mu A$	—	3	5	—	5	7.5	—	5	10	nA
		$I_{SY} = 150\mu A$	—	20	35	—	24	35	—	30	50	
		$I_{SY} = 450\mu A$	—	60	90	—	70	100	—	80	125	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15.0/13.5	—	—	-15.0/13.5	—	—	-15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 3)	CMRR	$V_S = \pm 15V$ & $-15V \leq V_{CM} \leq +13.5V$	95	110	—	90	105	—	80	100	—	dB
Power Supply Rejection Ratio (Note 3)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V_- = 0V$, $V_+ = 3V$ to $30V$	—	3.2	10	—	10	32	—	32	56	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	750	1000	—	500	1000	—	400	1000	—	V/mV
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	750	1000	—	500	1000	—	400	1000	—	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 0.70	± 0.75	—	± 0.65	± 0.75	—	± 0.6	± 0.7	—	V
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$										
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 13.8	± 14.1	—	± 13.6	± 14.1	—	± 13.0	± 14.0	—	V
Supply Current No Load (Note 4)	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	16	18	—	16	20	—	16	25	μA
		$I_{SET} = 10\mu A$	—	160	180	—	160	200	—	160	250	
		$I_{SET} = 30\mu A$	—	450	550	—	450	600	—	450	650	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	12	14	—	12	17	—	12	25	μA
		$I_{SET} = 10\mu A$	—	120	140	—	120	170	—	120	200	
		$I_{SET} = 30\mu A$	—	360	450	—	360	500	—	360	550	

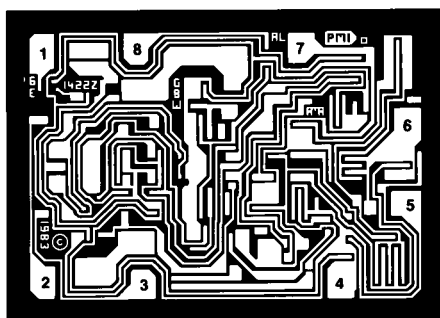
NOTES:

1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.
3. PSRR and CMRR measured with V_{OS} unnull'd and I_{SET} held constant.

4. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V_+) - (V_-)}{6}$$

DICE CHARACTERISTICS



DIE SIZE 0.070 X 0.050 inch, 3500 sq. mils
(1.78 X 1.27 mm, 2.26 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V_-
5. BALANCE
6. OUTPUT
7. V_+
8. I_{SET}

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32N LIMIT	OP-32G LIMIT	OP-32GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	500	1000	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	2	2	3	nA MAX
Input Bias Current (Note 1)	I_B	$I_{SY} = 15\mu A$	5	7.5	10	nA MAX
		$I_{SY} = 150\mu A$	35	35	50	
		$I_{SY} = 450\mu A$	90	100	125	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15/13.5	-15/13.5	-15/13.5	V MIN
Common-Mode Rejection Ratio (Note 2)	CMRR	$V_S = \pm 15V$ $-15V \leq V_{CM} \leq +13.5V$	100	95	85	dB MIN
Power Supply Rejection Ratio (Note 2)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V_- = 0V$, $V_+ = 3V$ to $30V$	6	12	25	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	1000	750	500	V/mV MIN
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	1000	750	500	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 0.8	± 0.8	± 0.75	V MIN
		$R_L = 100k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$				
		$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 14	± 14	± 13.8	V MIN
Supply Current No Load (Note 3)	I_{SY}	$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	12.5	15	18	μA MAX
		$I_{SET} = 10\mu A$	125	150	180	
		$I_{SET} = 30\mu A$	400	450	500	
		$V_S = \pm 15V$, $I_{SET} = 1\mu A$	17	19	21	μA MAX
		$I_{SET} = 10\mu A$	170	190	200	
		$I_{SET} = 30\mu A$	525	600	650	

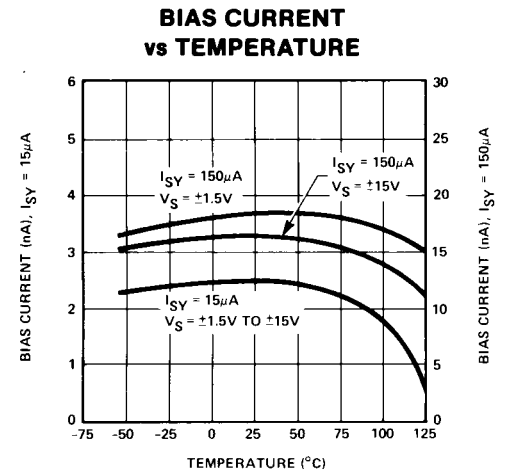
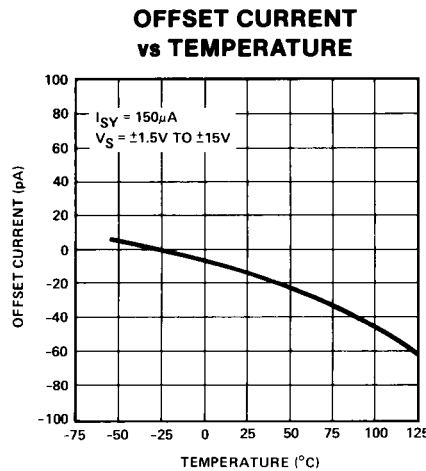
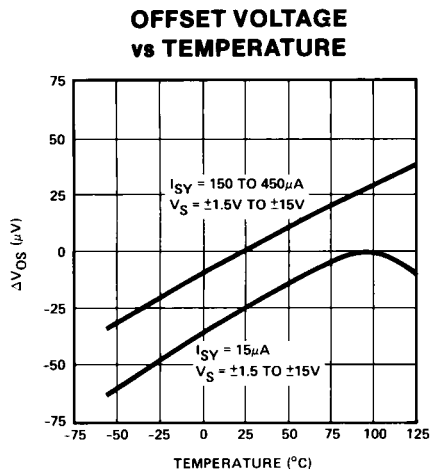
NOTES:

- I_B and I_{OS} are measured at $V_{CM} = 0$.
- PSRR and CMRR measured with V_{OS} unnullified and I_{SET} held constant.
- The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V_+) - (V_-)}{6}$$

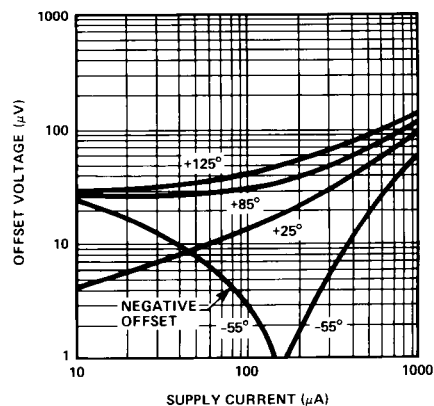
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL DC PERFORMANCE CHARACTERISTICS

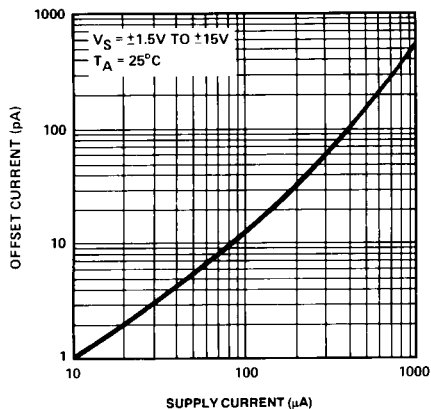


TYPICAL DC PERFORMANCE CHARACTERISTICS

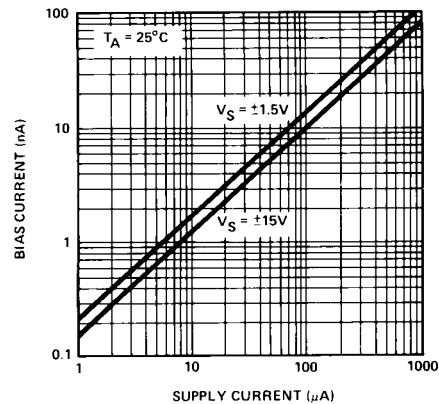
**OFFSET VOLTAGE
vs SUPPLY CURRENT**



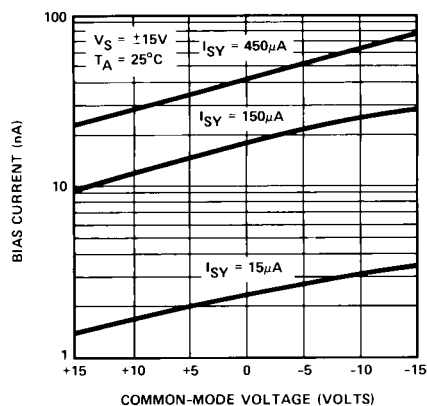
**OFFSET CURRENT
vs SUPPLY CURRENT**



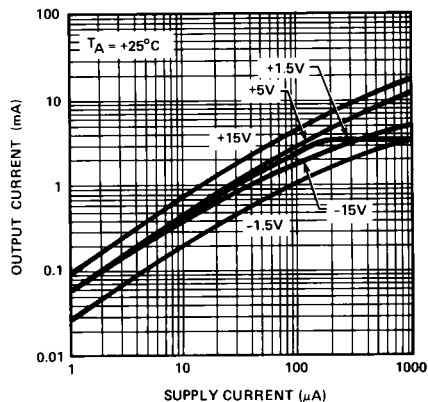
**BIAS CURRENT
vs SUPPLY CURRENT**



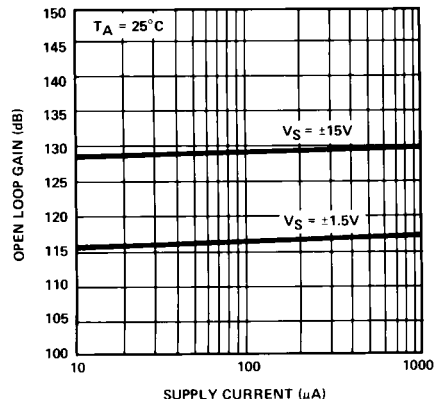
**BIAS CURRENT vs
COMMON-MODE VOLTAGE**



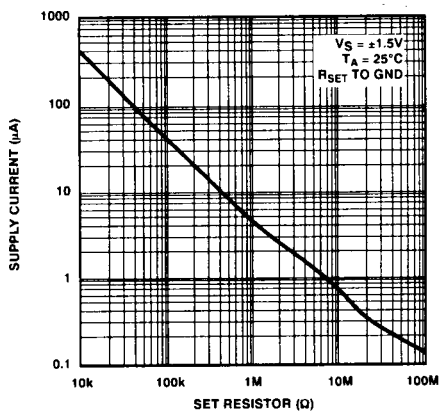
**MAXIMUM OUTPUT CURRENT
vs SUPPLY CURRENT AT
 $V_S = \pm 15V, +5V$ AND $\pm 1.5V$**



**OPEN-LOOP GAIN
vs SUPPLY CURRENT**

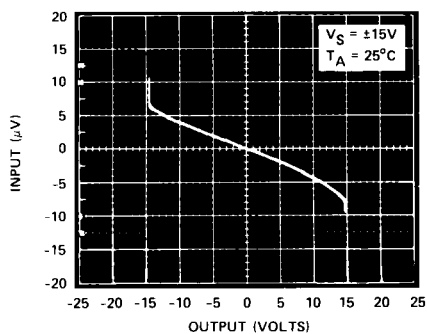


**SUPPLY CURRENT
vs SET RESISTOR**

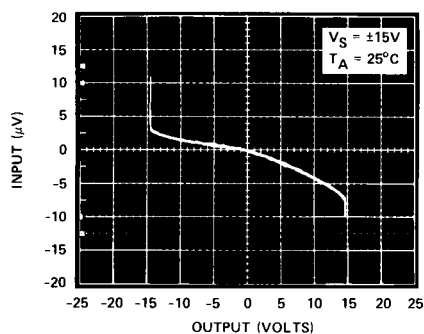


TYPICAL DC OPEN-LOOP INPUT-OUTPUT CHARACTERISTICS

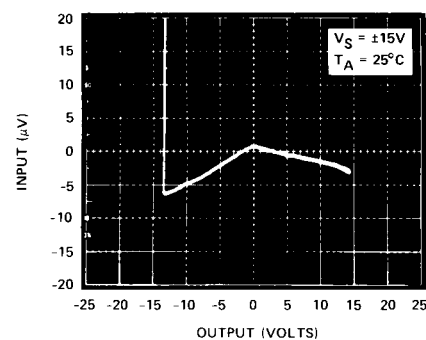
$I_{SY} = 1\text{mA}, R_L = 100\text{k}\Omega$



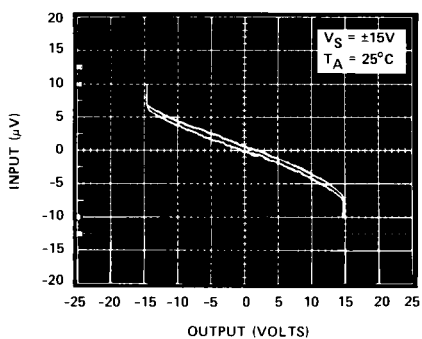
$I_{SY} = 1\text{mA}, R_L = 10\text{k}\Omega$



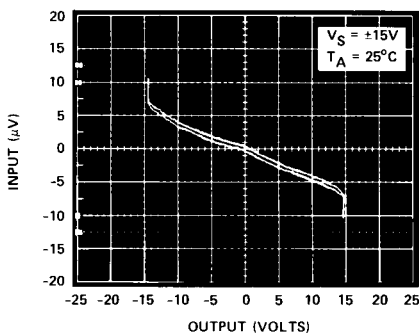
$I_{SY} = 1\text{mA}, R_L = 2\text{k}\Omega$



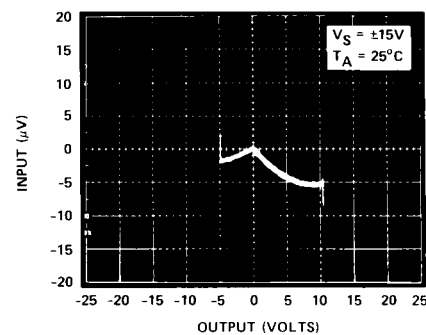
$I_{SY} = 100\mu\text{A}, R_L = 100\text{k}\Omega$



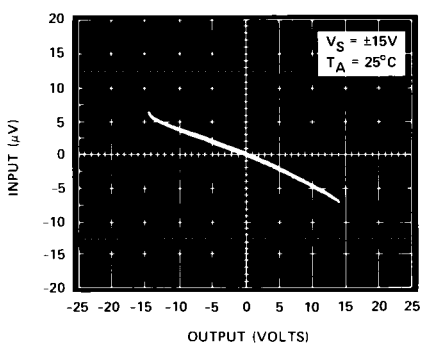
$I_{SY} = 100\mu\text{A}, R_L = 10\text{k}\Omega$



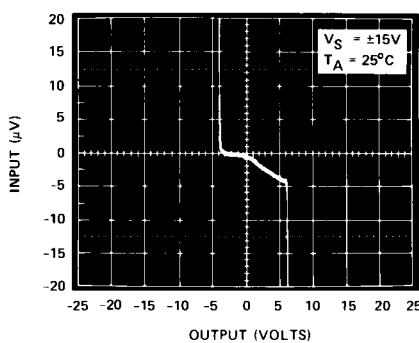
$I_{SY} = 100\mu\text{A}, R_L = 2\text{k}\Omega$



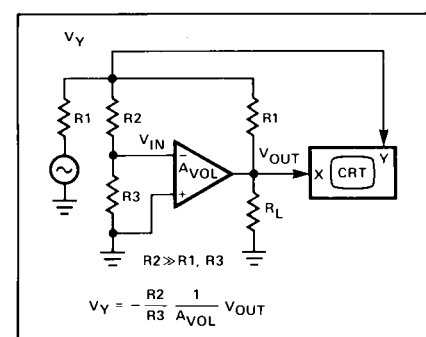
$I_{SY} = 10\mu\text{A}, R_L = 100\text{k}\Omega$



$I_{SY} = 10\mu\text{A}, R_L = 10\text{k}\Omega$



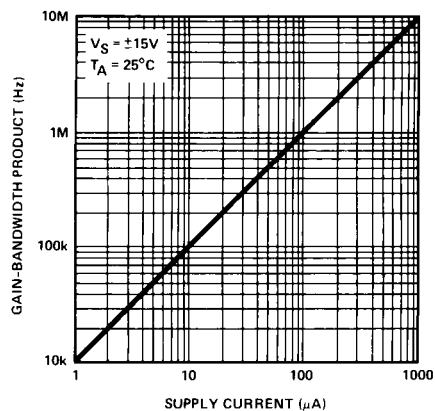
TEST CIRCUIT



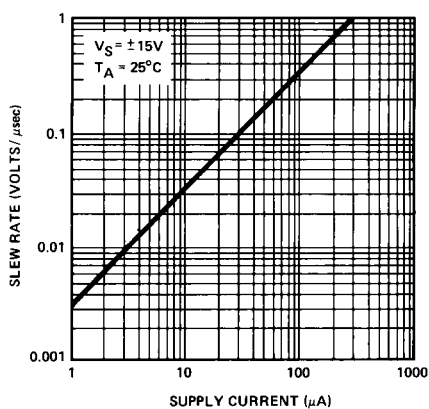
OP-32

TYPICAL AC PERFORMANCE CHARACTERISTICS

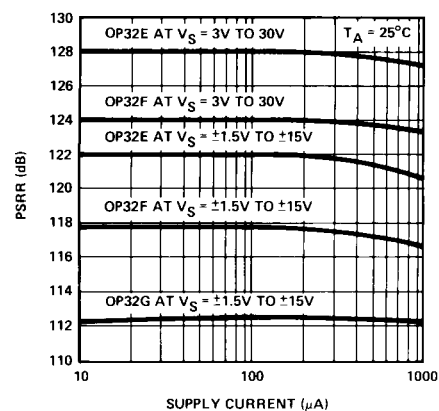
**GAIN-BANDWIDTH PRODUCT
vs SUPPLY CURRENT**



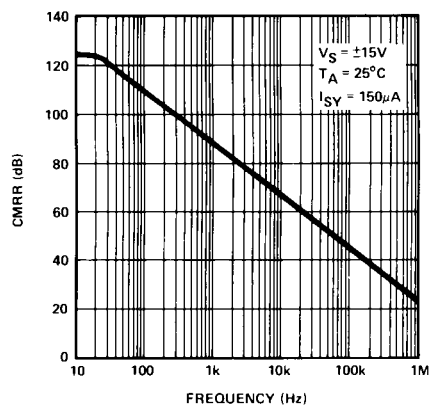
**SLEW RATE vs
SUPPLY CURRENT**



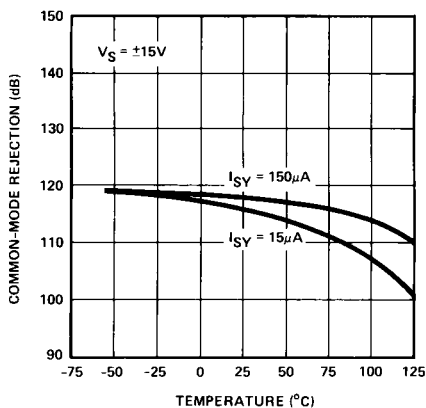
**POWER SUPPLY REJECTION
vs SUPPLY CURRENT**



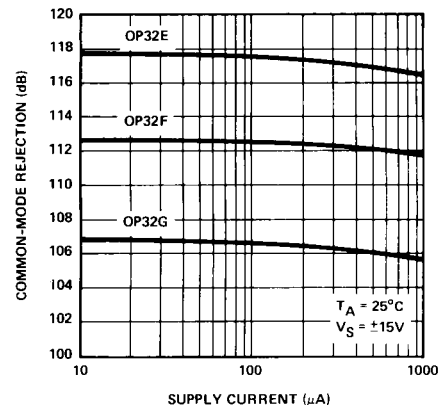
**COMMON-MODE REJECTION
vs FREQUENCY**



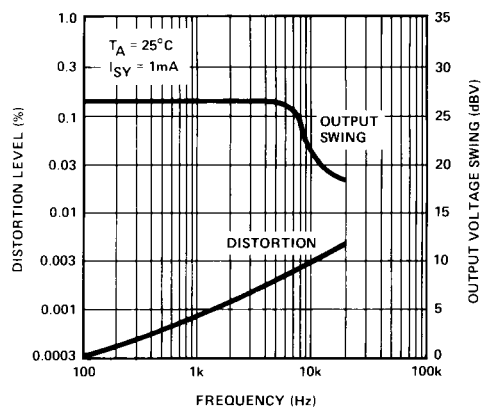
**COMMON-MODE REJECTION
vs TEMPERATURE**



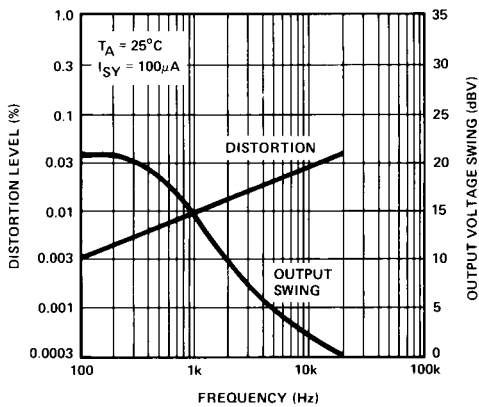
**COMMON-MODE REJECTION
vs SUPPLY CURRENT**



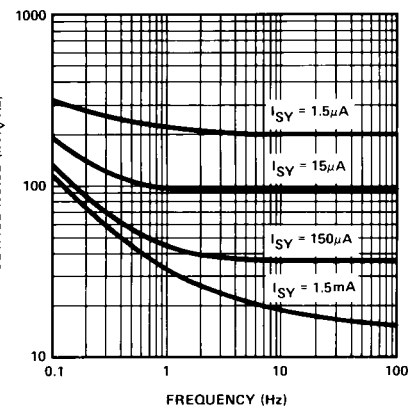
**TOTAL HARMONIC
DISTORTION vs FREQUENCY**



**TOTAL HARMONIC
DISTORTION vs FREQUENCY**



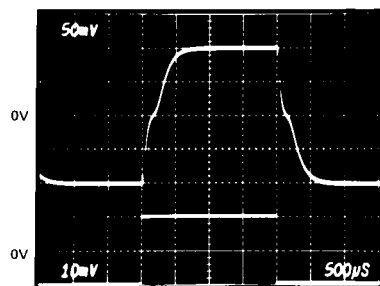
**VOLTAGE NOISE
vs FREQUENCY**



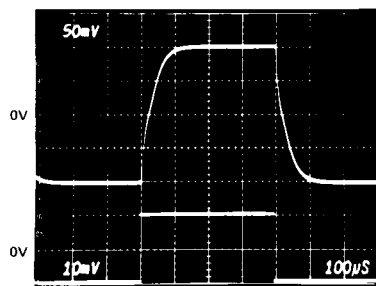
TYPICAL AC PERFORMANCE CHARACTERISTICS

SMALL-SIGNAL TRANSIENT RESPONSE vs SUPPLY CURRENT

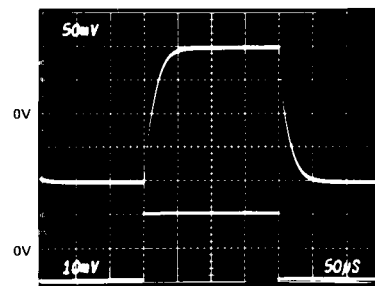
$I_{SY} = 1.5\mu A$



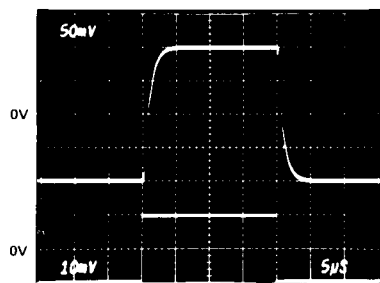
$I_{SY} = 7.5\mu A$



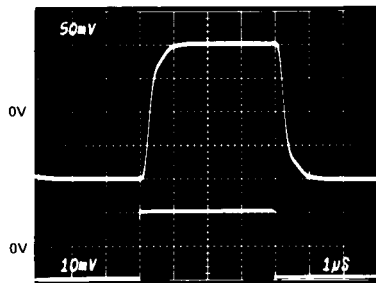
$I_{SY} = 15\mu A$



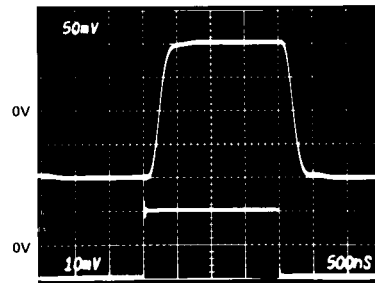
$I_{SY} = 150\mu A$



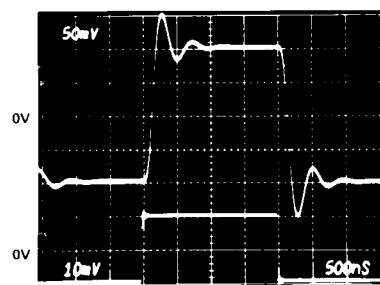
$I_{SY} = 450\mu A$



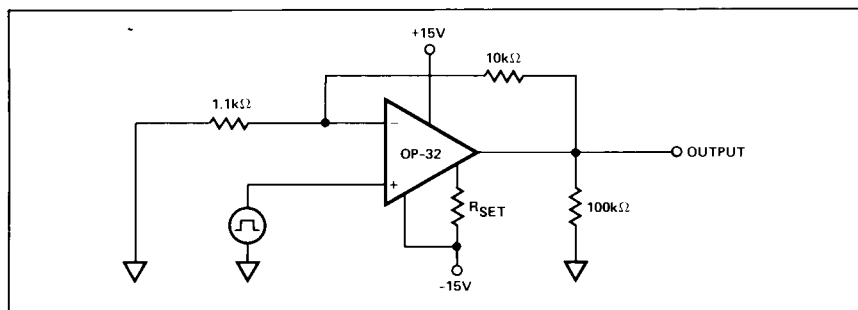
$I_{SY} = 750\mu A$



$I_{SY} = 1.5mA$



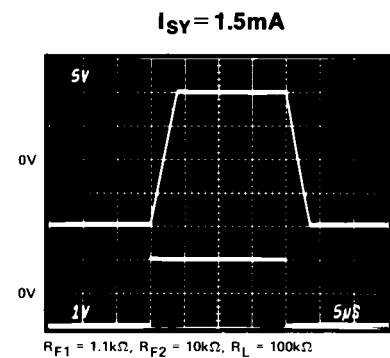
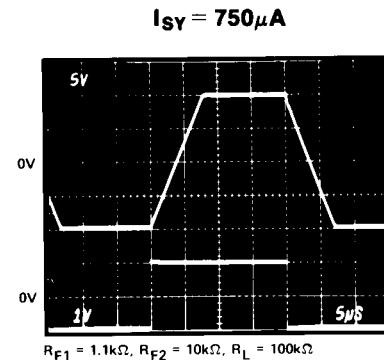
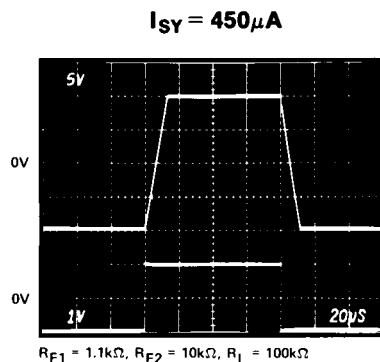
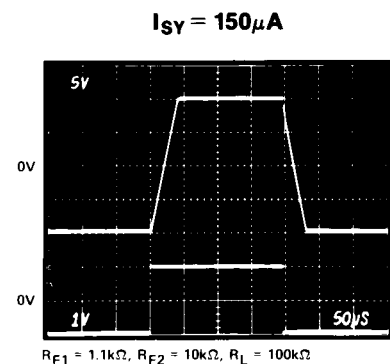
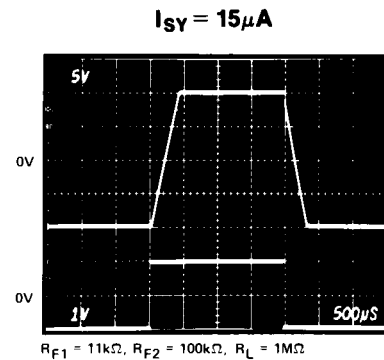
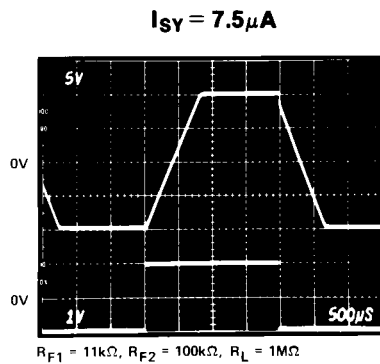
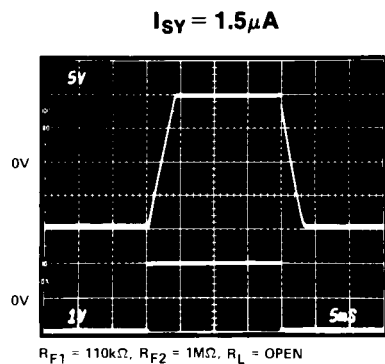
TEST CIRCUIT



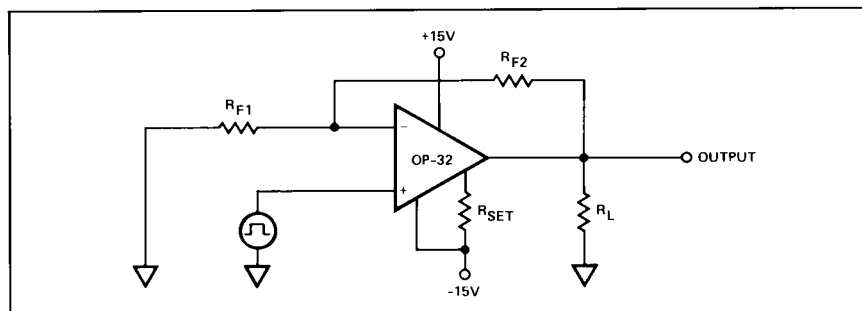
OP-32

TYPICAL AC PERFORMANCE CHARACTERISTICS

LARGE-SIGNAL TRANSIENT RESPONSE vs SUPPLY CURRENT



TEST CIRCUIT



APPLICATIONS INFORMATION

SETTING SUPPLY CURRENT

The op amp power supply current is determined by the current flowing out of pin 8. Pin 8 is at the $V+$ voltage less two diode drops, which is approximately $V+$ minus 1.1V. Do not connect pin 8 to ground or $V-$ without a set resistor in series or excessive supply current will be drawn which may damage the OP-32.

The set resistor value is selected to make the power supply current optimum for the specific application. Adjusting the OP-32 power supply current determines the slew-rate, bandwidth, and the output current limits (see Performance Characteristics). The supply current is nominally 15 times the set current and the set resistor value is calculated from:

$$R_S = \frac{(V_{SUPPLY} - 1.1V)}{I_{SET}}, \text{ where } I_{SY} \approx 15 I_{SET}$$

(See graph below)

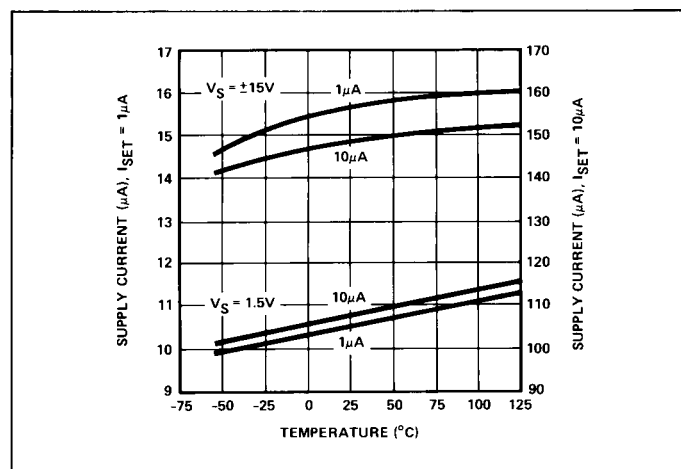
Note that the set resistor can go to either negative supply or to ground. If the set resistor goes to negative supply, then $V_{SUPPLY} = (V+) - (V-)$. For a single-supply circuit, V_{SUPPLY} is simply $(V+)$. If the supply voltage varies widely, set current can be stabilized with circuits (a), (b), or (c).

The relationship between supply voltage, supply current and set current can be approximated by:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V+) - (V-)}{6} \quad (T_A = 25^\circ C)$$

The ratio $\frac{I_{SY}}{I_{SET}}$ increases with temperature by approximately 0.05%/°C.

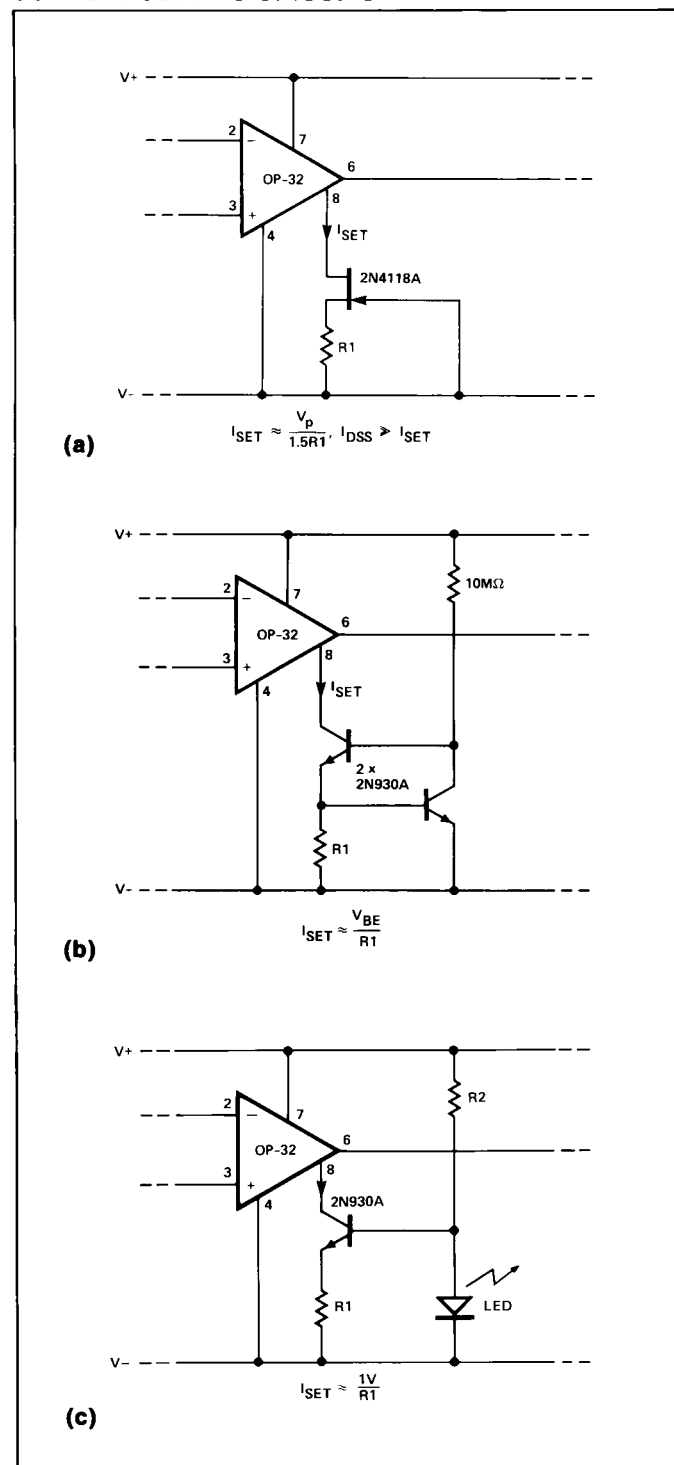
SUPPLY CURRENT vs TEMPERATURE



INPUT BIAS CURRENT

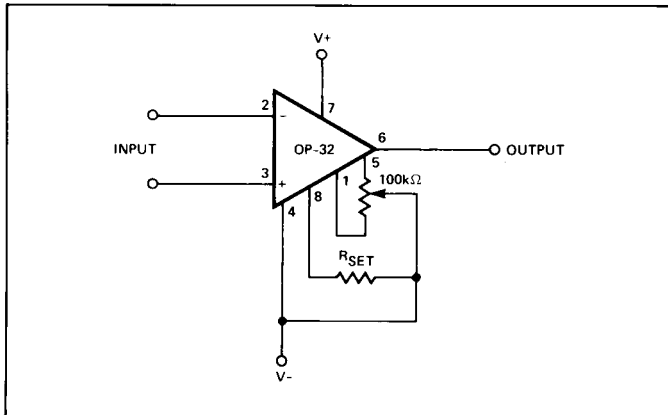
Input bias current varies directly with set current. The set current required for a given supply current ranges from $I_{SY}/10.5$ at $\pm 1.5V$ supply voltage to $I_{SY}/15$ at $\pm 15V$. Therefore, I_B will be highest at the minimum supply voltage condition of $\pm 1.5V$ (or 3V) for any given supply current.

CURRENT SETTING CIRCUITS



OP-32

OFFSET NULLING CIRCUIT



OFFSET VOLTAGE ADJUSTMENT

The offset voltage can be trimmed to zero using a 100kΩ potentiometer (see offset nulling circuit). Adjusting the pot wiper towards pin 5 causes the output to go positive. Adjustment range is approximately $\pm 5\text{mV}$ at $V_S = \pm 15\text{V}$. The V_{OS} adjust range is proportional to supply voltage. Resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors.

If power supply voltages vary widely and the set current is established by a resistor, the op amp supply currents will vary in proportion to the supply voltage changes. V_{OS} will remain almost constant with supply current changes if the null pins (1 and 5) are not used. If a V_{OS} adjust pot is used, current variations may flow through the offset pot causing an apparent V_{OS} change. If a V_{OS} adjust pot is used in combination with widely-varying supply voltages, a set-current stabilizer circuit as shown in (a), (b), or (c) is recommended.

APPLICATIONS EXAMPLE

BATTERY-POWERED, GAIN-OF-100 AMPLIFIER

The simple noninverting amplifier circuit shown in Figure 1 provides an accurate gain-of-100 while operating from a pair of 9V batteries. The circuit requires only $15\mu\text{A}$ of supply current. Slew-rate is approximately $0.06\text{V}/\mu\text{sec}$ and output swing is $\pm 8\text{V}$.

A value of $500\text{k}\Omega$ was chosen for R_2 . For a gain of 100, R_1 is calculated as:

$$A_{VCL} = 1 + \frac{R_2}{R_1}$$

$$100 = 1 + \frac{500\text{k}\Omega}{R_1}$$

$$\therefore R_1 = 5.05\text{k}\Omega$$

BATTERY-POWERED, GAIN-OF-100 AMPLIFIER

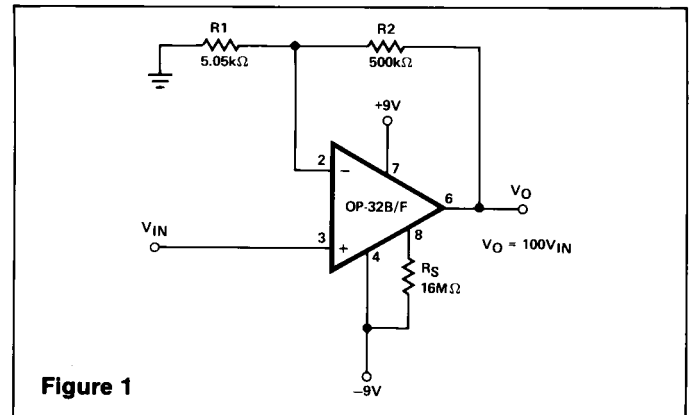


Figure 1

Using an OP-32B/F, we can expect an $I_B + I_{OS}/2$ of less than 8.5nA when operating at I_{SY} of $15\mu\text{A}$, so the input offset caused by $I_B R_1$ will be negligible ($8.5\text{nA} \times 5.05\text{k}\Omega \sim 43\mu\text{V}$).

The set resistor R_S needed for a supply current of $15\mu\text{A}$ is calculated from:

$$R_S = \frac{V_{SUPPLY} - 1.1\text{V}}{I_{SY}/15} = \frac{18\text{V} - 1.1\text{V}}{1\mu\text{A}}$$

$$\therefore R_S = 16.9\text{M}\Omega$$

Offset voltage adjustment is optional. An OP-32B/F has maximum input offset voltage of $500\mu\text{V}$ which would cause an output offset voltage of 50mV . Drift over temperature is very low, typically less than $1.0\mu\text{V}/^\circ\text{C}$, and is guaranteed to be less than $2.0\mu\text{V}/^\circ\text{C}$. PSRR is also low, only $6\mu\text{V}/\text{V}$, so battery voltage change has negligible effect on offset.

Most micropower programmable op amps lose open-loop gain and CMRR at low supply currents. The OP-32 design overcomes these limitations so accuracy is maintained at supply currents of only a few microamps. The OP-32B/F used in this example has a minimum open-loop gain of over 117dB . Gain error due to finite open-loop gain will be less than $100/750,000$, which is only 133PPM . CMRR will typically be 110dB , an error of 3PPM . Gain accuracy of the circuit is almost entirely dependent on the accuracy of the R_1/R_2 ratio; the op amp contributes less than 0.015% gain error.

Considering all error sources, this simple $\times 100$ battery-powered circuit using an OP-32B/F is capable of achieving excellent accuracy. Without external adjustments of any kind, output offset will be less than 54mV and gain accuracy will be better than $\pm 0.015\%$ (exclusive of R_2/R_1 error). Gain linearity, slew-rate symmetry, and stability over temperature are all excellent with the OP-32, making circuit performance very predictable.