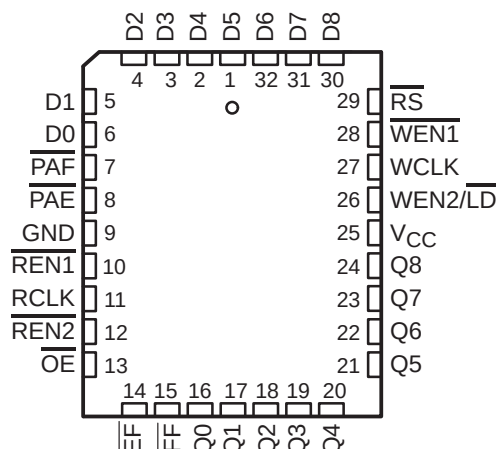
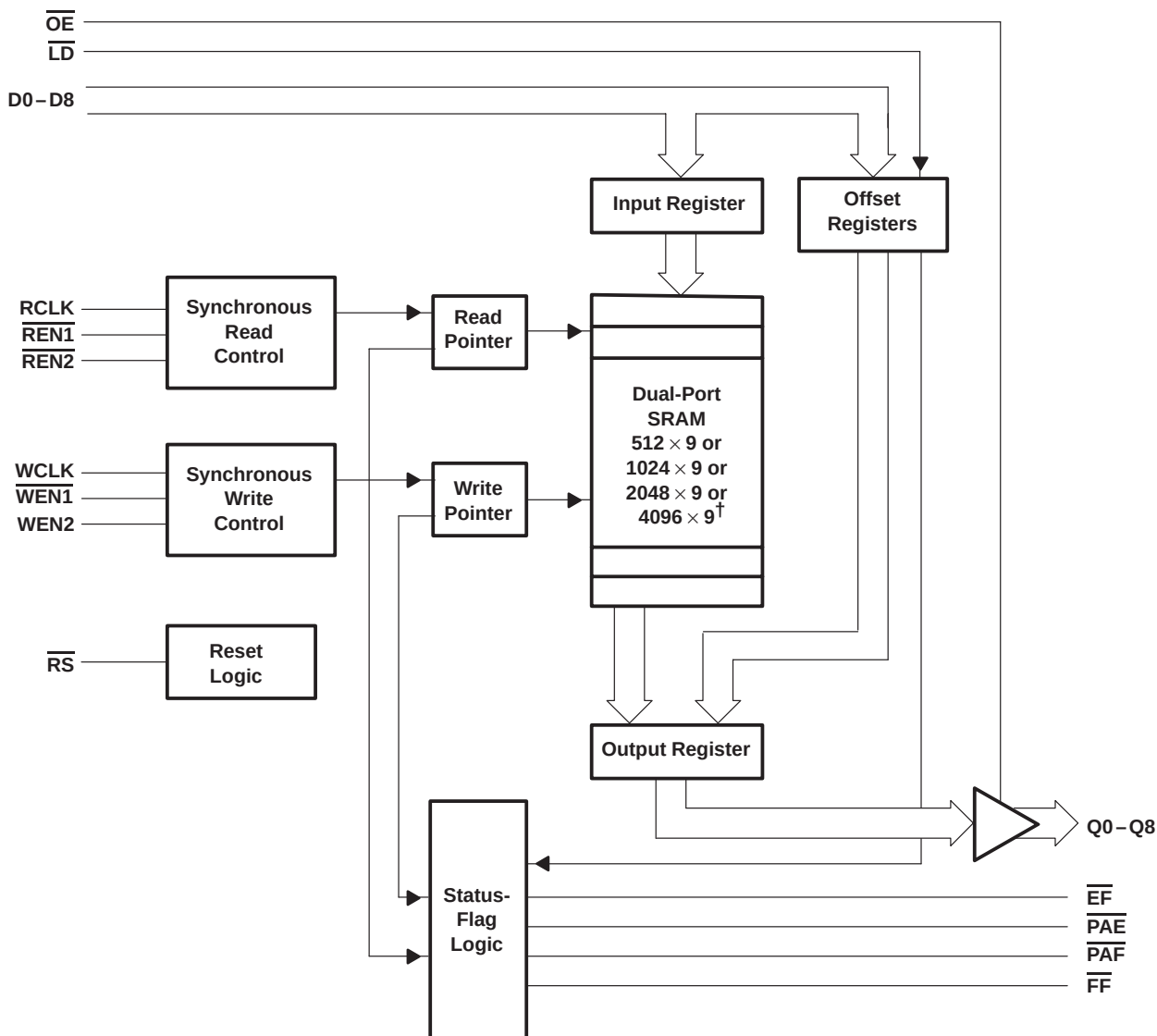


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- RJ PACKAGE
-
- (TOP VIEW)



functional block diagram



[†] 512 × 9 for the SN74ACT72211L; 1024 × 9 for the SN74ACT72221L; 2048 × 9 for the SN74ACT72231L; 4096 × 9 for the SN74ACT72241L

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
D0–D8	6–1, 32–30	I	Data inputs
$\overline{EF}$	14	O	Empty-flag. When memory is empty, $\overline{EF}$ is low and further data reads are ignored by the device. When $\overline{EF}$ is high, the memory is not empty and data reads are allowed. $\overline{EF}$ is synchronized to RCLK by one flip-flop.
$\overline{FF}$	15	O	Full-flag. When memory is full, $\overline{FF}$ is low and data writes are inhibited. $\overline{FF}$ is synchronized to WCLK by one flip-flop.
GND	9		Ground
$\overline{OE}$	13	I	Output-enable. Q0–Q8 are in the high-impedance state when $\overline{OE}$ is high. Q0–Q8 are active when $\overline{OE}$ is low.
$\overline{PAE}$	8	O	Programmable almost-empty-flag. $\overline{PAE}$ is low when the FIFO is almost empty based on the value in its offset register. The default value for the register is empty + 7. $\overline{PAE}$ is synchronized to RCLK by one flip-flop.
$\overline{PAF}$	7	O	Programmable almost-full-flag. $\overline{PAF}$ is low when the FIFO is almost full based on the value in its offset register. The default value for the register is full – 7. $\overline{PAF}$ is synchronized to WCLK by one flip-flop.
Q0–Q8	16–24	O	Data outputs
RCLK	11	I	Read-clock. A data read is performed by the low-to-high transition of RCLK when $\overline{REN1}$ and $\overline{REN2}$ are asserted and $\overline{EF}$ is high.
$\overline{REN1}$, $\overline{REN2}$	10, 11	I	Read-enable. Data is read from the FIFO on a low-to-high transition of RCLK when $\overline{REN1}$ and $\overline{REN2}$ are low and $\overline{EF}$ is high.
$\overline{RS}$	29	I	Reset. When $\overline{RS}$ is set low, the read and write pointers are initialized to the first RAM location and the FIFO is empty. $\overline{FF}$ and $\overline{PAF}$ are set high, and $\overline{EF}$ and $\overline{PAE}$ are set low. Each bit in the data output register is set low by a device reset. The FIFO must be reset after power up before data is written.
V _{CC}			Supply voltage
WCLK	27	I	Write-clock. Data is written by the low-to-high transition of WCLK when $\overline{WEN1}$ and $\overline{WEN2/LD}$ are asserted and $\overline{FF}$ is high.
$\overline{WEN1}$	28	I	Write-enable 1. $\overline{WEN1}$ is the only write enable terminal if the device is configured to have programmable flags. Data is written on a low-to-high transition of WCLK when $\overline{WEN1}$ is low and $\overline{FF}$ is high. If the FIFO is not configured for programmable flags, data is written on a low-to-high transition of WCLK when $\overline{WEN1}$ and $\overline{WEN2}$ are asserted and $\overline{FF}$ is high.
$\overline{WEN2/LD}$	26	I	Write-enable 2/load. This is a dual-purpose input. The FIFO can have either two write enables or programmable flags. To use $\overline{WEN2/LD}$ as a $\overline{WEN2}$, $\overline{WEN2/LD}$ must be held high at reset. When $\overline{WEN2}$ and $\overline{WEN1}$ are asserted and $\overline{FF}$ is high, a low-to-high transition of WCLK writes data. To use $\overline{WEN2/LD}$ as the $\overline{LD}$ terminal, it must be held low at reset. In this case, $\overline{LD}$ is asserted low to write or read the programmable offset registers.

detailed description

device reset

A reset is performed by taking the reset ($\overline{RS}$) input low. This initializes both the write and read pointers to the first memory location. After a reset, the full flag ($\overline{FF}$) and programmable almost-full flag ($\overline{PAF}$) are high and the empty flag ($\overline{EF}$) and programmable almost-empty flag ($\overline{PAE}$) are low. Each bit in the data output register (Q0–Q8) is set low, and the flag offset registers are loaded with the default offset values. A FIFO must be reset after power up before a write cycle is allowed.

The logic level on the dual-purpose input write enable 2/load ($\text{WEN2}/\overline{LD}$) during reset determines its function. If $\text{WEN2}/\overline{LD}$ is high when $\overline{RS}$ returns high at the end of the reset cycle, the input is a second write enable (see FIFO writes and reads) and the programmable flags ($\overline{PAF}$, $\overline{PAE}$) can only use the default values. If $\text{WEN2}/\overline{LD}$ is low when $\overline{RS}$ returns high at the end of the reset cycle, the input is the load ($\overline{LD}$) enable for writing and reading flag offset registers (see flag programming).

FIFO writes and reads

Data is written to memory by a low-to-high transition of write clock (WCLK) when write enable 1 ($\overline{WEN1}$) is low, $\text{WEN2}/\overline{LD}$ is high, and $\overline{FF}$ is high. This stores D0–D8 data in the dual-port SRAM and increments the write pointer.

If no reads are performed after reset ($\overline{RS} = V_{IL}$), $\overline{FF}$ is set low upon the completion of 512 writes to the SN74ACT72211, 1024 writes to the SN74ACT72221, 2048 writes to the SN74ACT72231, and 4096 writes to the SN74ACT72241. Attempted write cycles are ignored when $\overline{FF}$ is low. $\overline{FF}$ is set high by the first low-to-high transition of WCLK after data is read from a full FIFO. $\overline{FF}$ and $\overline{PAF}$ are each synchronized to the low-to-high transition of WCLK by one flip-flop.

If a device is configured to have two write enables (see device reset), data is read by the low-to-high transition of read clock (RCLK) when both read enables ($\overline{REN1}$, $\overline{REN2}$) are low and $\overline{EF}$ is high. $\text{WEN2}/\overline{LD}$ must also be high if the device is configured to have programmable flags. A read from the FIFO puts RAM data on Q0–Q8 and increments the read pointer in the same sequence as the write pointer. New data is not shifted to the output register while either one or both of the read enables are high.

$\overline{EF}$ and $\overline{PAE}$ are each synchronized to the low-to-high transition of RCLK by one flip-flop. When the device is empty, the write and read pointers are equal and $\overline{EF}$ is set low. Attempted read cycles are ignored while $\overline{EF}$ is set low. $\overline{EF}$ is set high by the first low-to-high transition of RCLK after data is written to an empty FIFO.

WCLK and RCLK can be asynchronous or coincident to one another. Writing data to FIFO memory is independent of reading data from FIFO memory and vice versa.

flag programming

When $\text{WEN2}/\overline{LD}$ is held low during a device reset ($\overline{RS} = V_{IL}$), the input is the load ($\overline{LD}$) enable for flag offset programming. In this configuration, $\text{WEN2}/\overline{LD}$ can be used to access the four 8-bit offset registers contained in the SN74ACT72211L/-72221L/-72231L/-72241L for writing or reading data.

When the device is configured for programmable flags and both $\text{WEN2}/\overline{LD}$ and $\overline{WEN1}$ are low, the first low-to-high transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth low-to-high transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when $\text{WEN2}/\overline{LD}$ and $\overline{WEN1}$ are low. The fifth low-to-high transition of WCLK while $\text{WEN2}/\overline{LD}$ and $\overline{WEN1}$ are low writes data to the empty LSB register again. Figure 1 shows the register sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then, by bringing the $\text{WEN2}/\overline{LD}$ input high, the FIFO is returned to normal read and write operation. The next time $\text{WEN2}/\overline{LD}$ is brought low, a write operation stores data in the next offset register in sequence.

flag programming (continued)

The contents of the offset registers can be read to the data outputs when $\overline{WEN2}/\overline{LD}$ is low and both $\overline{REN1}$ and $\overline{REN2}$ are low. Low-to-high transitions of RCLK read the register contents to the data outputs. Writes and reads should not be performed simultaneously on the offset registers (see Figure 1 and Table 1).

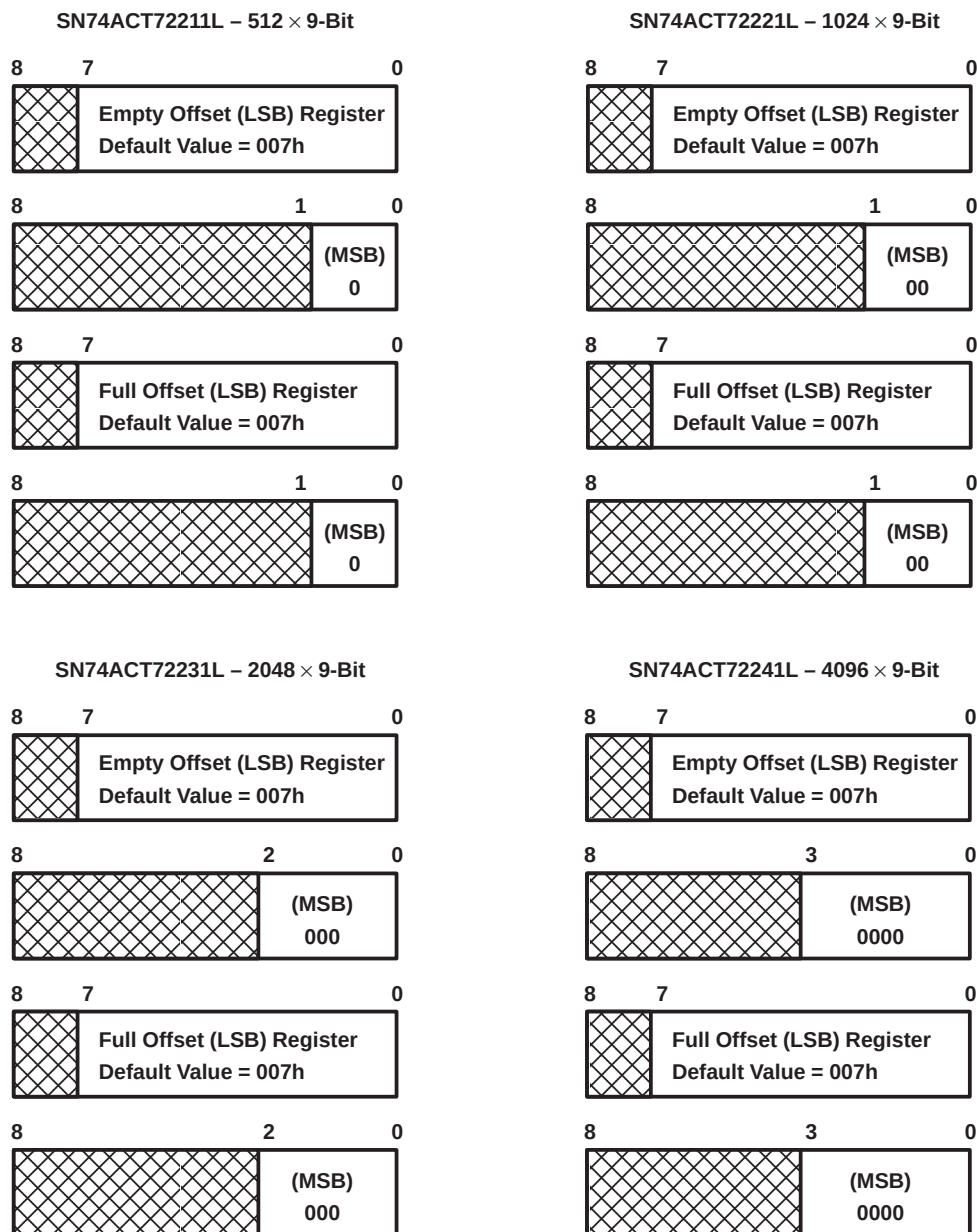


Figure 1. Offset Register Location and Default Values

flag programming (continued)

Table 1. Writing the Offset Registers

LD	WEN1	WCLK [†]	SELECTION
0	0	↑	Empty offset (LSB) ← Empty offset (MSB) Full offset (LSB) Full offset (MSB) →
0	1	↑	No operation
1	0	↑	Write into FIFO
1	1	↑	No operation

[†] The same selection sequence applies to reading from the registers. $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are enabled and a read is performed on the low-to-high transition of RCLK.

programmable flag ($\overline{\text{PAE}}$, $\overline{\text{PAF}}$) operation

Whether the flag offset registers are programmed as described in Table 1 or the default values are used, the programmable almost-empty flag ($\overline{\text{PAE}}$) and programmable almost-full flag ($\overline{\text{PAF}}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

The number formed by the empty offset least significant bit register and empty offset most significant bit register is referred to as n and determines the operation of $\overline{\text{PAE}}$. $\overline{\text{PAE}}$ is synchronized to the low-to-high transition of RCLK by one flip-flop and is low when the FIFO contains n or fewer unread words. $\overline{\text{PAE}}$ is set high by the low-to-high transition of RCLK when the FIFO contains $(n + 1)$ or greater unread words.

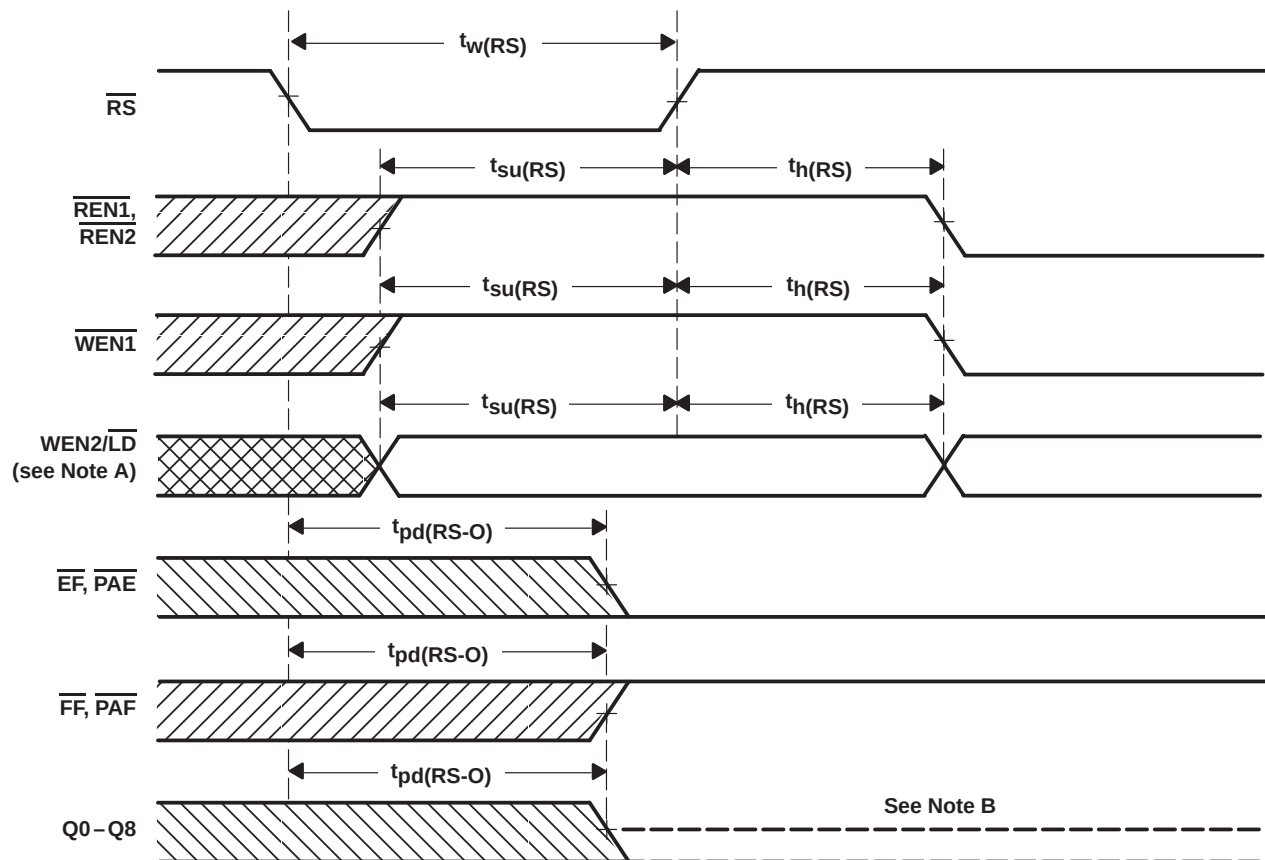
The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as m and determines the operation of $\overline{\text{PAF}}$. $\overline{\text{PAF}}$ is synchronized to the low-to-high transition of WCLK by one flip-flop and is set low when the number of unread words in the FIFO is greater than or equal to $(512 - m)$ for the SN74ACT72211L, $(1024 - m)$ for the SN74ACT72221L, $(2048 - m)$ for the SN74ACT72231L, and $(4096 - m)$ for the SN74ACT72241L. $\overline{\text{PAF}}$ is set high by the low-to-high transition of WCLK when the number of available memory locations is greater than m (see Table 2).

Table 2. Status Flags

NUMBER OF WORDS IN FIFO				OUTPUTS			
SN74ACT72211L	SN74ACT72221L	SN74ACT72231L	SN74ACT72241L	$\overline{\text{FF}}$	$\overline{\text{PAF}}$	$\overline{\text{PAE}}$	$\overline{\text{EF}}$
0	0	0	0	H	H	L	L
1 to $n^{\dagger}$	1 to $n^{\dagger}$	1 to $n^{\dagger}$	1 to $n^{\dagger}$	H	H	L	H
$(n + 1)$ to [512 – $(m + 1)$]	$(n + 1)$ to [1024 – $(m + 1)$]	$(n + 1)$ to [2048 – $(m + 1)$]	$(n + 1)$ to [4096 – $(m + 1)$]	H	H	H	H
$(512 - m)^{\ddagger}$ to 511	$(1024 - m)^{\ddagger}$ to 1023	$(2048 - m)^{\ddagger}$ to 2047	$(4096 - m)^{\ddagger}$ to 4095	H	L	H	H
512	1024	2048	4096	L	L	H	H

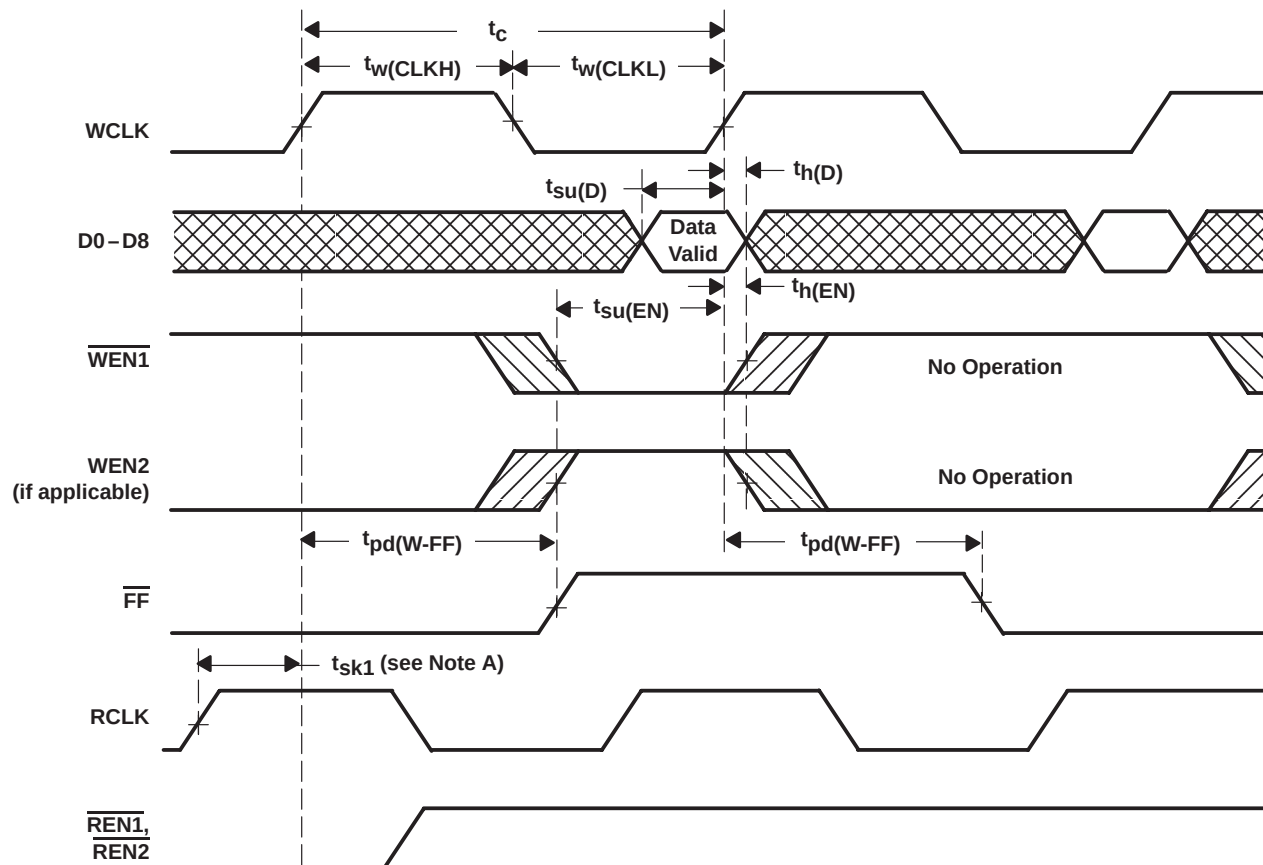
[†] n = empty offset (default value = 7)

[‡] m = full offset (default value = 7)



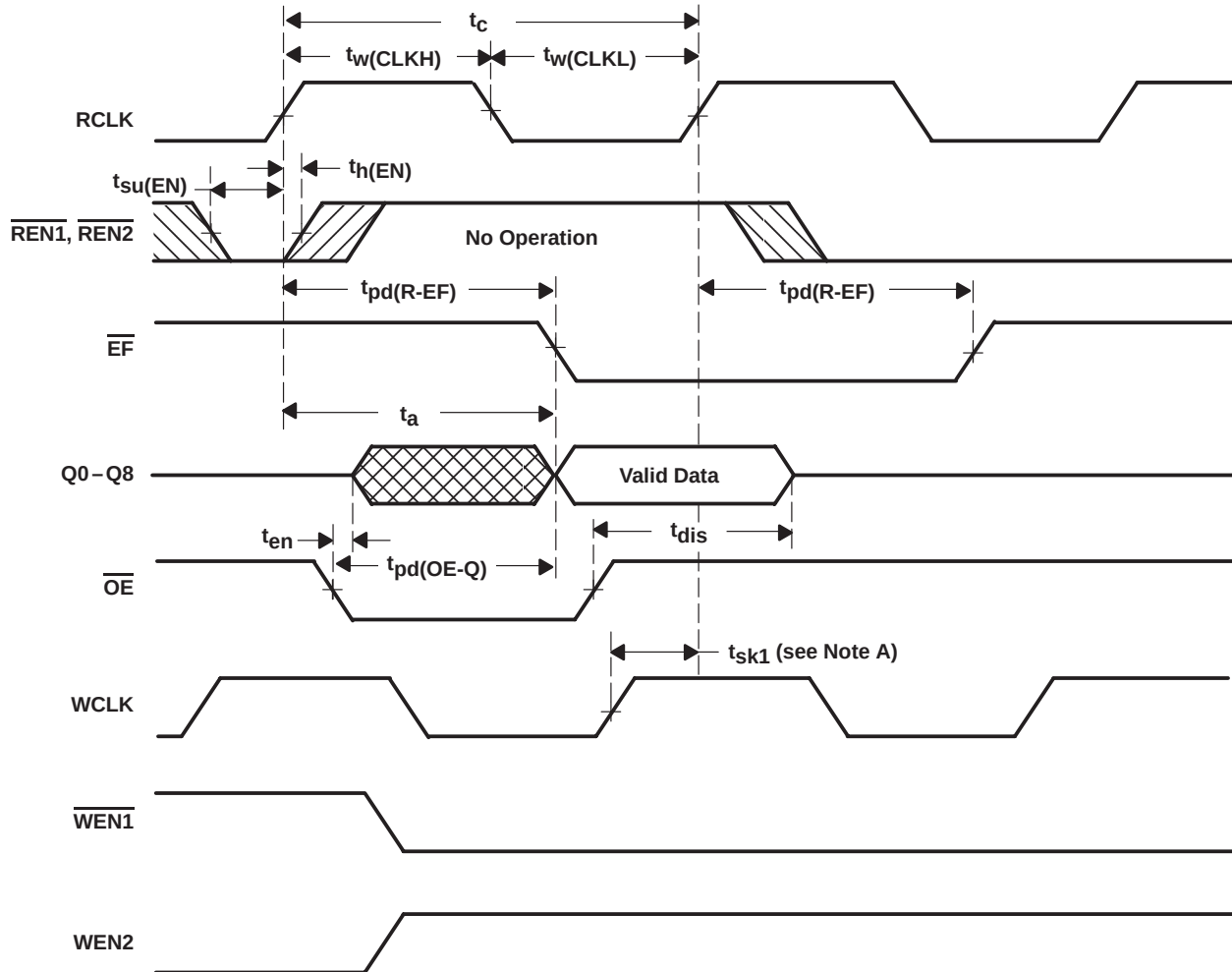
- NOTES: A. Holding $\overline{WEN2/LD}$ high during reset makes it act as a second write enable. Holding $\overline{WEN2/LD}$ low during reset makes it act as a load enable for the programmable flag offset registers.
 B. After reset, the outputs are low if $\overline{OE}$ is low and at the high-impedance level if $\overline{OE}$ is high.
 C. The clocks (RCLK, WCLK) can be free running during reset.

Figure 2. Reset Timing



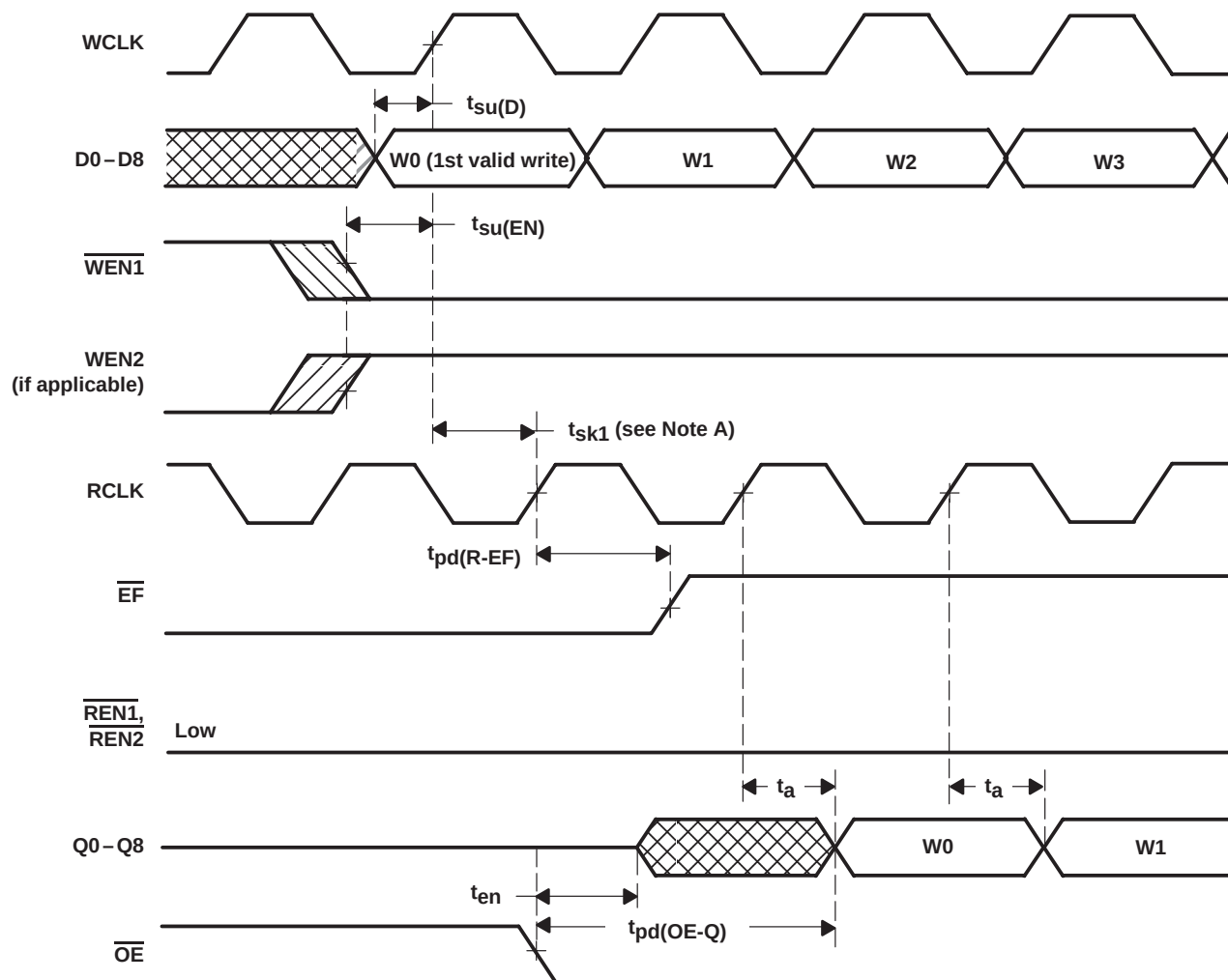
NOTE A: t_{sk1} is the minimum time between a rising RCLK edge and a subsequent rising WCLK edge for $\overline{FF}$ to change logic levels during the current clock cycle. If the time between the rising edge of RCLK and the subsequent rising edge of WCLK is less than t_{sk1} , then $\overline{FF}$ may not change its logic level until the next WCLK rising edge.

Figure 3. Write-Cycle Timing



NOTE A: t_{sk1} is the minimum time between a rising WCLK edge and a subsequent rising RCLK edge for $\overline{EF}$ to change logic levels during the current clock cycle. If the time between the rising edge of WCLK and the subsequent rising edge of RCLK is less than t_{sk1} , then $\overline{EF}$ may not change its logic level until the next RCLK rising edge.

Figure 4. Read-Cycle Timing

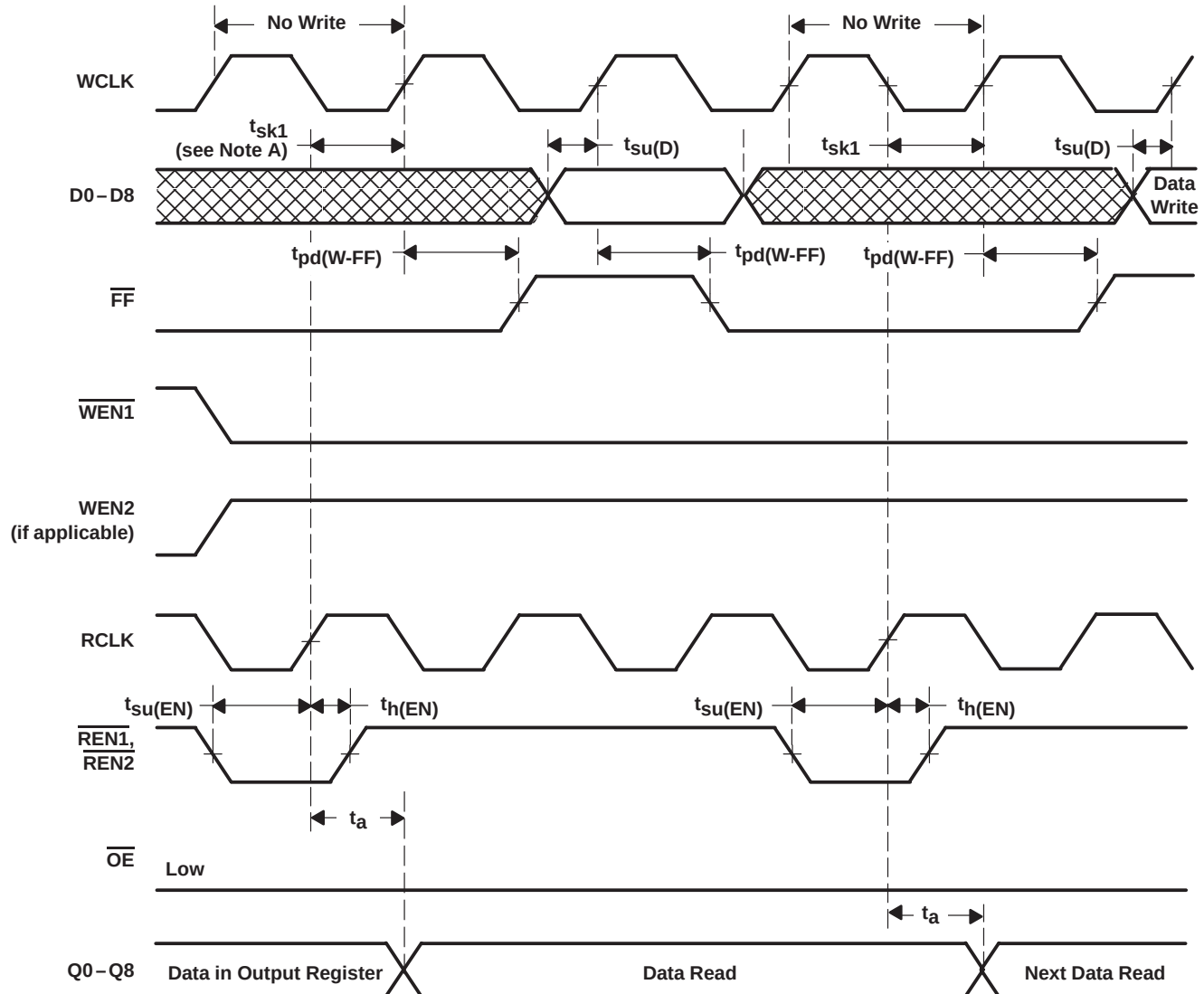


NOTE A: t_{sk1} is the minimum time between a rising WCLK edge and a subsequent rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{sk1} , then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 5. First-Data-Word-Latency Timing

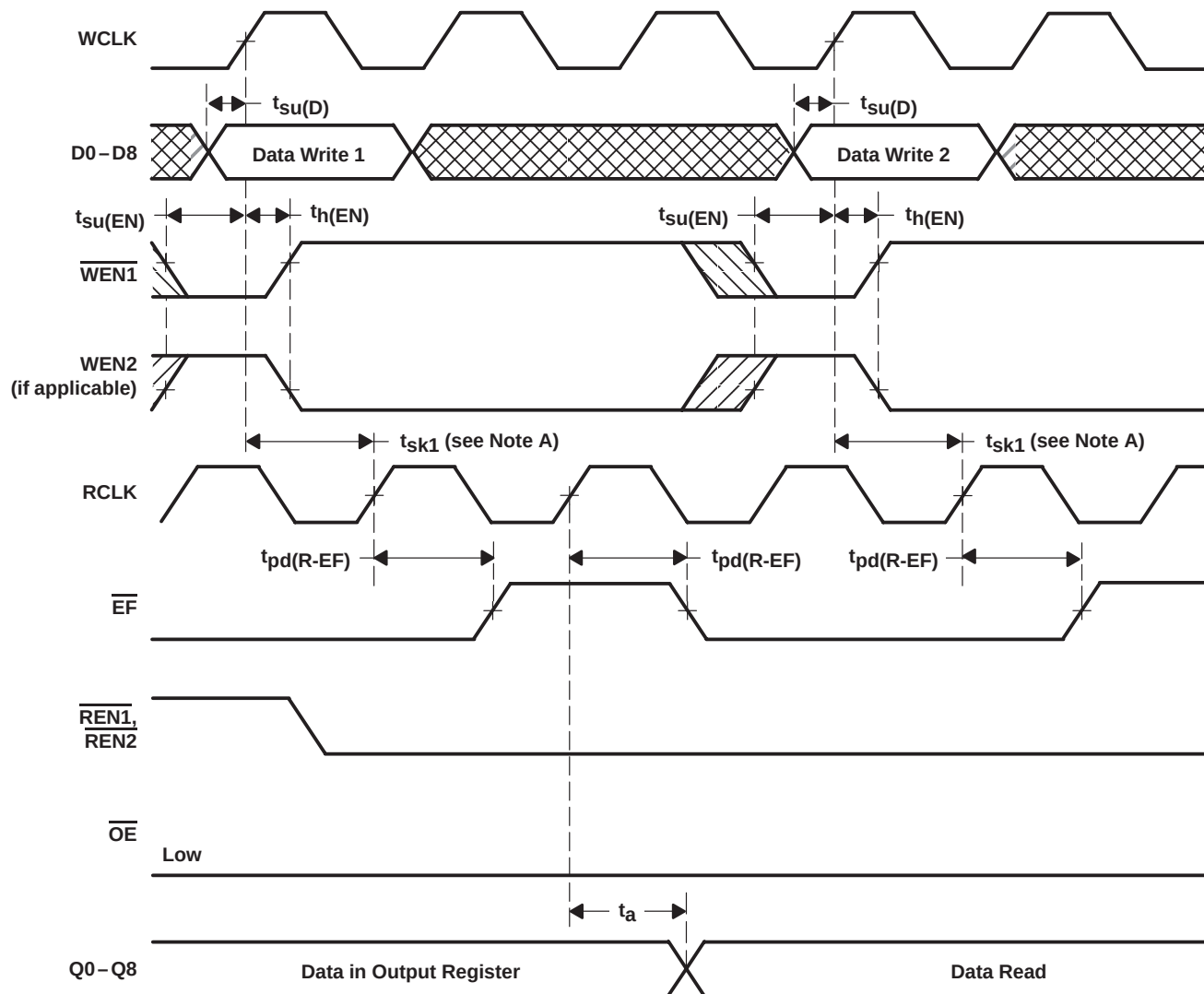
SN74ACT72211L, SN74ACT7221L, SN74ACT72231L, SN74ACT72241L
 512 × 9, 1024 × 9, 2048 × 9, AND 4096 × 9
 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

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NOTE A: t_{sk1} is the minimum time between a rising RCLK edge and a subsequent rising WCLK edge for $\overline{FF}$ to change logic levels during the current clock cycle. If the time between the rising edge of RCLK and the subsequent rising edge of WCLK is less than t_{sk1} , then $\overline{FF}$ may not change its logic level until the next WCLK rising edge.

Figure 6. Full-Flag Timing

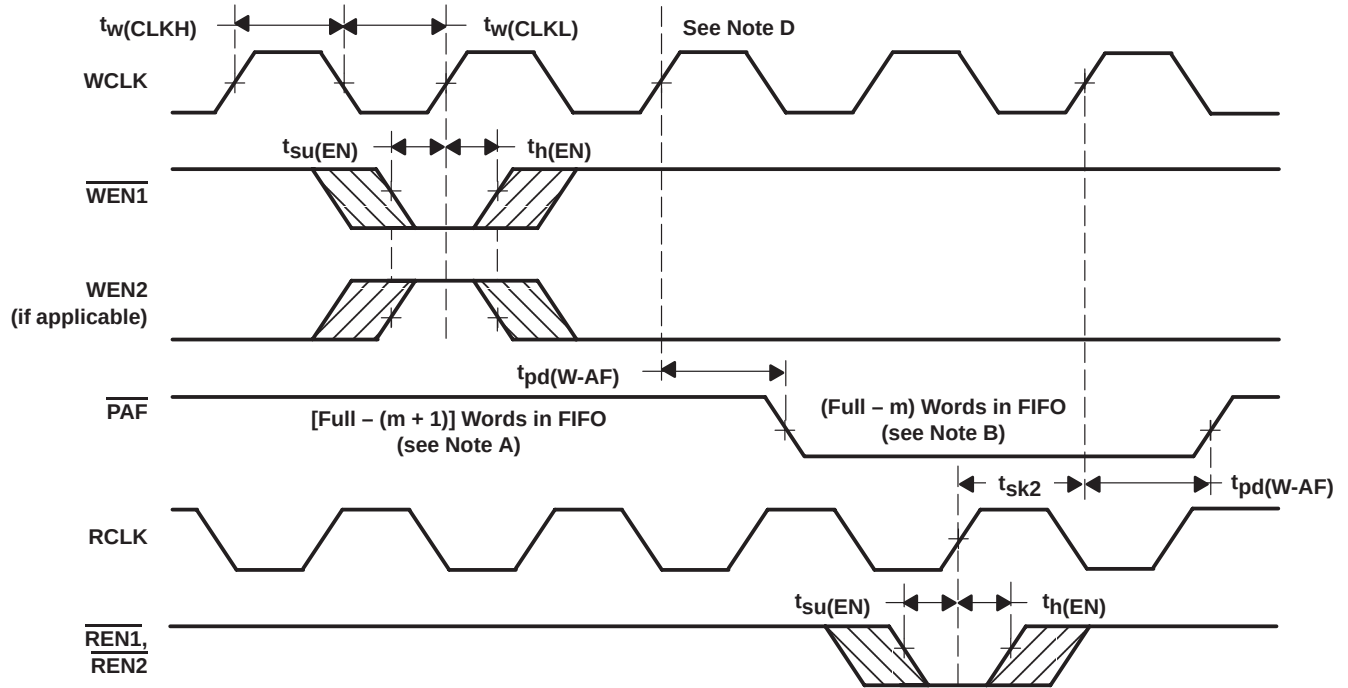


NOTE A: t_{sk1} is the minimum time between a rising WCLK edge and a subsequent rising RCLK edge for $\overline{EF}$ to change logic levels during the current clock cycle. If the time between the rising edge of WCLK and the subsequent rising edge of RCLK is less than t_{sk1} , then $\overline{EF}$ may not change its logic level until the next RCLK rising edge.

Figure 7. Empty-Flag Timing

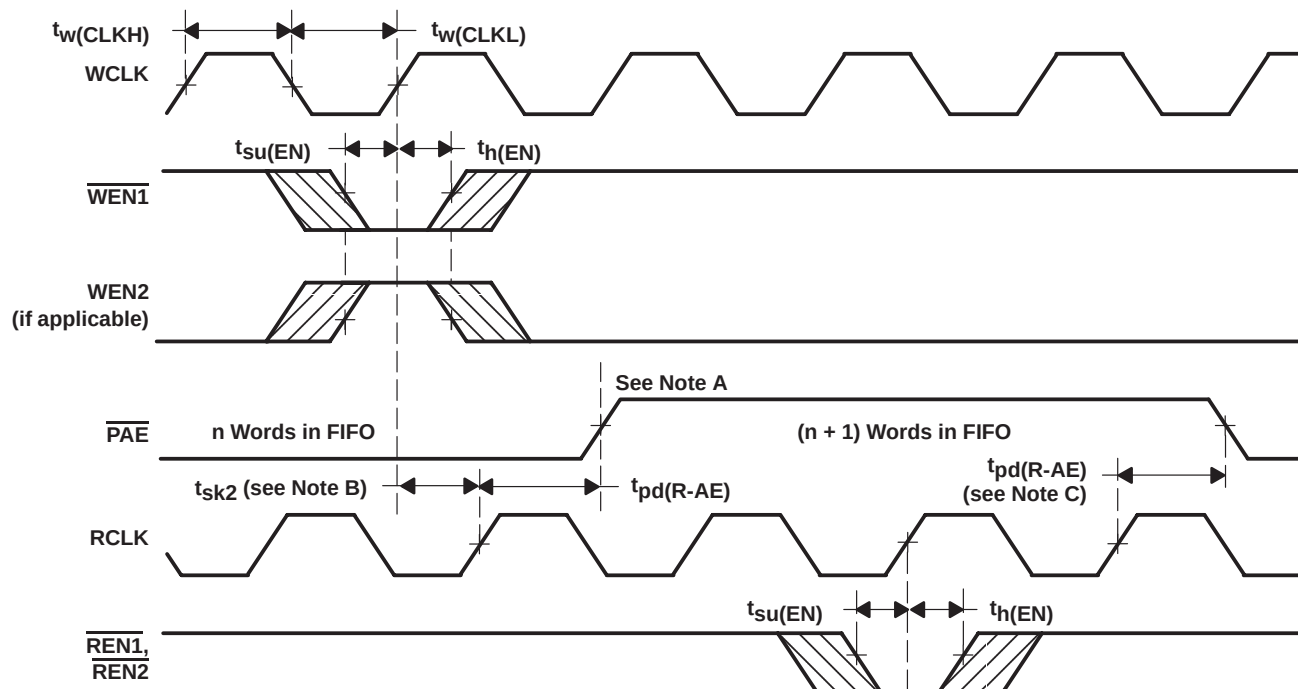
SN74ACT72211L, SN74ACT72221L, SN74ACT72231L, SN74ACT72241L
 512 × 9, 1024 × 9, 2048 × 9, AND 4096 × 9
 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

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- NOTES: A. $\overline{PAF}$ offset = m
 B. $(512 - m)$ words for SN74ACT72211L, $(1024 - m)$ words for SN74ACT72221L, $(2048 - m)$ words for SN74ACT72231L, $(4096 - m)$ words for SN74ACT72241L
 C. t_{sk2} is the minimum time between a rising RCLK edge and the subsequent rising WCLK edge for $\overline{PAF}$ to change its logic level during that clock cycle. If the time between the rising edge of RCLK and the subsequent rising edge of WCLK is less than t_{sk2} , then $\overline{PAF}$ may not change its logic level until the next WCLK rising edge.
 D. If a write is performed on this rising edge of the write clock, there will be $[Full - (m - 1)]$ words in the FIFO when $\overline{PAF}$ goes low.

Figure 8. Programmable Almost-Full Flag Timing

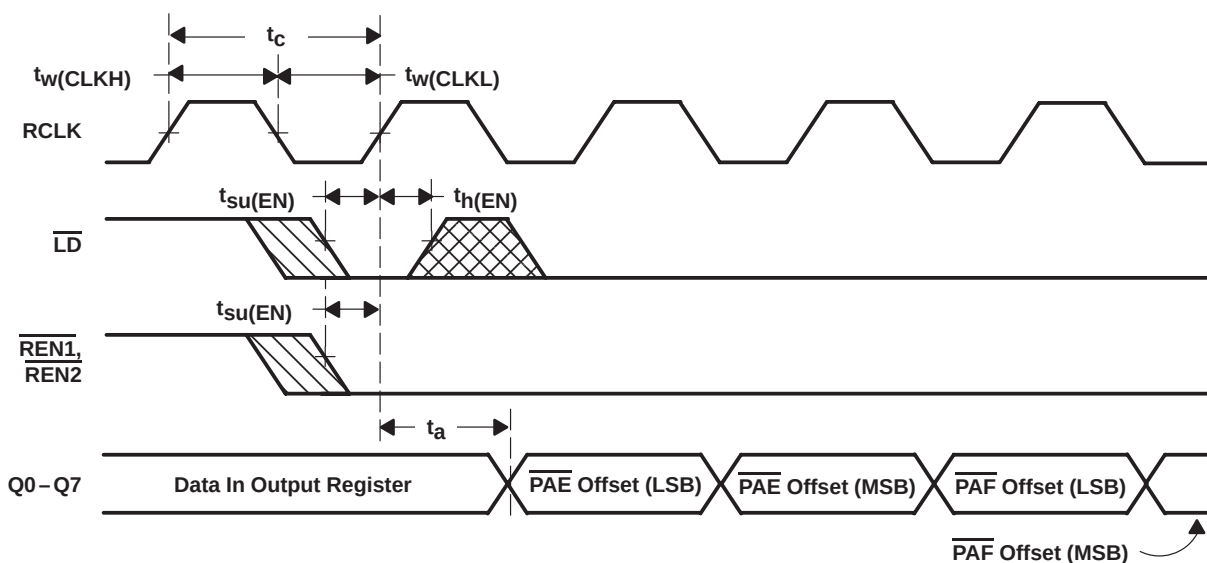
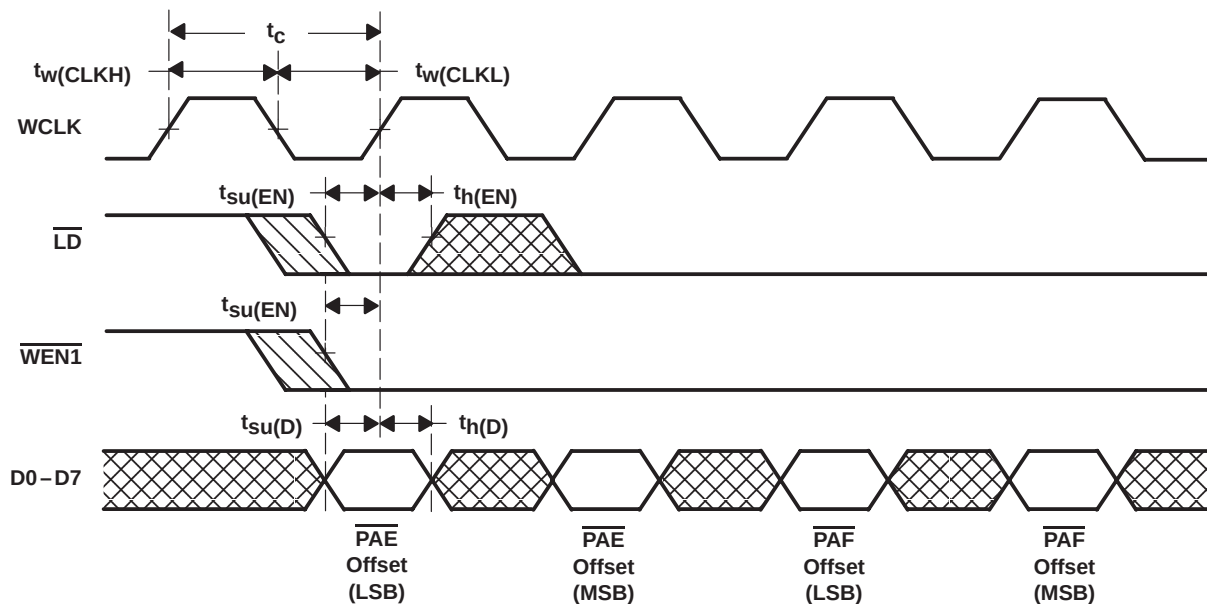


NOTES: A. $\overline{\text{PAE}}$ offset = n

B. t_{sk2} is the minimum time between a rising WCLK edge and the subsequent rising RCLK edge for $\overline{\text{PAE}}$ to change its logic level during that clock cycle. If the time between the rising edge of WCLK and the subsequent rising edge of RCLK is less than t_{sk2} , then $\overline{\text{PAE}}$ may not change its logic level until the next RCLK rising edge.

C. If a write is performed on this rising edge of the write clock, there will be [Empty + (n - 1)] words in the FIFO when $\overline{\text{PAE}}$ goes low.

Figure 9. Programmable Almost-Empty Flag Timing



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Input voltage range, any input, V_I (see Note 1)	–0.5 V to 7 V
Continuous output current, I_O	±50 mA
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range under bias	–55°C to 125°C
Storage temperature range	–55°C to 125°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			–2	mA
I_{OL} Low-level output current			8	mA
T_A Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH} High-level output voltage	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -2\text{ mA}$	2.4		V
V_{OL} Low-level output voltage	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 8\text{ mA}$		0.4	V
I_I Input current	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or 0 V		±1	μA
I_{OZ} High-impedance output current	$V_{CC} = 5.5\text{ V}$, $V_O = V_{CC}$ or 0 V		±10	μA
$C_i^{\ddagger}$ Input capacitance	$V_I = 0$, $f = 1\text{ MHz}$		10	pF
$C_o^{\ddagger}$ Output capacitance	$V_O = 0$, $f = 1\text{ MHz}$, $\overline{OE} \geq V_{IH}$		10	pF
I_{CC}^{∇} Active supply current	$f_{clock} = 20\text{ MHz}$	SN74ACT72211L		140 [§]
		SN74ACT72221L, SN74ACT72231L, SN74ACT72241L		160 [#]
				mA

[‡] Specified by design but not tested

[§] I_{CC} measurements are made with outputs open (only capacitive loading). Typical $I_{CC} = 65 + (f_{clock} \times 1.1/\text{MHz}) + (f_{clock} \times C_L \times 0.03/\text{MHz-pF})$ mA (C_L = external capacitive load).

[¶] The I_{CC} limits are valid for $t_C = 15, 20, 25$, and 50 ns.

[#] I_{CC} measurements are made with outputs open (only capacitive loading). Typical $I_{CC} = 80 + (f_{clock} \times 2.1/\text{MHz}) + (f_{clock} \times C_L \times 0.03/\text{MHz-pF})$ mA (C_L = external capacitive load).

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 2 through 13)

		'ACT72211L-15 'ACT72221L-15 'ACT72231L-15 'ACT72241L-15	'ACT72211L-20 'ACT72221L-20 'ACT72231L-20 'ACT72241L-20	'ACT72211L-25 'ACT72221L-25 'ACT72231L-25 'ACT72241L-25	'ACT72211L-50 'ACT72221L-50 'ACT72231L-50 'ACT72241L-50	UNIT
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
f_{clock}	Clock frequency, RCLK or WCLK	66.7		50		MHz
t_c	Clock cycle time, RCLK or WCLK	15 [†]		20		ns
$t_{w(\text{CLKH})}$	Pulse duration, RCLK or WCLK high	6		8		ns
$t_{w(\text{CLKL})}$	Pulse duration, RCLK or WCLK low	6		8		ns
$t_{w(\text{RS})}$	Pulse duration, $\overline{\text{RS}}$ low	15		20		ns
$t_{\text{su}}(\text{D})$	Setup time, D0–D8 before RCLK $\uparrow$	4		5		ns
$t_{\text{su}}(\text{EN})$	Setup time, $\overline{\text{WEN1}}$, $\overline{\text{WEN2}}^\ddagger$, and $\overline{\text{LD}}^\S$ before WCLK $\uparrow$; $\overline{\text{REN1}}$, $\overline{\text{REN2}}$, and $\overline{\text{LD}}^\S$ before RCLK $\uparrow$	4		5		ns
$t_{\text{su}}(\text{RS})$	Setup time, $\overline{\text{REN1}}$, $\overline{\text{REN2}}$, $\overline{\text{WEN1}}$, and $\overline{\text{WEN2}}/\overline{\text{LD}}$ before $\overline{\text{RS}}$ high	15		20		ns
$t_{\text{h}}(\text{D})$	Hold time, D0–D8 after RCLK $\uparrow$	1		1		ns
$t_{\text{h}}(\text{EN})$	Hold time, $\overline{\text{WEN1}}$, $\overline{\text{WEN2}}^\ddagger$, and $\overline{\text{LD}}^\S$ after WCLK $\uparrow$; $\overline{\text{REN1}}$, $\overline{\text{REN2}}$, and $\overline{\text{LD}}^\S$ after RCLK $\uparrow$	1		1		ns
$t_{\text{h}}(\text{RS})$	Hold time, $\overline{\text{REN1}}$, $\overline{\text{REN2}}$, $\overline{\text{WEN1}}$, and $\overline{\text{WEN2}}/\overline{\text{LD}}$ after $\overline{\text{RS}}$ high	15		20		ns
t_{sk1}	Skew time between RCLK $\uparrow$ and WCLK $\uparrow$ to allow $\overline{\text{EF}}$ or $\overline{\text{FF}}$ to change logic levels during the current clock cycle	6		8		ns
t_{sk2}	Skew time between RCLK $\uparrow$ and WCLK $\uparrow$ to allow $\overline{\text{PAF}}$ or $\overline{\text{PAE}}$ to change logic levels during the current clock cycle	28		35		ns

[†] Valid for $\overline{\text{PAE}}$ or $\overline{\text{PAF}}$ program values as follows:

≤ 63 bytes from the respective boundary for the SN74ACT72211L;

≤ 511 bytes from the respective boundary for the SN74ACT72221L/-72231L/-72241L;

minimum t_c is 20 ns for program values greater than those indicated above.

[‡] Applicable when the device is configured with two write-enable inputs ($\overline{\text{WEN2}}/\overline{\text{LD}} = \overline{\text{WEN2}}$).

[§] Applicable when the device is configured to have programmable flags ($\overline{\text{WEN2}}/\overline{\text{LD}} = \overline{\text{LD}}$).

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 2 through 13)

PARAMETER		'ACT72211L-15 'ACT72221L-15 'ACT72231L-15 'ACT72241L-15		'ACT72211L-20 'ACT72221L-20 'ACT72231L-20 'ACT72241L-20		'ACT72211L-25 'ACT72221L-25 'ACT72231L-25 'ACT72241L-25		'ACT72211L-50 'ACT72221L-50 'ACT72231L-50 'ACT72241L-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, RCLK↑ to Q0–Q8 valid	2	10	2	12	3	15	3	25	ns
$t_{pd(OE-Q)}$	Propagation delay time, $\overline{OE}$ low to Q0–Q8 valid	3	8	3	10	3	13	3	28	ns
$t_{pd(R-EF)}$	Propagation delay time, RCLK↑ to $\overline{EF}$ low or high		10		12		15		30	ns
$t_{pd(W-FF)}$	Propagation delay time, WCLK↑ to $\overline{FF}$ low or high		10		12		15		30	ns
$t_{pd(R-AE)}$	Propagation delay time, RCLK↑ to $\overline{PAE}$ low or high		10		12		15		30	ns
$t_{pd(W-AF)}$	Propagation delay time, WCLK↑ to $\overline{PAF}$ low or high		10		12		15		30	ns
$t_{pd(RS-O)}$	Propagation delay time, $\overline{RS}$ low to $\overline{FF}$ and $\overline{PAF}$ high and $\overline{EF}$, $\overline{PAE}$, and Q0–Q8 low		15		20		25		50	ns
t_{en}	Enable time, $\overline{OE}$ low to Q0–Q8 at the low-impedance level†	0		0		0		0		ns
t_{dis}	Disable time, $\overline{OE}$ high to Q0–Q8 at the high-impedance level†	3	8	3	10	3	13	3	28	ns

† These values are characterized but not tested.

APPLICATION INFORMATION

width-expansion configuration

Word width is increased by connecting the corresponding input control signals of multiple devices. Composite empty and full flags should be created by monitoring all devices in width expansion. Almost-full and almost-empty status can be obtained from any one device. Figure 12 shows an 18-bit-wide data path formed by using two SN74ACT72211L/72221L/72231L/72241L devices.

In Figure 12, read enable 2 ($\overline{\text{REN2}}$) is grounded and read enable 1 ($\overline{\text{REN1}}$) acts as the only read control. The write enable 2/load (WEN2/LD) input of only one device is set low at reset to configure the device for programmable flags and to have it act as a load control for reading and writing the programmable flag offset registers.

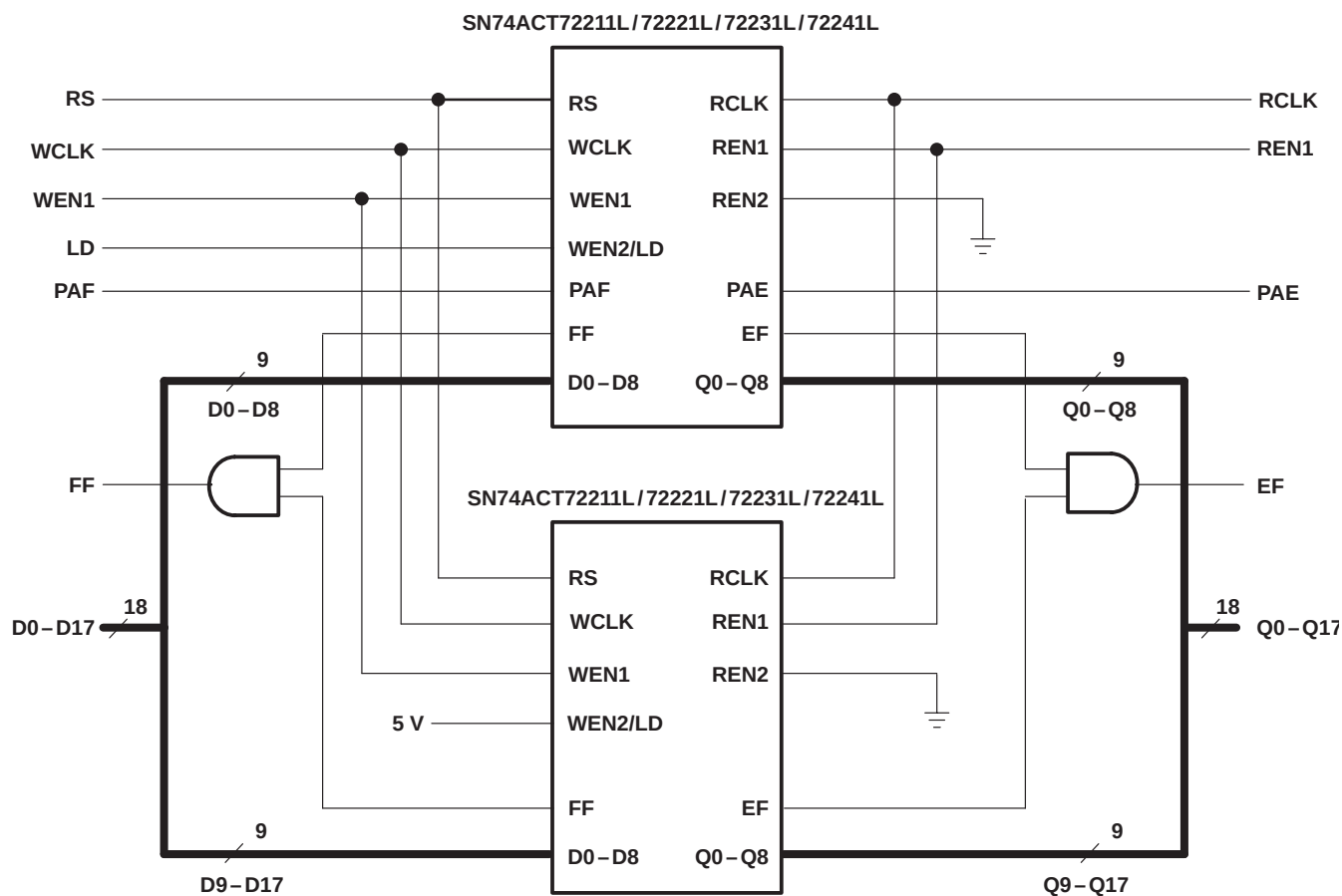
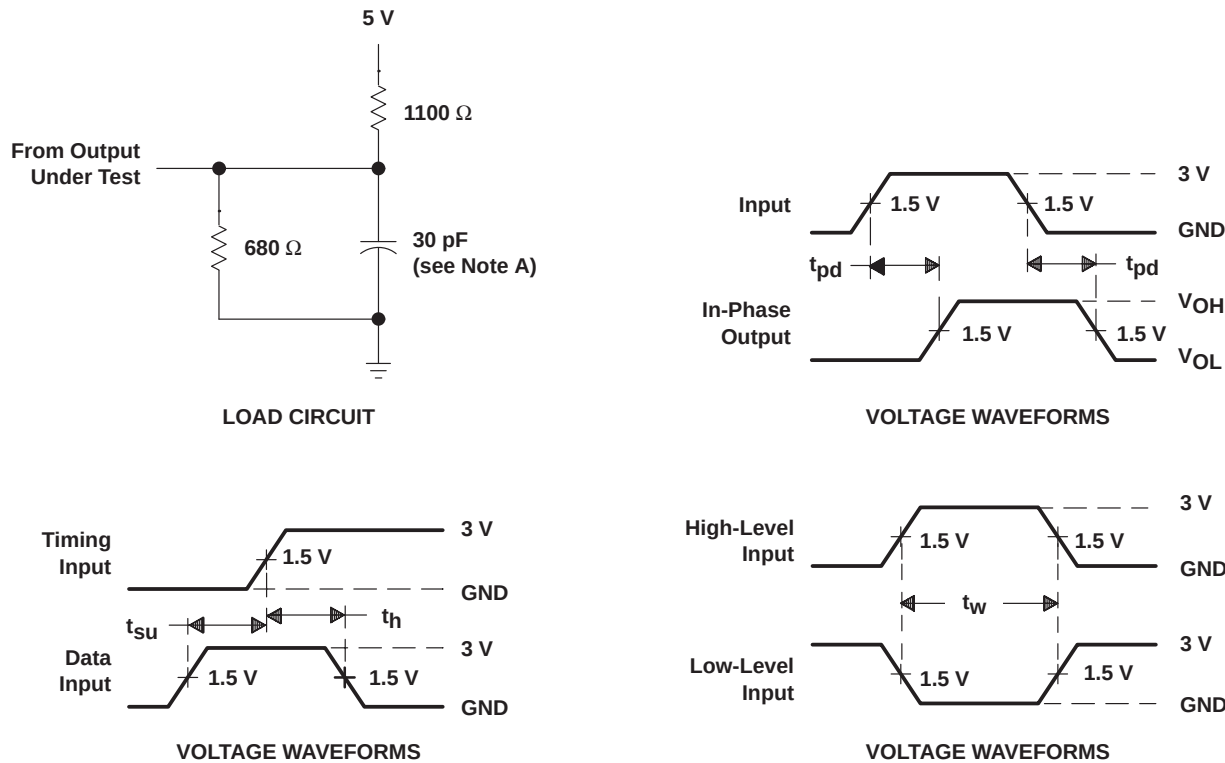


Figure 12. Word-Width Expansion for 512/1024/2048/4096 × 18 FIFO

PARAMETER MEASUREMENT INFORMATION



NOTE A: Includes probe and jig capacitance

Figure 13. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ACT72211L15RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L20RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L20RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L25RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L35RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L50RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L50RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L15RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L20RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L25RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L35RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72211L50RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72231L15RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72231L20RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72231L20RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72231L25RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72231L35RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72231L50RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72241L15RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72241L20RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72241L20RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72241L25RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72241L35RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT72241L50RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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