TARGET DATASHEET Rev. 0.6 (4.03)

Features

- High Performance:

Speed Sorts	-5 DDR2 -400	-3.7 DDR2 -533	-3 DDR2 -667	Units
Bin (CL-tRCD-tRP)	3-3-3	4-4-4	4-4-4	tck
max. Clock Frequency	200	266	333	MHz
Data Rate	400	533	667	Mb/s/pin
$\overline{CAS}$ Latency	3	4	4	tck
tRCD	15	15	12	ns
tRP	15	15	12	ns
tRC	60	60	57	ns

- 1.8V ± 0.1V Power Supply Voltage
- 8 internal memory banks, selectable by three bank address bits
- Programmable $\overline{CAS}$ Latency: 3, 4 and 5
- Programmable Additive Latency: 0, 1, 2, 3 and 4

- Write Latency = Read Latency -1
- Programmable Burst Length: 4 and 8
- Programmable Sequential / Interleave Burst
- OCD (Off-Chip Driver Impedance Adjustment)
- ODT (On-Die Termination)
- 4 bit prefetch architecture
- 1k page size for x 4 & x 8, 2k page size for x16
- Data-Strobes: Bidirectional, Differential
- Strong and Weak Strength Data-Output Driver
- Auto-Refresh and Self-Refresh
- Power Saving Power-Down modes
- 7.8 µs Maximum Average Periodic Refresh Interval
- Lead and Halogen free Packages:
    60+8 pin PTFBGA for x4 & x8 components
  84+ 8 pin PTFBPA for x16 components

1.0 Description

The 1Gb Double-Data-Rate-II (DDR2) DRAMs are high-speed CMOS Double Data Rate II Synchronous DRAM devices containing 1,073,741,824 bits. It is internally configured as a octal-bank DRAM. The 1Gb chip is organized as either 64Mbit x 4 I/O x 4 bank, 32Mbit x 8 I/O x 4 bank or 16Mbit x 16 I/O x 4 bank device. These synchronous devices achieve high speed double-data-rate transfer rates of up to 667 Mb/sec/pin for general applications, and 800 Mb/sec/pin for future lightly loaded applications.

The chip is designed to comply with all key DDR2 DRAM key features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) normal and weak strength data-output driver, (4) variable data-output impedance adjustment and (5) an ODT (On-Die Termination) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion. A 17 bit address bus for x4 and x8 organised components and a 16 bit address bus for x16 components is used to convey row, column, and bank address devices.

These devices operate with a single 1.8V +/-0.1V power supply and are available in FBGA packages.

An Auto-Refresh and Self-Refresh mode is provided along with various power-saving power-down modes.

1.1 Ordering Information

Part Number	CAS Latency	Clock (MHz)	Speed Sort	DRAM Organisation	Package
HYB18T1G400AF-5	3	200	DDR2-400	8 banks x 32Mbits x 4	60 pin PTFBGA
HYB18T1G800AF-5				8 banks x 16Mbits x 8	60 pin PTFBGA
HYB18T1G160AF-5				8 banks x 8Mbits x 16	84 pin PTFBGA
HYB18T1G400AF-3.7	4	266	DDR2-533	8 banks x 32Mbits x 4	60 pin PTFBGA
HYB18T1G800AF-3.7				8 banks x 16Mbits x 8	60 pin PTFBGA
HYB18T1G160AF-3.7				8 banks x 8Mbits x 16	84 pin PTFBGA
HYB18T1G400AF-3	4	333	DDR2-667	8 banks x 32Mbits x 4	60 pin PTFBGA
HYB18T1G800AF-3				8 banks x 16Mbits x 8	60 pin PTFBGA
HYB18T1G160AF-3				8 banks x 8Mbits x 16	84 pin PTFBGA

Notes: 1.) All packages are lead and halogen free
2.) For product nomenclature see section 10 of this datasheet

1.2 Pin Description

1.2.1 x4 Components

Symbol	Function	Symbol	Function
A0~A13	Row Address Inputs	DQS, $\overline{DQS}$	Differential Data Strobes
A0~A9,A11	Column Address Inputs	NC	No Connection (Chip to Pin)
BA0, BA1, BA2	Bank Address Inputs	VDD	Supply Voltage
A10/AP	Column Address Input for Auto-Precharge	VSS	Ground
$\overline{CS}$	Chip Select	VDDQ	Supply Voltage for DQ
$\overline{RAS}$	Row Address Strobe	VSSQ	Ground for DQs
$\overline{CAS}$	Column Address Strobe	VDDL	Supply Voltage for DLL
$\overline{WE}$	Write Enable	VSSDL	Ground for DLL
DQ0~DQ3	Data Inputs/Outputs (x4)	VREF	Reference Voltage for SSTL Inputs
CKE	Clock Enable	ODT	On Die Termination Enable
CK, $\overline{CK}$	Differential Clock Inputs	NC	Not connected
DM	Data Input Mask		

1.2.1 x8 Components

Symbol	Function	Symbol	Function
A0~A13	Row Address Inputs	DQS, $\overline{DQS}$	Differential Data Strobes
A0~A9	Column Address Inputs	RDQS, $\overline{RDQS}$	Differential Read Data Strobes
BA0, BA1, BA2	Bank Address Inputs	VDD	Supply Voltage
A10/AP	Column Address Input for Auto-Precharge	VSS	Ground
$\overline{CS}$	Chip Select	VDDQ	Supply Voltage for DQ
$\overline{RAS}$	Row Address Strobe	VSSQ	Ground for DQs
$\overline{CAS}$	Column Address Strobe	VDDL	Supply Voltage for DLL
$\overline{WE}$	Write Enable	VSSDL	Ground for DLL
DQ0~DQ7	Data Inputs/Outputs (x8)	VREF	Reference Voltage for SSTL Inputs
CKE	Clock Enable	ODT	On Die Termination Enable
CK, $\overline{CK}$	Differential Clock Inputs	NC	Not connected
DM	Data Input Mask		

1.2.3 x16 Components

Symbol	Function	Symbol	Function
A0~A12	Row Address Inputs	LDQS,$\overline{LDQS}$ UDQS,$\overline{UDQS}$	Differential Data Strobes
A0~A9	Column Address Inputs	NC	No Connection (Chip to Pin)
BA0, BA1, BA2	Bank Address Inputs	VDD	Supply Voltage
A10/AP	Column Address Input for Auto-Precharge	VSS	Ground
$\overline{CS}$	Chip Select	VDDQ	Supply Voltage for DQ
$\overline{RAS}$	Row Address Strobe	VSSQ	Ground for DQs
$\overline{CAS}$	Column Address Strobe	VDDL	Supply Voltage for DLL
$\overline{WE}$	Write Enable	VSSDL	Ground for DLL
LDQ0~7, UDQ0~7	Data Inputs/Outputs	VREF	Reference Voltage for SSTL Inputs
CKE	Clock Enable	ODT	On Die Termination Enable
CK, $\overline{CK}$	Differential Clock Inputs	NC	Not connected
LDM, UDM	Data Input Masks		

1.3 1Gbit DDR2 Addressing

Configuration	256Mb x 4	128Mb x 8	64Mb x 16
# of Banks	8	8	8
Bank Address	BA0, BA1, BA2	BA0, BA1, BA2	BA0, BA1, BA2
Auto-Precharge	A10 / AP	A10 / AP	A10 / AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9, A11	A0 ~ A9	A0 ~ A9
Page Size	1024 (1kB)	1024 (1kB)	2048 (2kB)

note: page size in bytes = $2^{colbits}$ x ORG / 8, where colbits is the number of column address bits and ORG the number of I/O (DQ) bits.

1.4 Package Pinout & Addressing

1.4.1 Package Pinout for x4 components, 60 pins + 8 support pins, FBGA Package (top view)

	1	2	3			7	8	9
A	NC	NC					NC	NC
B								
C								
D								
E	VDD	NC	VSS			VSSQ	$\overline{DQS}$	VDDQ
F	NC	VSSQ	DM			DQS	VSSQ	NC
G	VDDQ	DQ1	VDDQ			VDDQ	DQ0	VDDQ
H	NC	VSSQ	DQ3			DQ2	VSSQ	NC
J	VDDL	VREF	VSS			VSSDL	CK	VDD
K		CKE	$\overline{WE}$			$\overline{RAS}$	$\overline{CK}$	ODT
L	BA2	BA0	BA1			$\overline{CAS}$	$\overline{CS}$	
M		A10	A1			A2	A0	VDD
N	VSS	A3	A5			A6	A4	
P		A7	A9			A11	A8	VSS
R	VDD	A12	NC(A14)			NC,(A15)	A13	
T								
U								
V								
W	NC	NC					NC	NC

Notes:
1) VDDL and VSSDL are power and ground for the DLL.They are isolated on the device from VDD, VDDQ, VSS and VSSQ.
2) NC, (A14) andNC,A15) are additional address pins for future generation DRAMs and are not connected on this component.

1.4.2 Package Pinout for x8 components, 60 pins + 8 support pins, FBGA Package (top view)

1	2	3		7	8	9
NC	NC		A		NC	NC
			B			
			C			
			D			
VDD	$\overline{\text{NU, RDQS}}$	VSS	E	VSSQ	$\overline{\text{DQS}}$	VDDQ
DQ6	VSSQ	DM , RDQS	F	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	K	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA1	L	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC,(A14)	R	NC,(A15)	A13	
			T			
			U			
			V			
NC	NC		W		NC	NC

Notes:

1) RDQS / $\overline{\text{RDQS}}$ are enabled by EMRS(1) command.
2) If RDQS / $\overline{\text{RDQS}}$ is enabled, the DM function is disabled
3) When enabled, RDQS & $\overline{\text{RDQS}}$ are used as strobe signals during reads.
4) VDDL and VSSDL are power and ground for the DLL. They are isolated on the device from VDD, VDDQ, VSS and VSSQ.
5) NC,(A14) and NC,(A15) are additional address pins for future generation DRAMs and are not connected on this component.
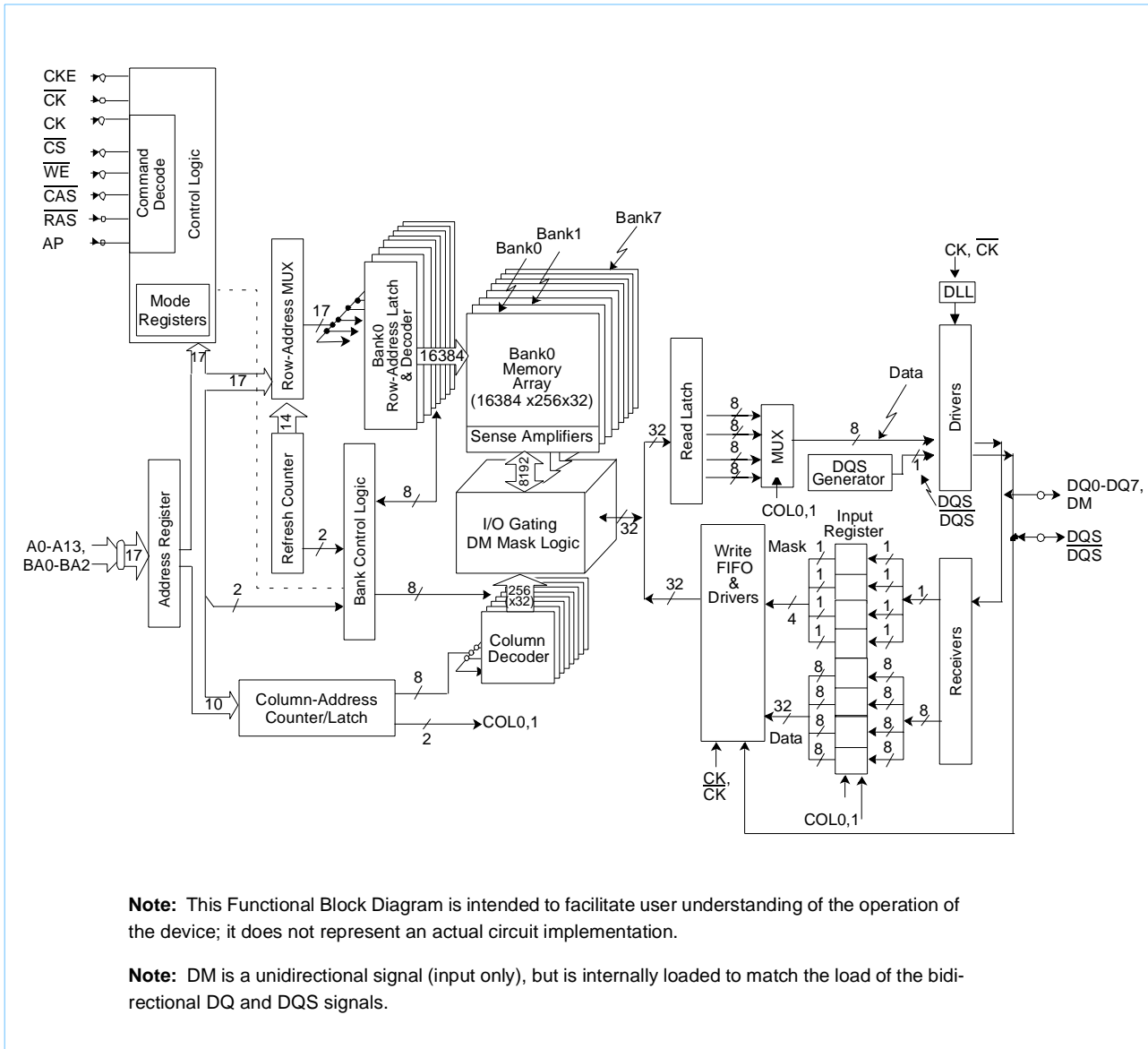
1.4.3 Package Pinout for x16 components 84 pins + 8 support pins, FBGA Package (top view)

1	2	3		7	8	9
NC	NC		**A**		NC	NC
			B			
			C			
VDD	NC	VSS	**D**	VSSQ	$\overline{\text{UDQS}}$	VDDQ
UDQ6	VSSQ	UDM	**E**	UDQS	VSSQ	UDQ7
VDDQ	UDQ1	VDDQ	**F**	VDDQ	UDQ0	VDDQ
UDQ4	VSSQ	DQ3	**G**	UDQ2	VSSQ	UDQ5
VDD	NC	VSS	**H**	VSSQ	$\overline{\text{LDQS}}$	VDDQ
LDQ6	VSSQ	LDM	**J**	LDQS	VSSQ	LDQ7
VDDQ	LDQ1	VDDQ	**K**	VDDQ	LDQ0	VDDQ
LDQ4	VSSQ	LDQ3	**L**	LDQ2	VSSQ	LDQ5
VDDL	VREF	VSS	**M**	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	**N**	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA1	**P**	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10	A1	**R**	A2	A0	VDD
VSS	A3	A5	**T**	A6	A4	
	A7	A9	**U**	A11	A8	VSS
VDD	A12	NC,(A14)	**V**	NC,(A15)	NC,(A13)	
			W			
			X			
NC	NC		**AA**		NC	NC

Notes:

1) UDQS/$\overline{\text{UDQS}}$ is data strobe for upper byte, LDQS/$\overline{\text{LDQS}}$ is data strobe for lower byte

2) UDM is the data mask signal for the upper byte UDQ0~UDQ7, LDM is the data mask signal for the lower byte LDQ0~LDQ7

3) NC,(A13), NC,(A14) and NC,(A15) are additional address pins for future generation DRAMs and are not connected on this component.

1.5 Input/Output Functional Description

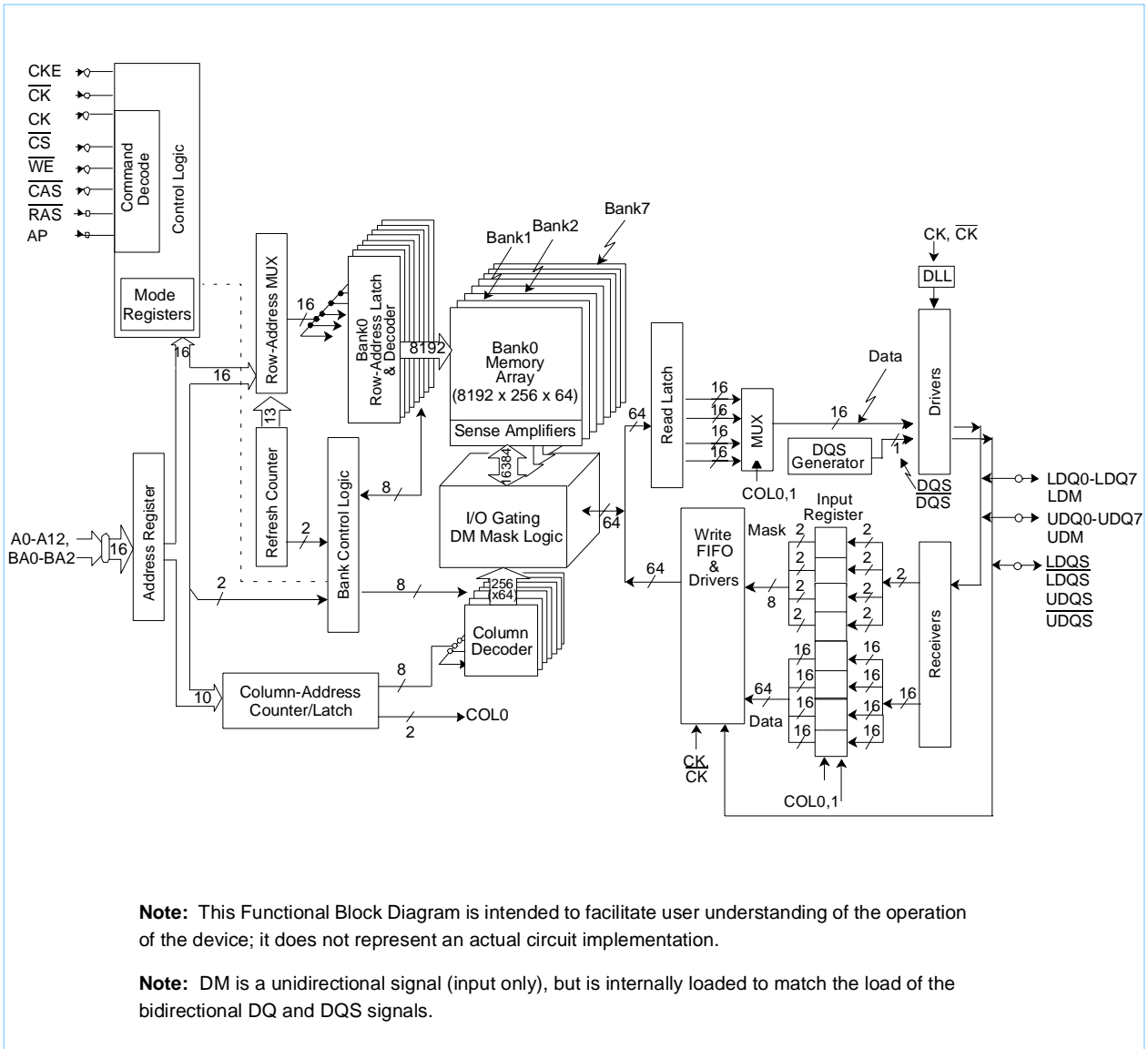| Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential system clock inputs. All address and control inputs are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) dara is referenced to the crossing of CK and $\overline{CK}$ (both direction of crossing)
CKE	Input	**Clock Enable:** CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during dower-down. Input buffers, excluding CKE are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All command are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inouts:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered
DM, LDM, UDM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. LDM and UDM are the input mask signals for x16 components and controll the lower or upper bytes. For x8 components the data mask function is disabled, when RDQS / RQDS are enabled by EMRS(1) command.
BA0, BA1, BA2	Input	**Bank Address Inputs:** BA0, BA1, BA2 define to which of the 8 internal memory banks an Activate, Read, Write or Precharge command is being applied. BA0 and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A13	Input	**Address Inputs:** Provides the row address for Activate commands and the column address and Auto-Precharge bit A10 (=AP) for Read/Write commands to select one location out of the memory array in the respective bank. A10 (=AP) is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10=low) or all banks (A10=high). If only one bank is to be precharged, the bank is selected by BA0, BA1 and BA2. The address inputs also provide the op-code during Mode Register Set commands. Row address A13 is used on x4 and x8 components only.
DQx, LDQx,UDQx	Input/ Output	**Data Inputs/Output:** Bi-directional data bus. DQ0~DQ3 for x4 components, DQ0~DQ7 for x8 components, LDQ0~LDQ7 and UDQ0~UDQ7 for x16 components
DQS, ($\overline{DQS}$) LDQS, ($\overline{LDQS}$), UDQS,($\overline{UDQS}$)	Input/ Output	**Data Strobe:** output with read data, input with write data. Edge aligned with read data, centered with write data. For the x16, LDQS corresponds to the data on LDQ0 - LDQ7; UDQS corresponds to the data on UDQ0-UDQ7. The data strobes DQS, LDQS, UDQS may be used in single ended mode or paired with the optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables the complementary data strobe signals.
RDQS, ($\overline{RDQS}$)	Input/ Output	**Read Data Strobe:** For the x8 components a RDQS, $\overline{RDQS}$ pair can be enabled via the EMRS(1) for read timing. RDQS, $\overline{RDQS}$ is not supported on x4 and x16 components. RDQS, $\overline{RDQS}$ are edge-aligned with read data. If RDQS, $\overline{RDQS}$ is enabled, the DM function is disabled on x8 components.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM signal for x4 and DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$ and DM for x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS, $\overline{UDQS}$, LDQS, $\overline{LDQS}$, UDM and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT.
NC		**No Connect:** no internal electrical connection is present
V$_{DDQ}$	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V$_{SSQ}$	Supply	**DQ Ground**
V$_{DDL}$	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V$_{SSDL}$	Supply	**DLL Ground**
V$_{DD}$	Supply	**Power Supply:** 1.8V +/- 0.1V
V$_{SS}$	Supply	**Ground**
VREF	Supply	**Reference Voltage**
(A14~A15)	-	A14 ~ A15 are additional address pins for future generation DRAMs and are not connected on this component.

1.6 Block Diagrams

Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.
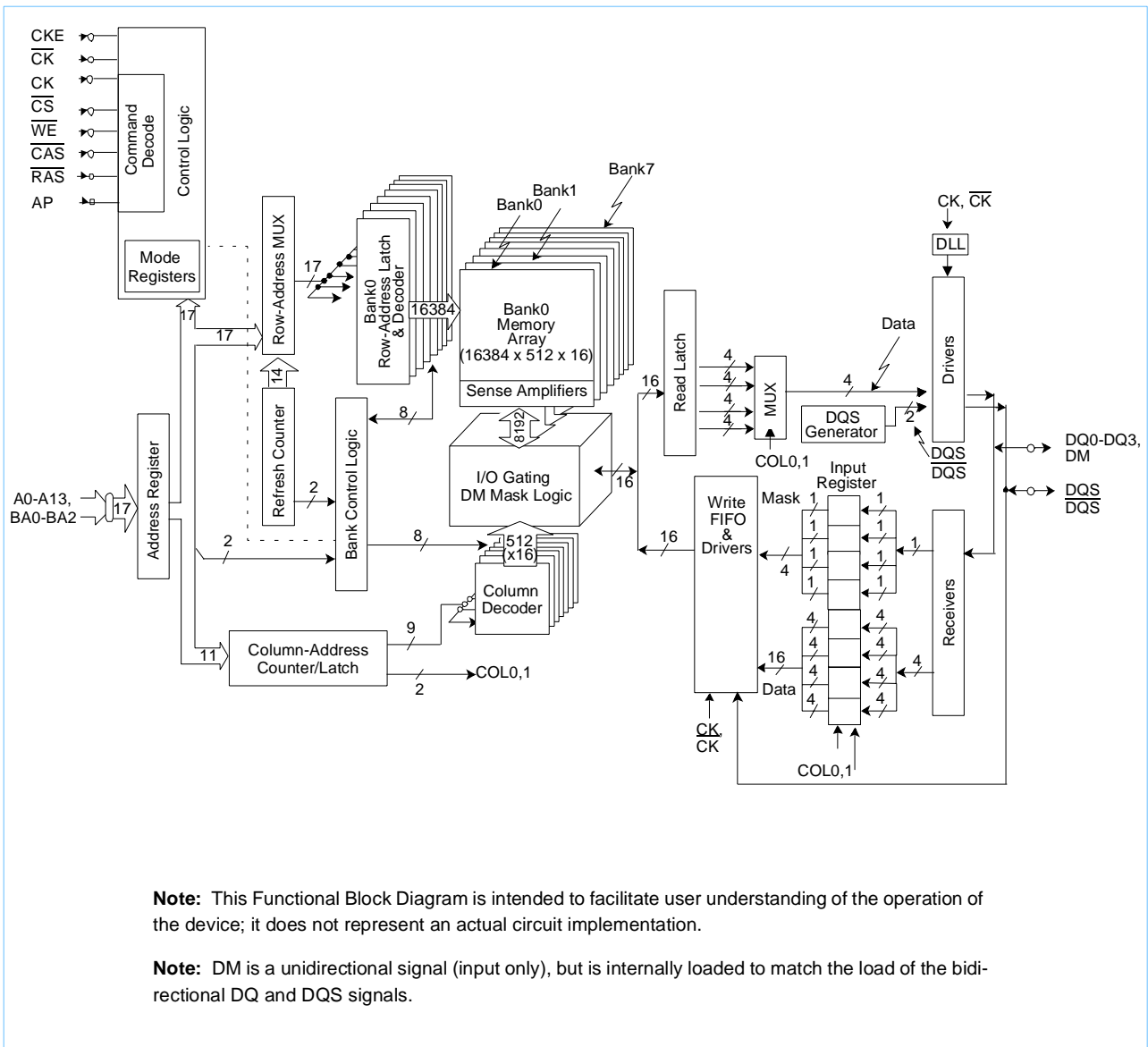
Block Diagram 64Mbit x 4 I/O x 4 Internal Memory Banks,

(128 Mbit x 4 Organisation with 14 Row, 3 Bank and 12 Column External Addresses)

Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Block Diagram 32Mbit x 8 I/O x 4 Internal Memory Banks

(64Mb x 8 Organisation with 14 Row, 3 Bank and 11 Column External Addresses)

Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Block Diagram 16Mbit x 16 I/O x 4 Internal Memory Banks

(32Mb x 16 Organisation with 13 Row, 3 Bank and 11 Column External Addresses)

2. Functional Description

2.1 Simplified State Diagram
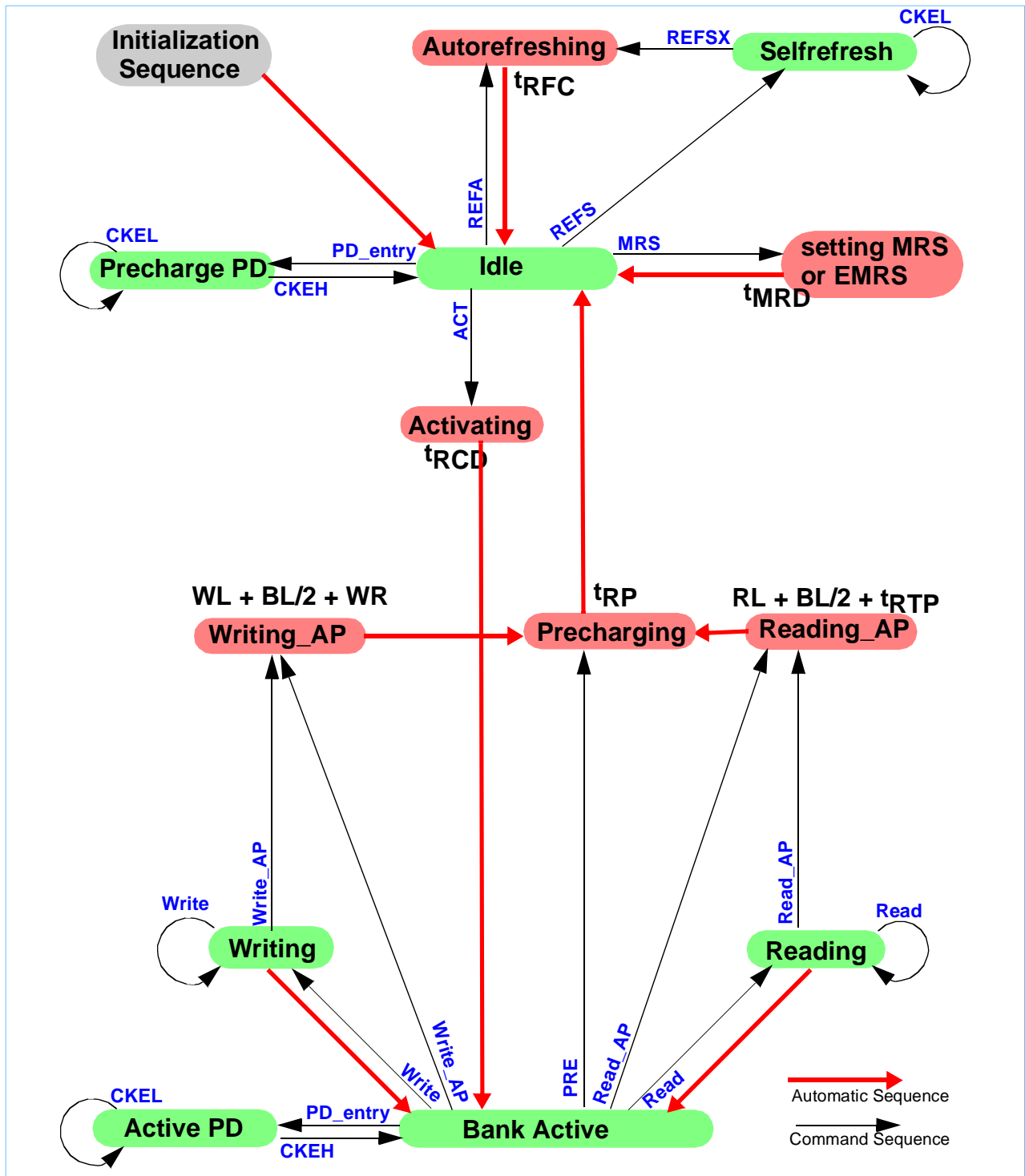
2.2 Basic Functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for the burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Activate command, which is followed by a Read or Write command. The address bits registered coincident with the activate command are used to select the bank and row to be accesses (BA0 ~ BA2 select one of the eight banks, A0-A13 select the row for x4 and x8 components, A0~A12 select the row for x16 components). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the Auto-Precharge command is to be issued. Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

2.2.1 Power On and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2 * VDDQ and ODT at a low state (all other inputs may be undefined). To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

   - VDD,VDDL and VDDQ are driven from a signle power converter output, AND
   - VTT is limited to 0.95 V max, AND
   - VREF tracks VDDQ/2
     or
   - Apply VDD before or at the same time as VDDL,
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & VREF.

   at least one of these two sets of conditions must be met.

2. Start clock (CK, $\overline{CK}$) and maintain stable power and clock condition for a minimum of 200 µs.
3. Apply NOP or Deselect commands & take CKE high.
4. Wait minimum of 400ns, then issue a Precharge-all command.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide "low" to BA0 and BA2 and "high" to BA1)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide "low" to BA2 and "high" to BA0 and BA1)
7. Issue EMRS(1) command to enable DLL. (To issue "DLL Enable" command, provide "low" to A0 and "high" to BA0 and "low" to BA1,BA2 and A13~A15)
8. Issue MRS command (Mode Register Set) for "DLL reset". (To issue DLL reset command, provide "high" to A8 and "low" to BA0 ~ BA2 and A13 ~ A15)
9. Issue Precharge-all command.
10. Issue 2 or more Auto-Refresh commands.
11. Issue a MRS command with low on A8 to initialize device operation. (i.e. to programm operating paramters with out resetting the DLL)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS OCD Default command (A9=A8=A7=1) followed by EMRS(1) OCD Calibration Mode Exit command (A9=A8=A7=0) must be issued with other parameters of EMRS(1).
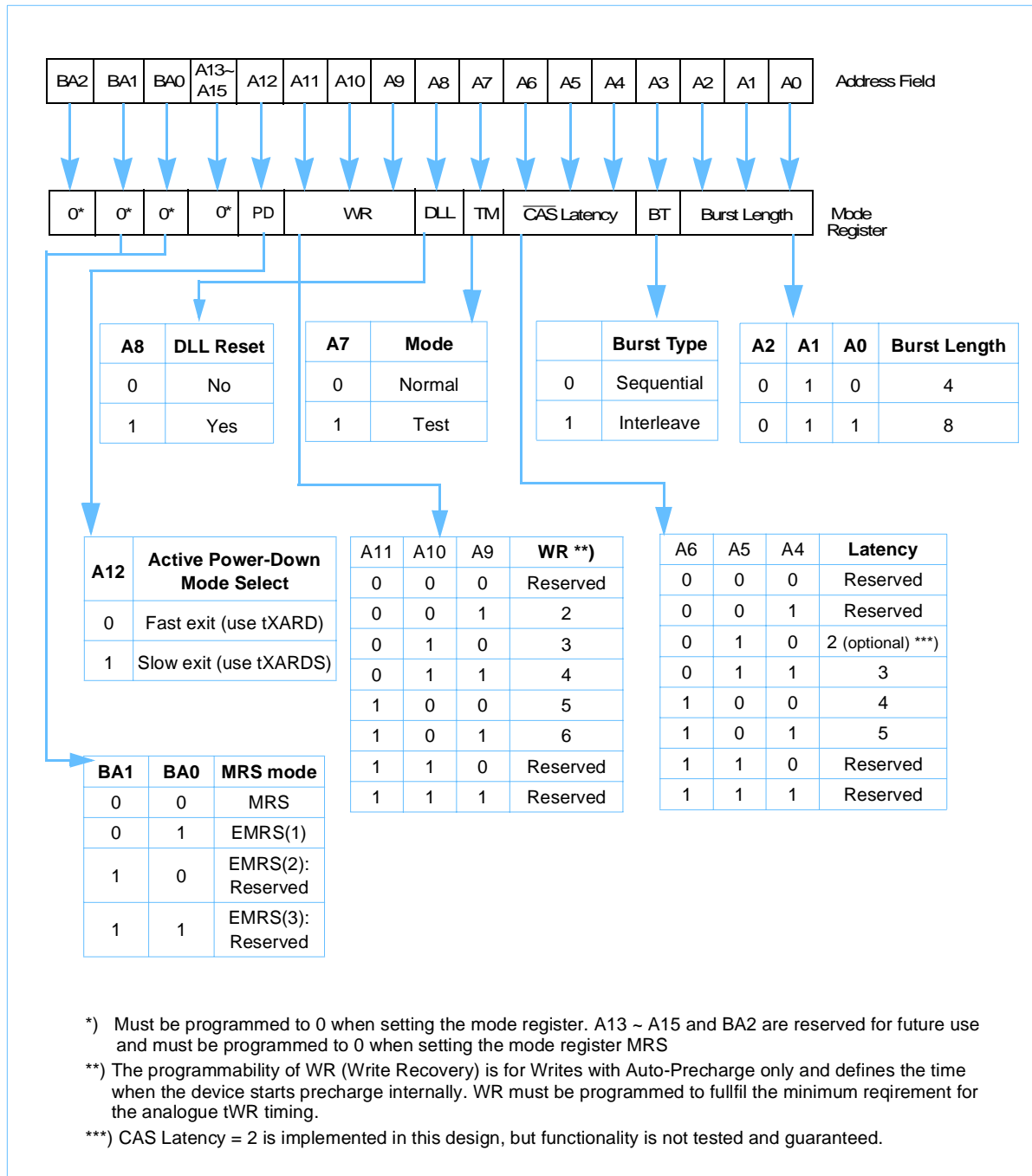13. The DDR2 SDRAM is now read for normal operation.

Example:
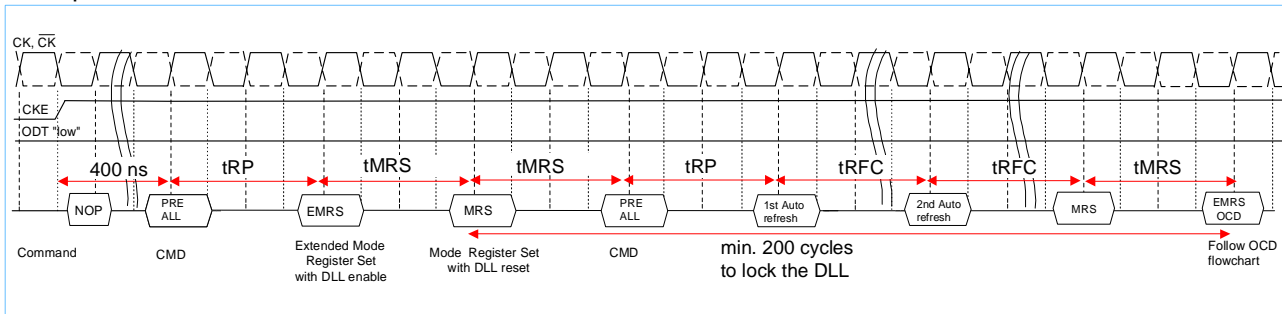
2.2.2 Programming the Mode Register and Extended Mode Registers

For application flexibility, burst length, burst type, $\overline{CAS}$ latency, DLL reset function, write recovery time (WR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, additive $\overline{CAS}$ latency, driver impedance, ODT (On Die Termination), single-ended strobe and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MRS) and Extended Node Registers (EMRS(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued. Also any programmig of EMRS(2) or EMRS(3) must be followed by programming of MRS and EMRS(1). After initial power up, all MRS and EMRS Commands must be issued before read or write cycles may begin. All banks must be in a precharged state and CKE must be high at least one cycles before the Mode Register Set Command can be issued. Either MRS or EMRS Commands are activated by the low signals of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ at the positive edge of the clock. When both bank addresses BA0 and BA1 are low, the DDR2 SDRAM enables the MRS command. When the bank addresses BA0 is high and BA1 low, the DDR2 SDRAM enables the EMRS(1) command. The address input data during this cycle defines the parameters to be set as shown in the MRS and EMRS table. A new command may be issued after the mode register set command cycle time (tMRD). MRS, EMRS and DLL Reset do not affect array contents, which means reinitializazion including those can be executed any time after power-up without affecting array contents.

2.2.2.1 DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It programs $\overline{CAS}$ latency, burst length, burst sequence, test mode, DLL reset, WR (write recovery) and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and BA1, while controlling the state of address pins A0 ~ A13. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (t$_{MRD}$) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst length. Burst address sequence type is defined by A3 and $\overline{CAS}$ latency is defined by A4 ~ A6. A7 is used for test mode and must be set to low for normal MRS operation. A8 is used for DLL reset. A9 ~ A11 are used for write recovery time (WR) definition for Auto-Precharge mode. With address bit A12 two Power-Down modes can be selected, a "standard mode" and a "low-power" Power-Down mode, where the DLL is disabled. Addess bit A13 and all "higher" address bits (including BA2) have to be set to "low" for compatibility with other DDR2 memory products with higher memory densities.
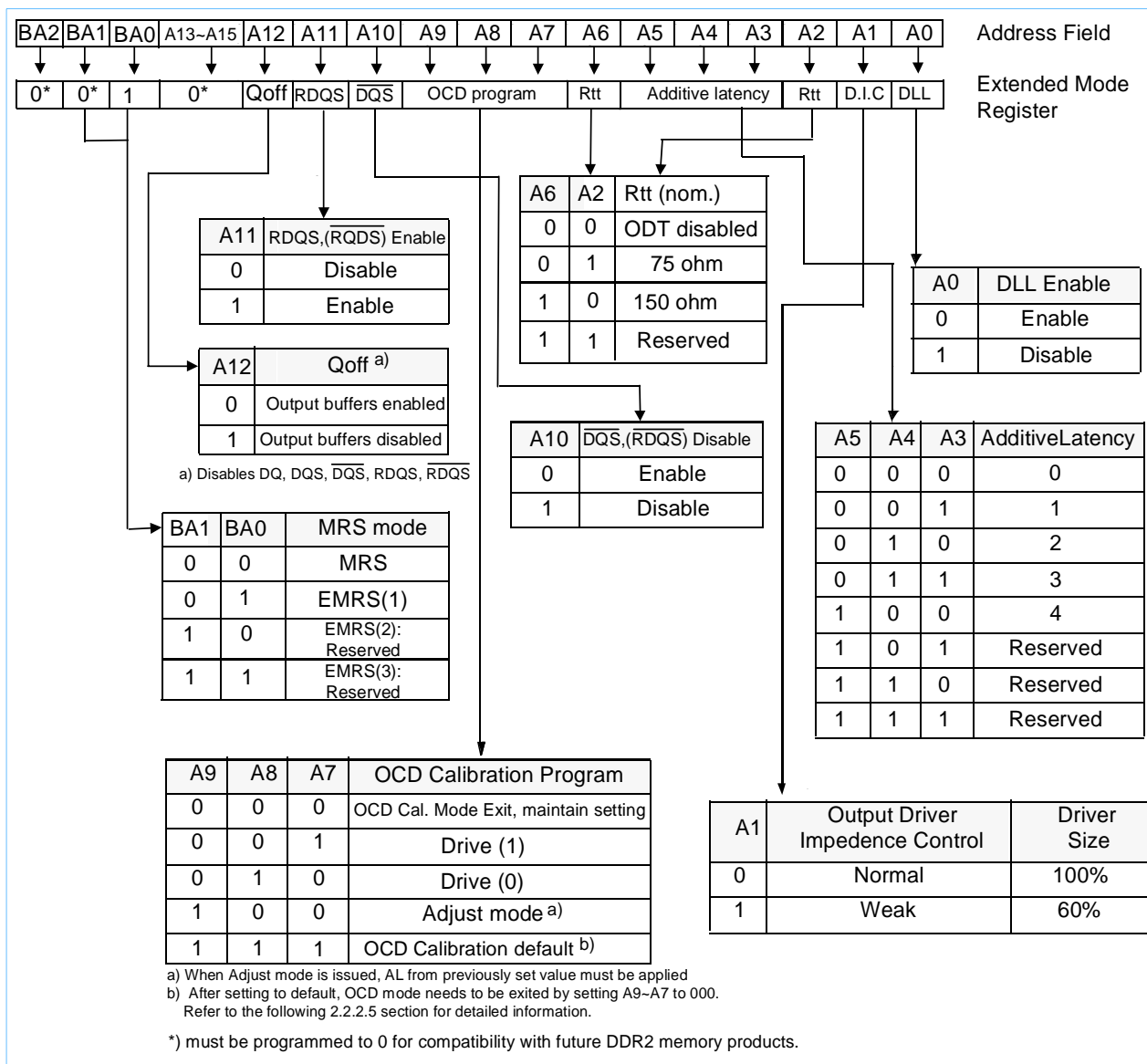
MRS Mode Register Operation Table (Address Input For Mode Set)

BA2	BA1	BA0	A13~A15	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field

0*	0*	0*	0*	PD	WR			DLL	TM	CAS Latency			BT	Burst Length			Mode Register

A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length
0	1	0	4
0	1	1	8

A12	Active Power-Down Mode Select
0	Fast exit (use tXARD)
1	Slow exit (use tXARDS)

A11	A10	A9	WR **)
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 (optional) ***)
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

*) Must be programmed to 0 when setting the mode register. A13 ~ A15 and BA2 are reserved for future use and must be programmed to 0 when setting the mode register MRS

**) The programmability of WR (Write Recovery) is for Writes with Auto-Precharge only and defines the time when the device starts precharge internally. WR must be programmed to fullfil the minimum reqirement for the analogue tWR timing.

***) CAS Latency = 2 is implemented in this design, but functionality is not tested and guaranteed.

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (EMRS(1))

The extended mode register EMRS(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, OCD program, ODT, $\overline{DQS}$ and output buffers disable, RQDS and $\overline{RDQS}$ enable. The default value of the extended mode register EMRS(1) is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA1 and high on BA0, while controlling the state of the address pins.. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the EMRS(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in precharge state.

EMRS(1) Extended Mode Register Operation Table (Address Input For Mode Set)

BA2	BA1	BA0	A13~A15	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0*	0*	1	0*	Qoff	RDQS	$\overline{DQS}$	OCD program			Rtt	Additive latency			Rtt	D.I.C	DLL	Extended Mode Register

A11	RDQS,($\overline{RQDS}$) Enable
0	Disable
1	Enable

A12	Qoff a)
0	Output buffers enabled
1	Output buffers disabled

a) Disables DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

A6	A2	Rtt (nom.)
0	0	ODT disabled
0	1	75 ohm
1	0	150 ohm
1	1	Reserved

A10	$\overline{DQS}$,($\overline{RDQS}$) Disable
0	Enable
1	Disable

A0	DLL Enable
0	Enable
1	Disable

A5	A4	A3	AdditiveLatency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Cal. Mode Exit, maintain setting
0	0	1	Drive (1)
0	1	0	Drive (0)
1	0	0	Adjust mode a)
1	1	1	OCD Calibration default b)

A1	Output Driver Impedence Control	Driver Size
0	Normal	100%
1	Weak	60%

a) When Adjust mode is issued, AL from previously set value must be applied
b) After setting to default, OCD mode needs to be exited by setting A9~A7 to 000.
Refer to the following 2.2.2.5 section for detailed information.

*) must be programmed to 0 for compatibility with future DDR2 memory products.

A0 is used for DLL enable or disable. A1 is used for enabling half-strength data-output driver. A2 and A6 enables ODT (On-Die termination) and sets the Rtt value. A3~A5 are used for additive latency settings and A7 ~ A9 enables the OCD impedance adjustment mode. A10 enables or disables the differential $\overline{DQS}$ and RDQS signals, A11 disables or enables RDQS. Address bit A12 have to be set to "low" for normal operation. With A12 set to "high" the SDRAM outputs are disabled and in Hi-Z. "High" on BA0 and "low" for BA1 have to be set to access the EMRS(1). A13 and all "higher" address bits (including BA2) have to be set to "low" for compatibility with other DDR2 memory products with higher memory densities. Refer to the table for specific codes on the previous page.

Single-ended and Differential Data Strobe Signals

The following table lists all possible combinations for DQS, $\overline{DQS}$, RDQS, $\overline{RQDS}$ which can be programmed by A10 & A11 address bits in EMRS(1). RDQS and $\overline{RDQS}$ are available in x8 components only. If RDQS is enabled in x8 components, the DM function is disabled. RDQS is active for reads and don't care for writes :

EMRS(1)		Stobe Function Matrix				Signaling
A11 (RDQS Enable)	**$\overline{A10}$ (DQS Enable)**	**RDQS/DM**	**$\overline{RDQS}$**	**DQS**	**$\overline{DQS}$**	
0 (Disable)	0 (Enable)	DM	Hi-Z	DQS	$\overline{DQS}$	differential DQS signals
0 (Disable)	1 (Disable)	DM	Hi-Z	DQS	Hi-Z	single-ended DQS signals
1 (Enable)	0 (Enable)	RDQS	$\overline{RDQS}$	DQS	$\overline{DQS}$	differential DQS signals
1 (Enable)	1 (Disable)	RDQS	Hi-Z	DQS	Hi-Z	single-ended DQS signals

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is reset, 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Less clock cycles may result in a violation of the tAC or tDQSCK parameters.

Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data (Qoff bit in the EMRS(1) is set to 0). When the Qoff bit is set to 1, the DRAM outputs will be disabled. Disabling the DRAM outputs allows users to measure IDD currents during Read operations, without including the output buffer current.

2.2.2.3 EMRS(2) and EMRS(3) Extended Mode Registers

The Extended Mode Registers EMRS(2) and EMRS(3) are reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

2.2.2.4 Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of the sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.
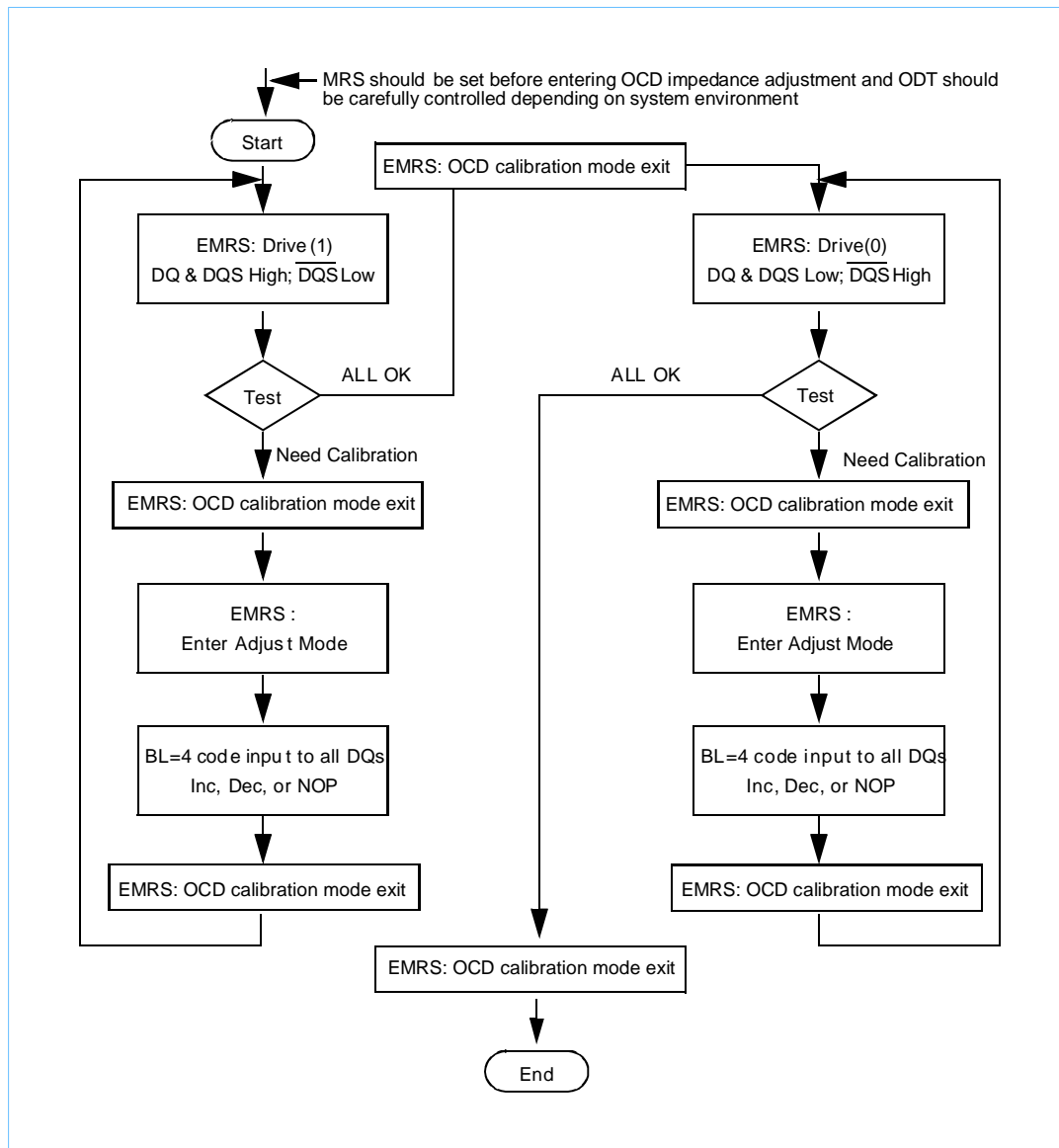
Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS(1) mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMRS(1) bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{DQS}$ (and $\overline{RDQS}$) signals are driven low. In Drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{DQS}$ (and $\overline{RDQS}$) signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in the following table. OCD applies only to normal full strength output drive setting defined by EMRS(1) and if half strength is set, OCD default driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS(1) commands not intended to adjust OCD characteristics must specify A7~A9 as '000' in order to maintain the default or calibrated value.

Off- Chip-Driver program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) high and $\overline{DQS}$, $\overline{(RDQS)}$ low
0	1	0	Drive(0) DQ, DQS, (RDQS) low and $\overline{DQS}$, $\overline{(RDQS)}$ high
1	0	0	Adjust mode
1	1	1	OCD calibration default

OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS(1) command along with a 4 bit burst code to DDR2 SDRAM as in the following table. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive the burst code to all DQs at the same time. DT0 is the table means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 8 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 8 step range. When Adjust mode command is issued, AL from previously set value must be applied.

Off- Chip-Driver Adjust Program

4 bit burst code inputs to all DQs				Operation	
D_{T0}	D_{T1}	D_{T2}	D_{T3}	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (no operation)	NOP (no operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	Reserved

For proper operation of adjust mode, WL = RL - 1 = AL + CL -1 clocks and tDS / tDH should be met as the following timing diagram. Input data pattern for adjustment, DT0 - DT3 is fixed and not affected by MRS addressing mode (i.e. sequential or interleave). Burst length of 4 have to be programmed in the MRS for OCD impedance adjustment.
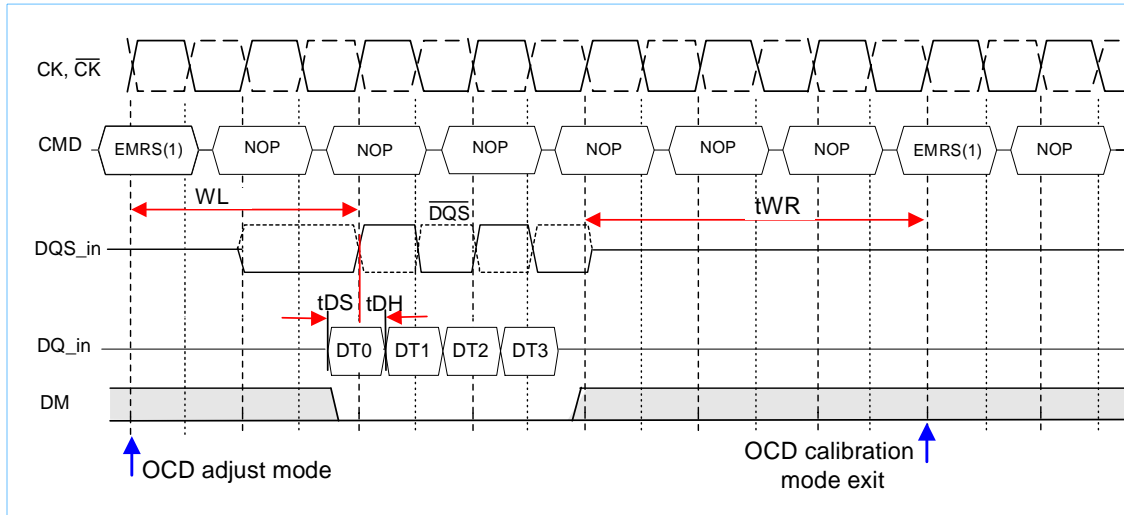
Drive Mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance before OCD impedance adjustment. In this mode, all outputs are driven out tOIT after "enter drive mode" command and all output drivers are turned-off tOIT after "OCD calibration mode exit" command as the following timing diagram.
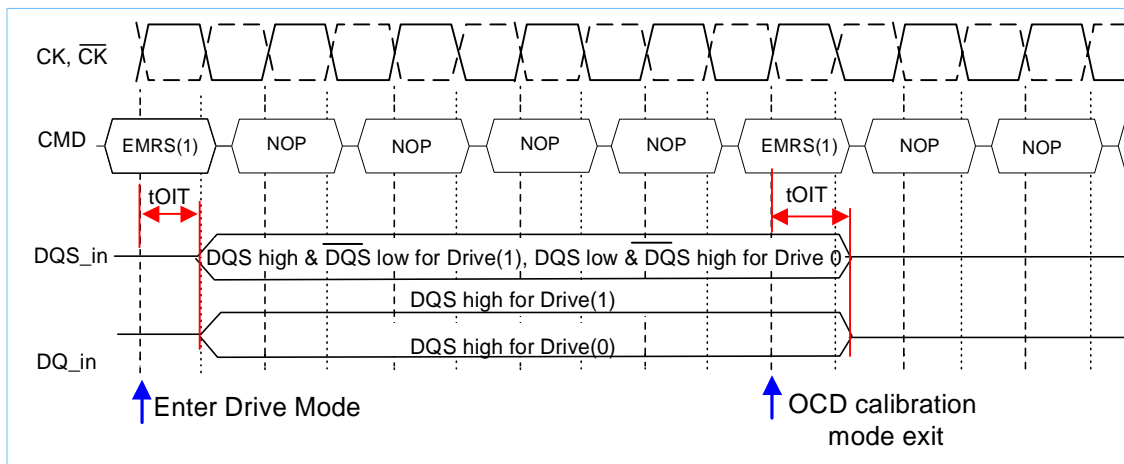
2.2.2.5 On-Die Termination (ODT)

ODT (On-Die Termination) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{DQS}$ and DM for x4 and DQ, DQS, $\overline{DQS}$, DM, RDQS (DM and RDQS share the same pin), and $\overline{RDQS}$ for x8 configuration via the ODT control pin, where $\overline{DQS}$ is terminated only when enabled in the EMRS(1) by address bit A10 = 0. For x8 configuration $\overline{RDQS}$ is only terminated, when enabled in the EMRS(1) by address bits A10 = 0 and A11 = 1.

For x16 configuration ODT is applied to each UDQ, LDQ, UDQS, $\overline{UDQS}$, LDQS, $\overline{LDQS}$, UDM and LDM signal via the ODT control pin, where $\overline{UDQS}$ and $\overline{LDQS}$ are terminated only when enabled in the EMRS(1) by address bit A10 = 0.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self-Refresh mode.

Funtional Prepresentation of ODT
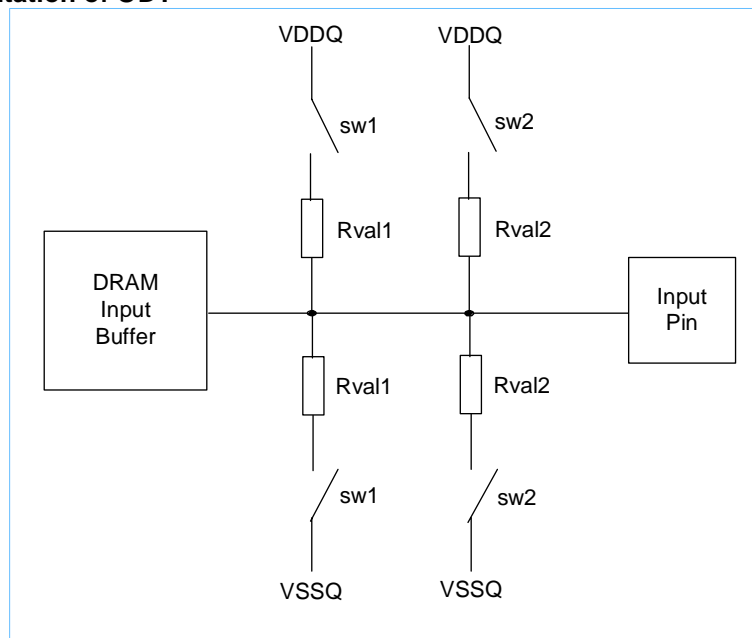
Switch sw1 or sw2 is enabled by the ODT pin. Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS(1) address bits A6 & A2. Target *Rtt = 0.5 * Rval1* or *0.5 * Rval2*.

The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT.

ODT Truth Tables

The ODT Truth Table shows which of the input pins are terminated depending on the state of address bit A10 and A11 in the EMRS(1) for all three device organisations (x4, x8 and x16). To activate termination of any of these pins, the ODT function has to be enabled in the EMRS(1) by address bits A6 and A2.

Input Pin	EMRS(1) Adress Bit A10	EMRS(1) Adress Bit A11
x4 components:		
DQ0~DQ3	X	X
DQS	X	X
$\overline{DQS}$	0	X
DM	X	X
x8 components:		
DQ0~DQ7	X	X
DQS	X	X
$\overline{DQS}$	0	X
RDQS	X	1
$\overline{RDQS}$	0	1
DM	X	0
x16 components:		
LDQ0~LDQ7	X	X
UDQ0~UDQ7	X	X
LDQS	X	X
$\overline{LDQS}$	0	X
UDQS	X	X
$\overline{UDQS}$	0	X
LDM	X	X
UDM	X	X

ODT Timing for Active / Standby (Idle) Mode and Standard Active Power-Down Mode

1) Both ODT to Power Down Entry and Exit Latency timing parameter tANPD and tAXPD are met, therefore Non-Power Down Mode timings have to be applied.

2) ODT turn-on time ($t_{AON,min}$) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max. ($t_{AON,max}$) is when the ODT resistance is fully on. Both are measured from t_{AOND}.

3) ODT turn off time min. ($t_{AOF,min}$) is when the device starts to turn off the ODT resistance. ODT turn off time max. ($t_{AOF,max}$) is when the bus is in high impedance. Both are measured from t_{AOFD}.

ODT Timing for Precharge Power-Down and Low Power Power-Down Mode

1) Both ODT to Power Down Entry and Exit Latencies tANPD and tAXPD are not met, therefore Power-Down Mode timings have to be applied.
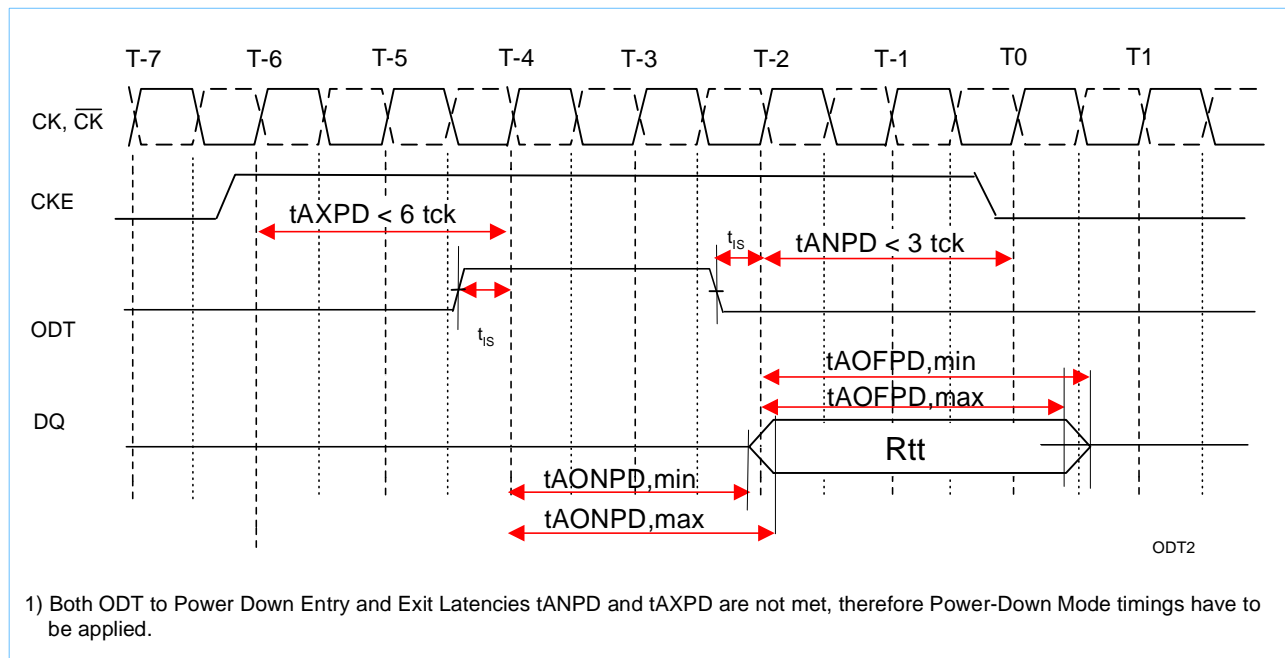
2.3 Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 ~ BA2 are used to select the desired bank. The row addresses A0 through A13 are used to determine which row to activate in the selected bank for x4 and x8 organised components. For x16 components row addresses A0 through A12 have to be applied. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined (tRC). The minimum time interval between Bank Active commands, to any other bank, is the Bank A to Bank B delay time (tRRD).

In order to ensure that components with 8 internal memory banks do not exceed the instantaneous current supplying capability, certain restrictions on operation of the 8 banks must be observed. There are two rules. One for restricting the number of sequential Active commands that can be issued and another for allowing more time for $\overline{RAS}$ precharge for a Precharge-All command. The rules are as follows:

1) *Sequential Bank Activation Restriction:* No more than 4 banks may be actived in a rolling 4 * tRRD + 2 * tCK windows. tRRD must be converted to clocks prior to multiplying by 4 and prior to adding 2 * tCK. Converting to clocks is done by dividing tRRD (ns) by tCK(ns) and rounding up to the next integer value.

2) *Precharge All Allowance:* tRP for a Precharge-All command will equal to tRP + 1 tCK, where tRP is the value for a single bank precharge

Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2
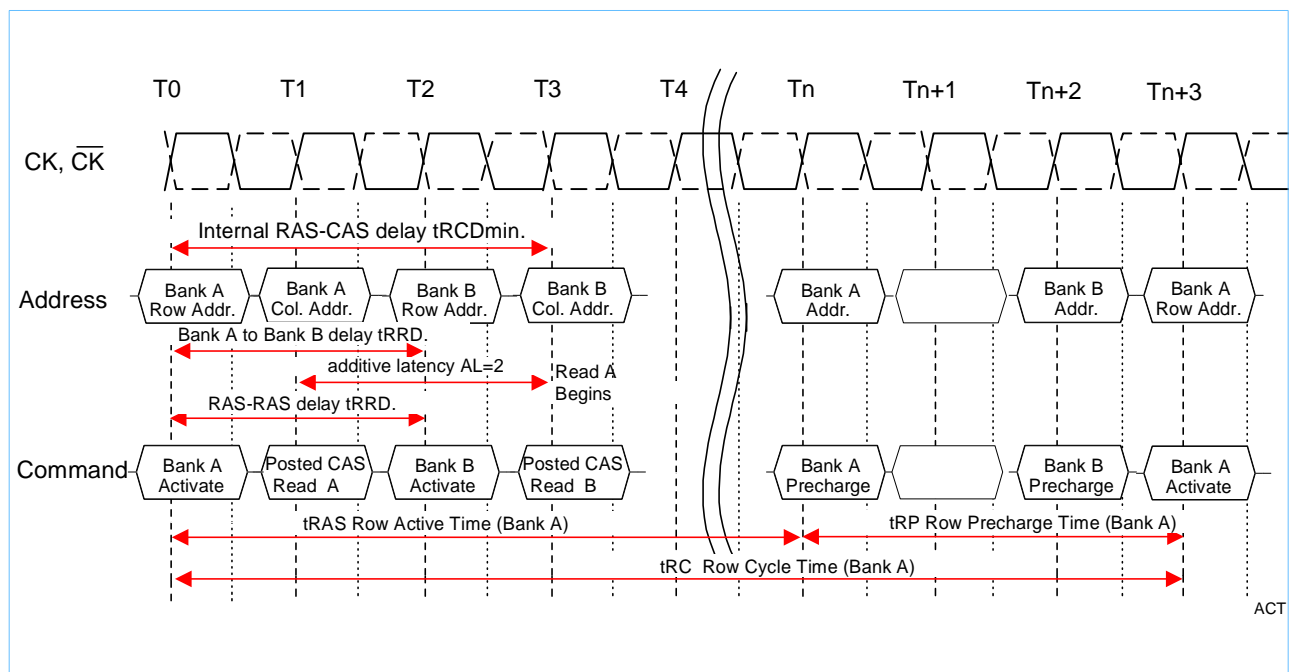
2.4 Read and Write Commands and Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low). The DDR2 SDRAM provides a wide variety of fast access modes. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles at data rates of up to 667Mb/sec/pin for main memory. The boundary of the burst cycle is restricted to specific segments of the page length.

For example, the 32Mbit x 4 I/O x 4 Bank chip has a page length of 1 kByte (defined by CA0-CA9 & CA11). In case of a 4-bit burst operation (burst length = 4) the page length of 1 kByte is divided into 512 uniquely addressable segments (4-bits x 4 I/O each). The 4-bit burst operation will occur entirely within one of the 512 segments (defined by CA0-CA8) beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9 & A11). The second, third and fourth access will also occur within this segment, however, the burst order is a function of the starting address, and the burst sequence.

In case of a 8-bit burst operation (burst length = 8) the page length of 1 kByte is divided into 256 uniquely addressable double segments (8-bits x 4 I/O each). The 8-bit burst operation will occur entirely within one of the 256 double segments (defined by CA0-CA7) beginning with the column address supplied to the deivce during the Read or Write Command (CA0-CA9 & CA11).

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. Therefore the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (tCCD) is a minimum of 2 clocks for read or write cycles.

For 8 bit burst operation (BL = 8) the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (tCCD) is 4 clocks for read or write cycles. Burst interruption is allowed with 8 bit burst operation. For details see the "Burst Interrupt" - Section of this datasheet.

Example:

Read Burst Timing Example : (CL = 3, AL = 0, RL = 3, BL = 4)
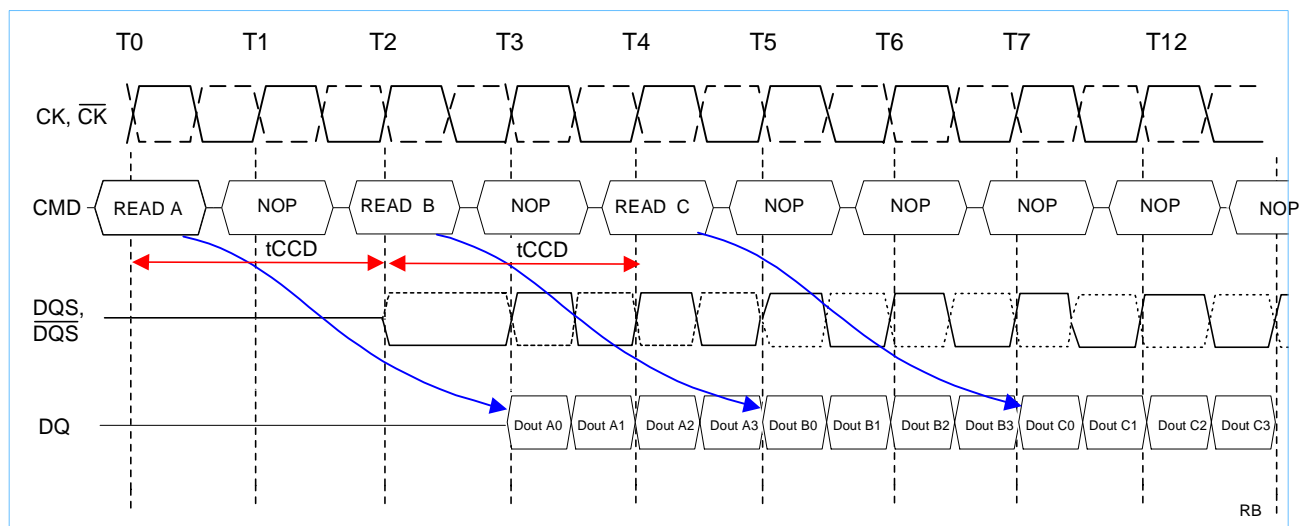
2.4.1 Posted $\overline{\text{CAS}}$

Posted $\overline{\text{CAS}}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the $\overline{\text{RAS}}$ bank activate command (or any time during the $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is the sum of AL and the $\overline{\text{CAS}}$ latency (CL). Therefore if a user chooses to issue a Read/Write command before the tRCDmin, then AL greater than 0 must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus $\overline{\text{CAS}}$ latency (RL=AL+CL). If a user chooses to issue a Read command after the tRCDmin period, the Read Latency is also defined as RL = AL + CL.

Examples:

Read followed by a write to the same bank, Activate to Read delay < tRCDmin:
AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 4
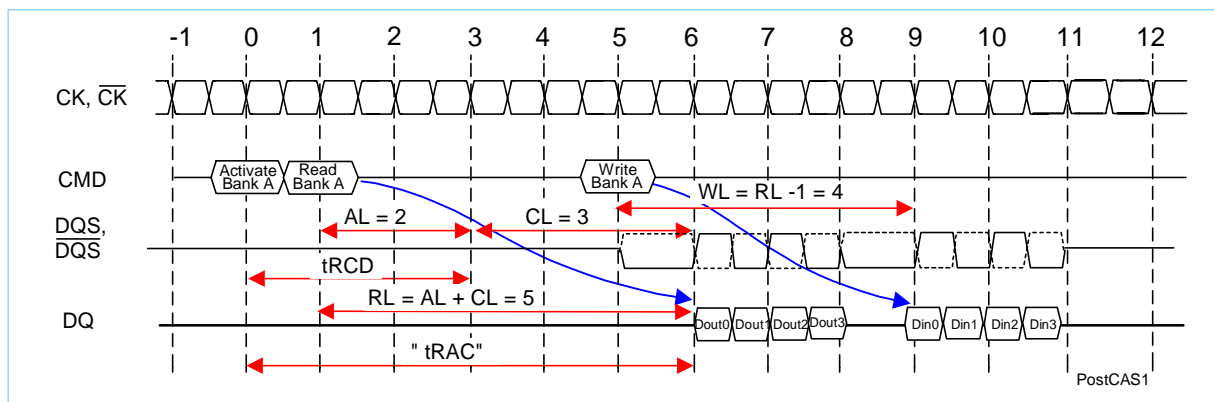
Read followed by a write to the same bank, Activate to Read delay < tRCDmin:
AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 8
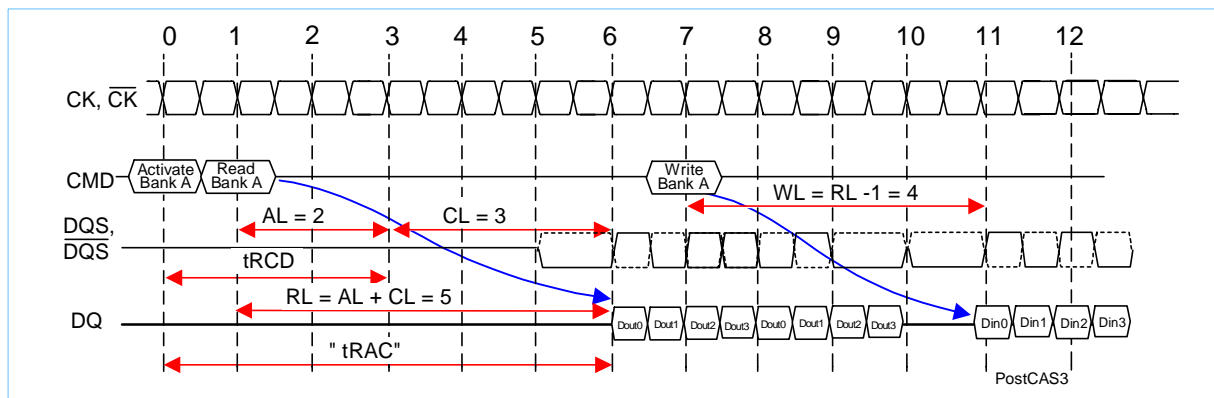
Read followed by a write to the same bank, Activate to Read delay = tRCDmin:
AL = 0, CL = 3, RL = (AL + CL) = 3, WL = (RL -1) = 2, BL = 4
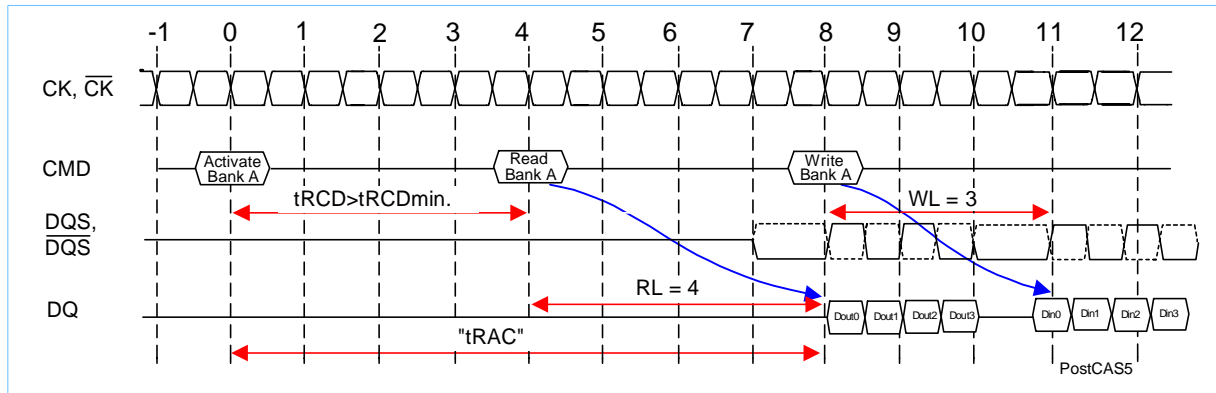
Read followed by a write to the same bank, Activate to Read delay > tRCDmin:
AL = 1, CL = 3, RL = 4, WL = 3, BL = 4
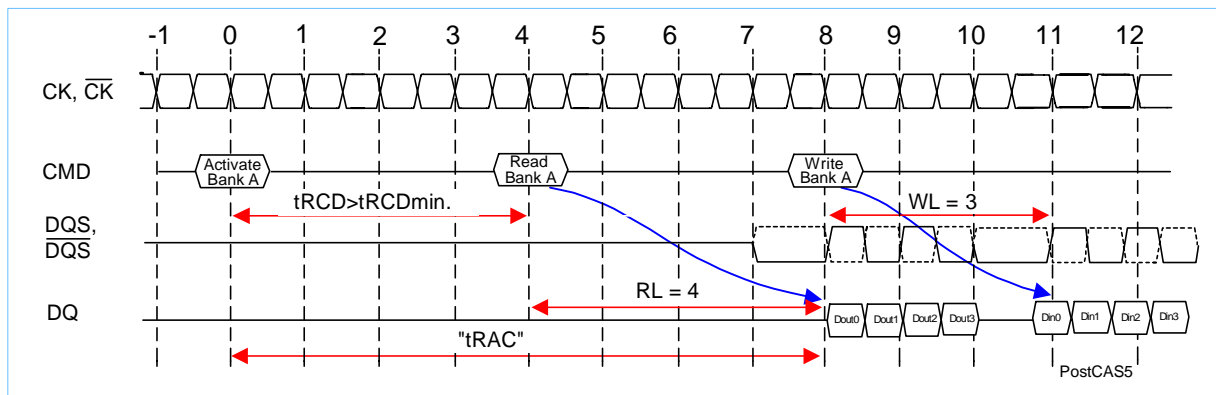
2.4.2 Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by the addresses A0 ~ A2 of the MRS. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS. Seamless burst read or write operations are supported. Interruption of a burst read or write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a read or write burst when burst length = 8 is used, see the "Burst Interruption " section of this datasheet. A Burst Stop command is not supported on DDR2 SDRAM devices.

Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Note: 1) Page length is a function of I/O organization
      128Mb X 4 organization (CA0-CA9, CA11); Page Length = 1 kByte
      64Mb X 8 organization (CA0-CA9); Page Length = 1 kByte
      32Mb X 16 organization (CA0-CA9); Page Length = 2 kByte
   2) Order of burst access for sequential addressing is "nibble-based" and therefore different from SDR
     or DDR components

2.4.3 Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command until the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register Set (EMRS(1)).

Basic Burst Read Timing
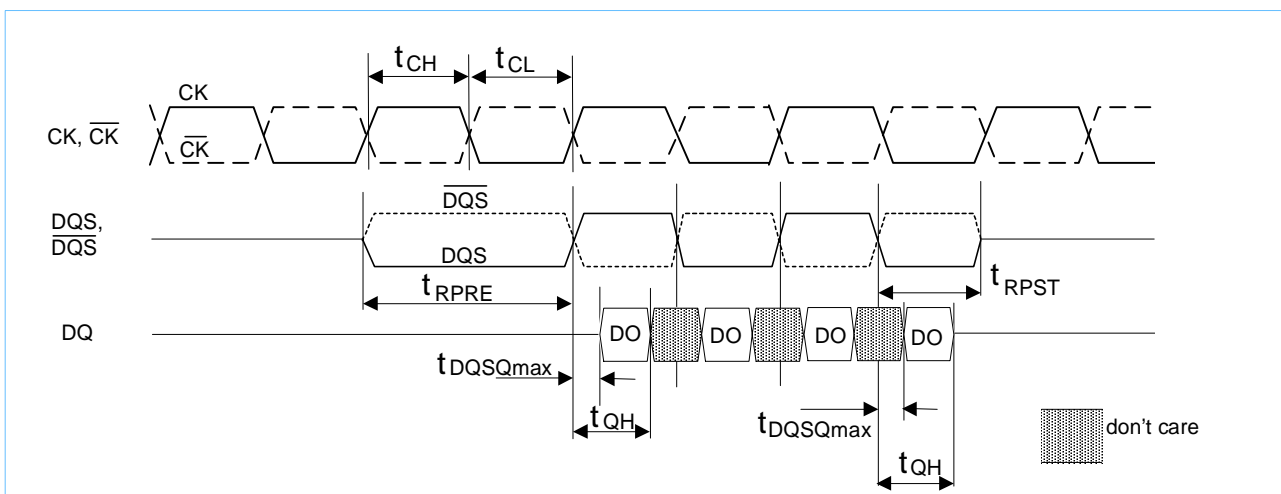
Examples:

Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)
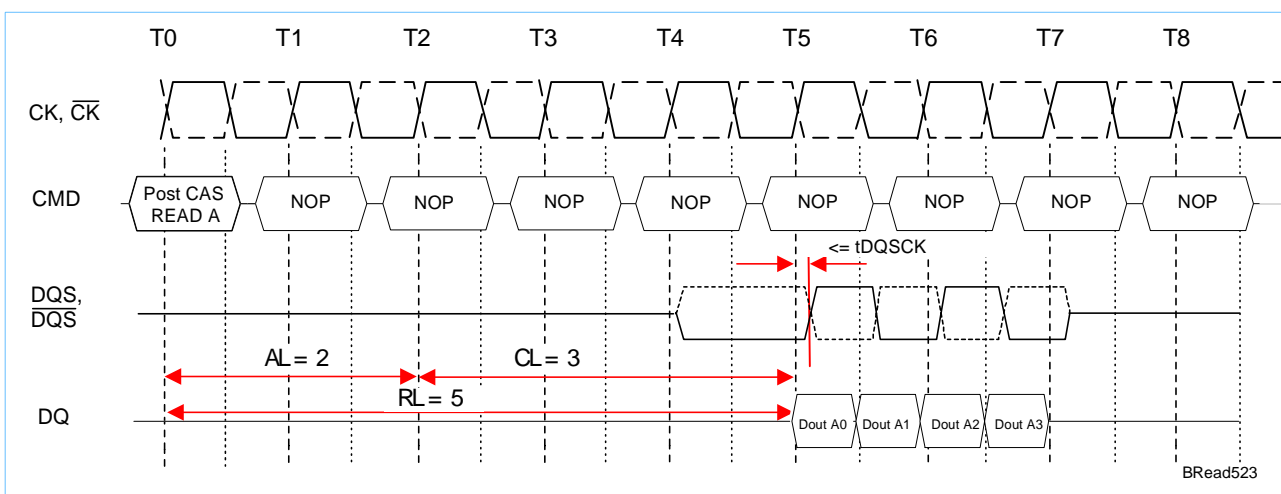
Burst Read Operation: RL = 3 (AL = 0, CL = 3, BL = 8)

BRead303
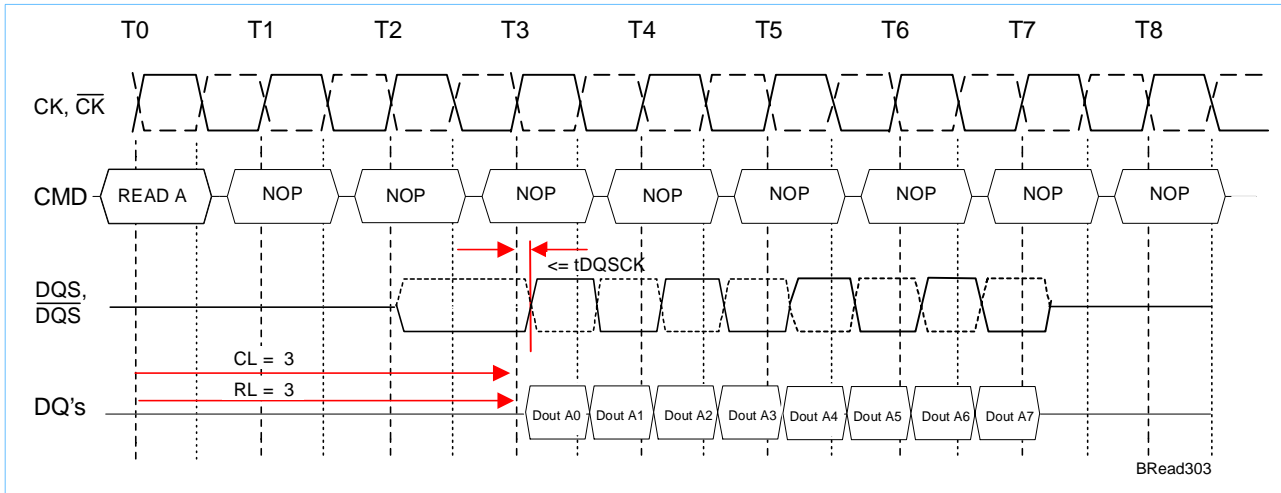
Burst Read followed by Burst Write : RL = 5, WL = (RL-1) = 4, BL = 4

BRBW514
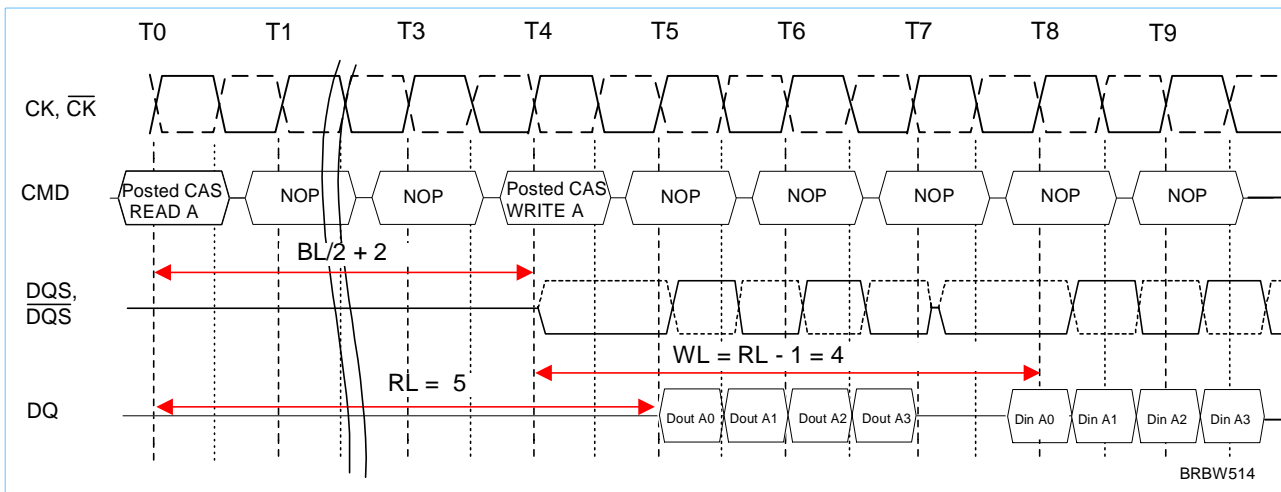
The minimum time from the burst read command to the burst write command is defined by a read-to-write turn-around time, which is BL/2 + 2 clocks.
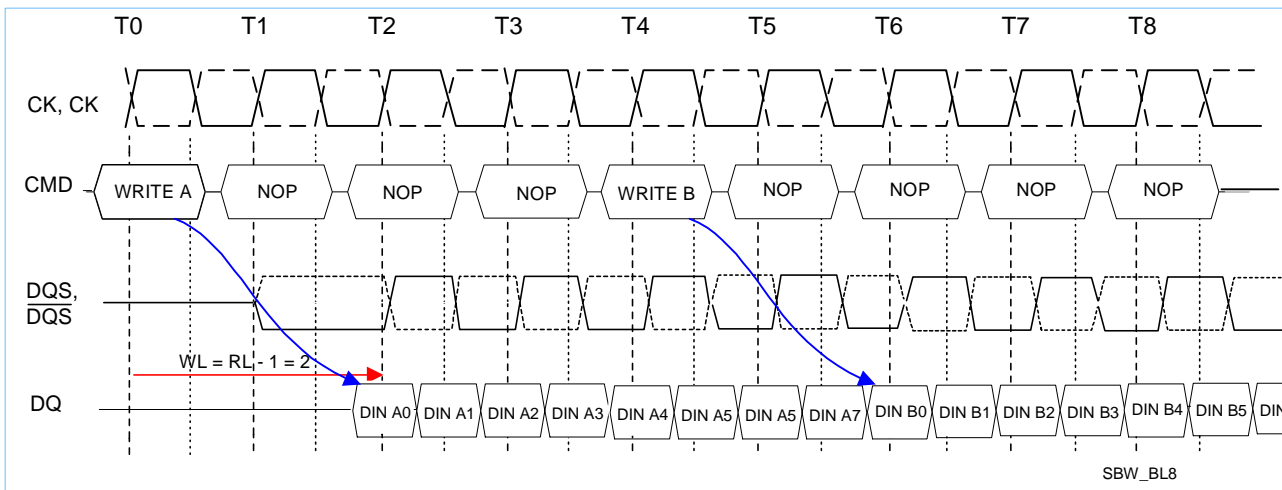
Seamless Burst Read Operation : RL = 5, AL = 2, CL = 3, BL = 4
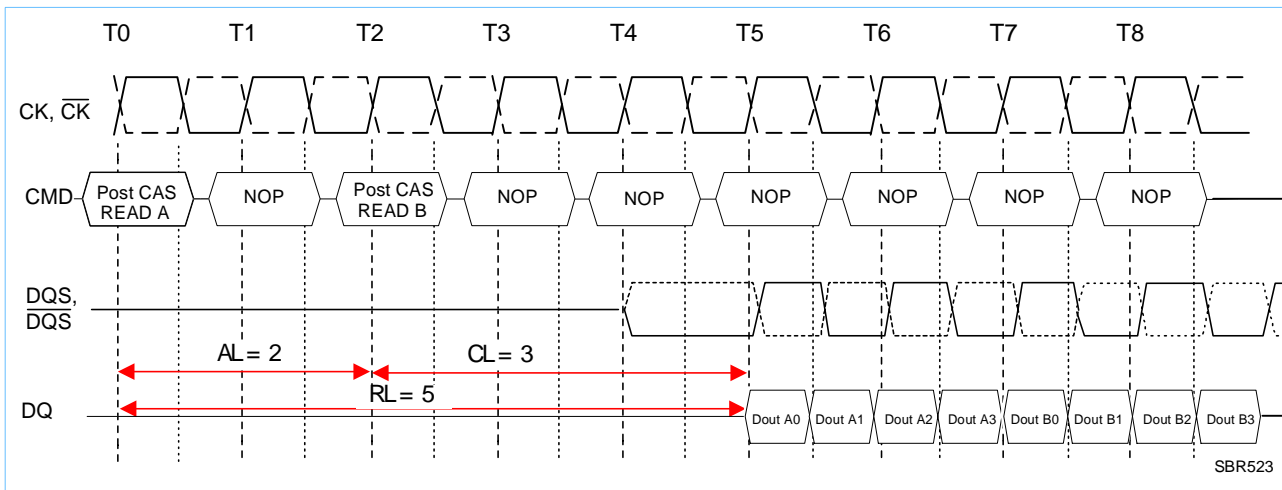
The seamless burst read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

Seamless Burst Read Operation : RL = 3, AL = 0, CL = 3, BL = 8 (non interrupting)
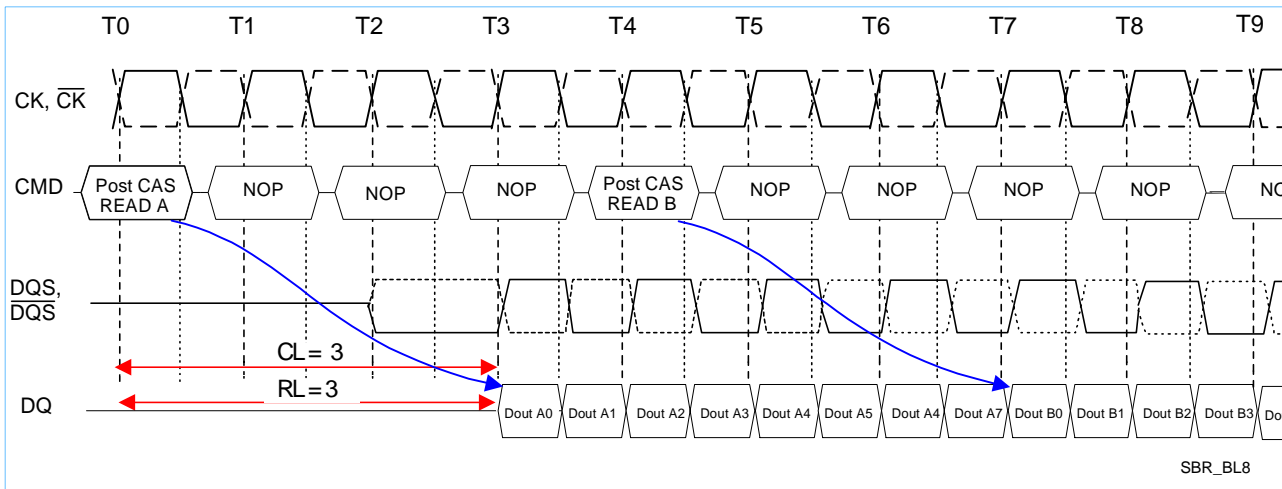
The seamless, non interrupting 8-bit burst read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

2.4.4 Burst Write Command

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is named "write recovery time" (tWR) and is the time needed to store the write data into the memory array. tWR is an analog timing parameter (see the AC table in this specification) and is not the programmed value for WR in the MRS.

Basic Burst Write Timing
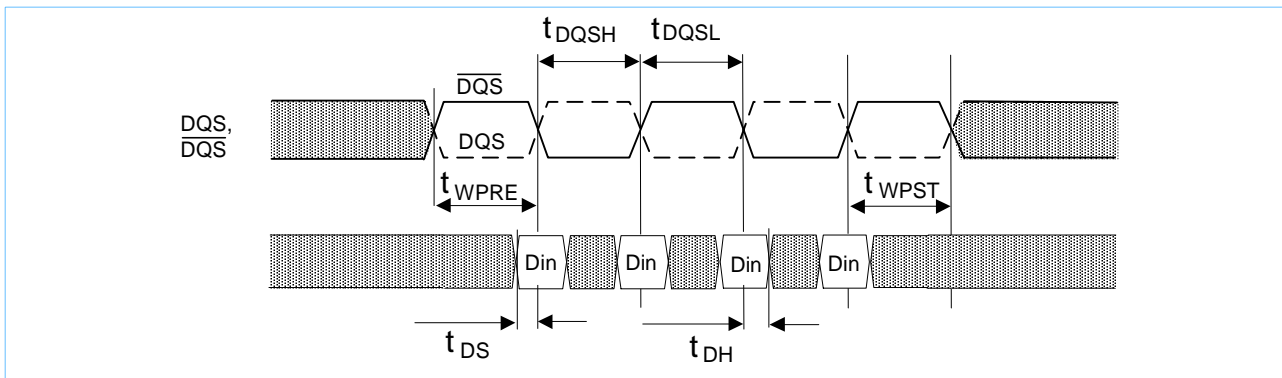
Example:.

Burst Write Operation : RL = 5 (AL = 2, CL = 3), WL = 4, BL = 4
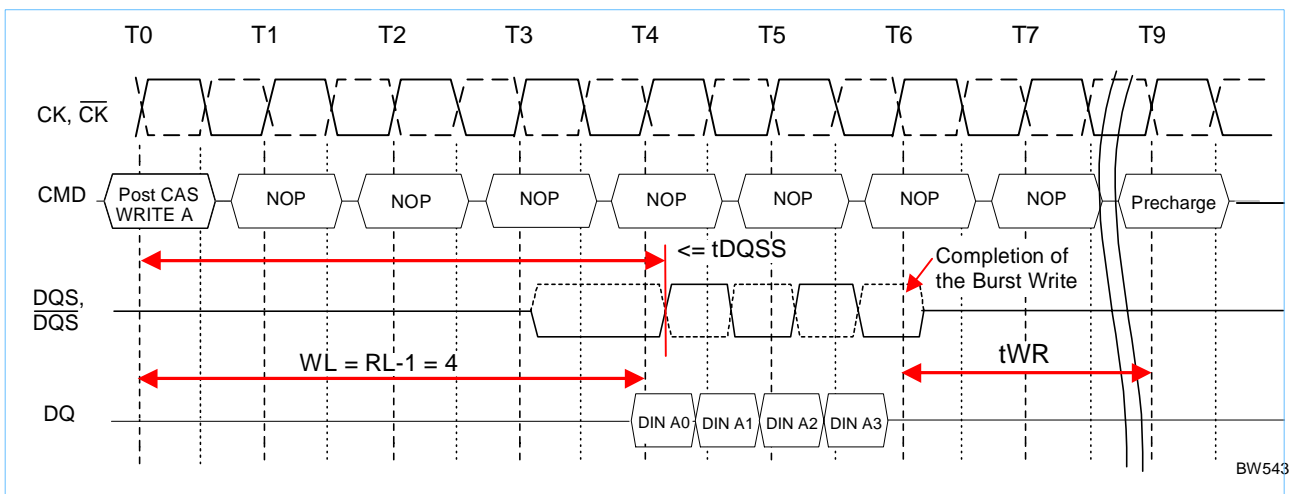
Burst Write Operation : RL = 3 (AL = 0, CL = 3), WL = 2, BL = 4
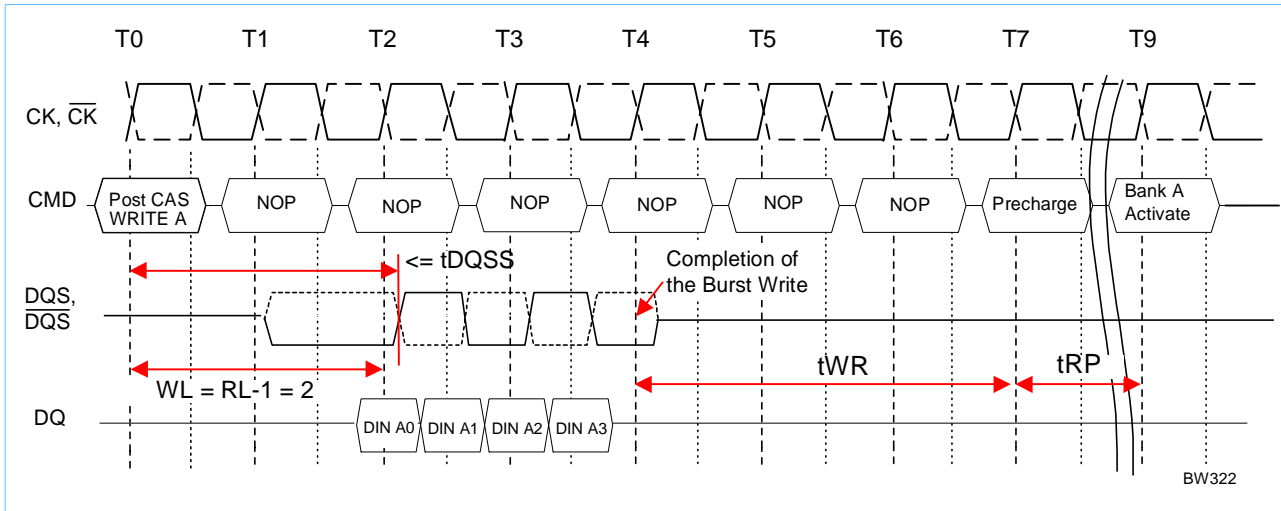
Burst Write followed by Burst Read : RL = 5 (AL = 2, CL = 3), WL = 4, tWTR = 2, BL = 4
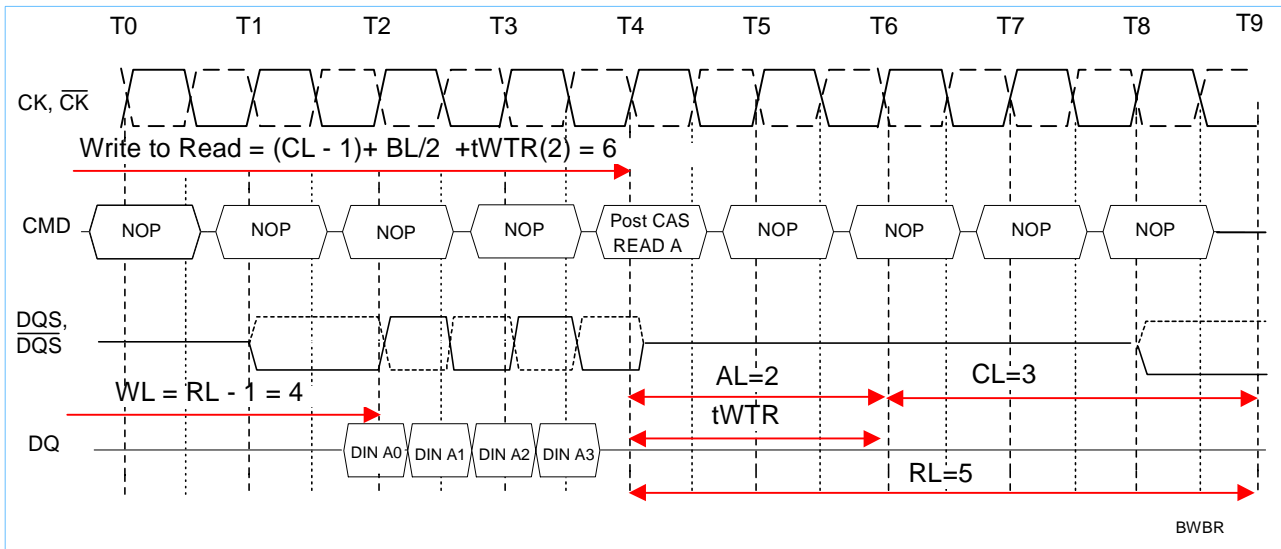
The minimum number of clocks from the burst write command to the burst read command is

$$(CL - 1) + BL/2 + tWTR$$

where tWTR is the write-to-read turn-around time tWTR expressed in clock cycles. The tWTR is not a write recovery time (tWR) but the time required to transfer 4 bit write data from the input buffer into sense amplifiers in the array.

Seamless Burst Write Operation : RL = 5, WL = 4, BL = 4
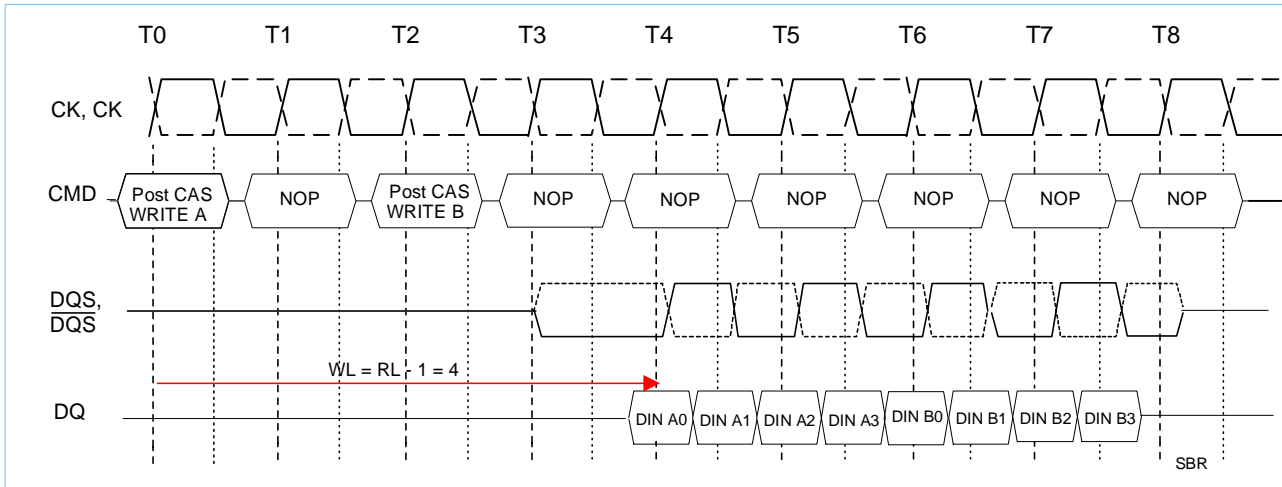
The seamless burst write operation is supported by enabling a write command every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

Seamless Burst Write Operation : RL = 3, WL = 2, BL = 8, non interrupting

The seamless, non interrupting 8-bit burst write operation is supported by enabling a write command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

2.4.5 Write Data Mask

One write data mask input (DM) for x4 and x8 components and two write data mask inputs (LDM, UDM) for x16 components are supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. Data mask is not used during read cycles. If DM is high during a write burst coincident with the write data, the write data bit is not written to the memory. For x8 components the DM function is disabled, when RDQS / $\overline{\text{RDQS}}$ are enabled by EMRS(1).

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Write Data Mask Timing

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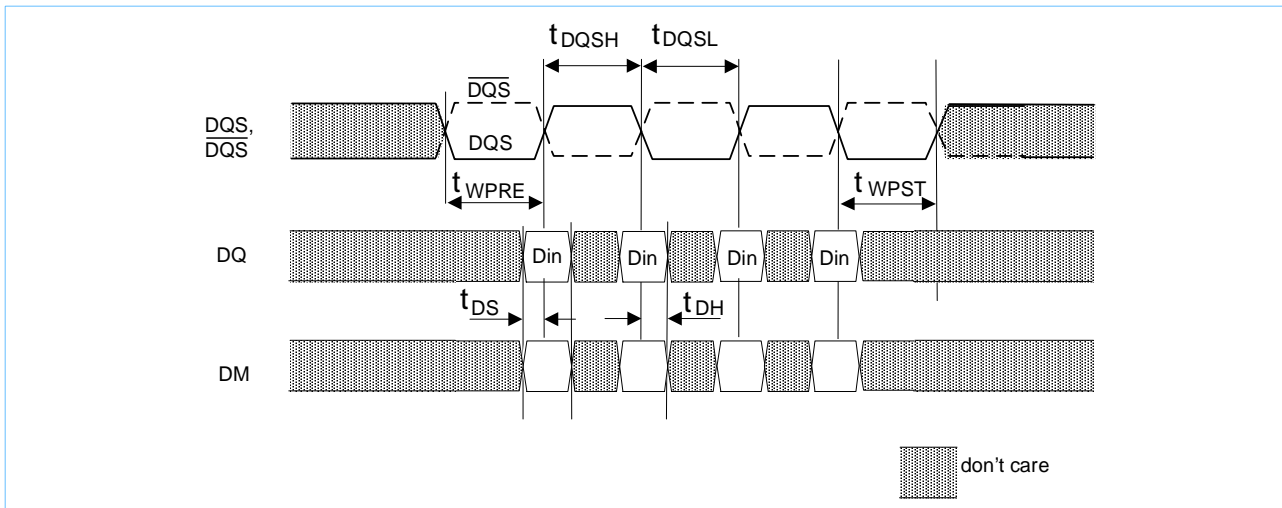
Burst Write Operation with Data Mask : RL = 3 (AL = 0, CL = 3), WL = 2, tWR = 3 , BL = 4
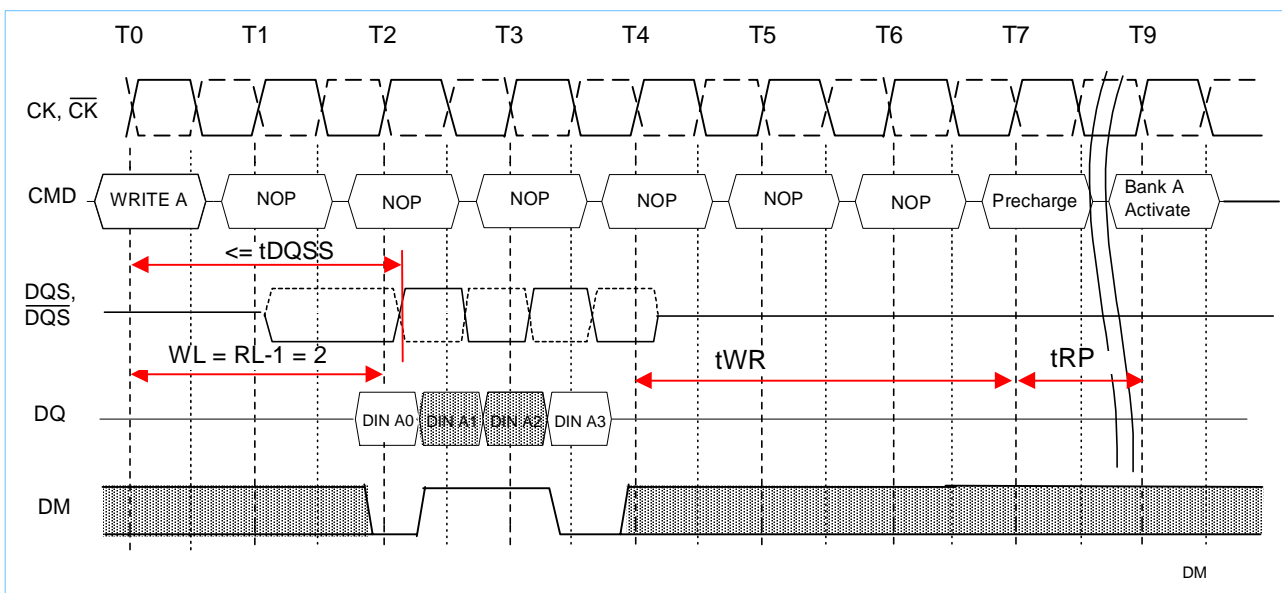
2.4.6 Burst Interruption

Interruption of a read or write burst is prohibited for burst length of 4 and only allowed for burst length of 8 under the following conditions:

1. A Read Burst of 8 can only be interrupted by another Read command. Read burst interruption by a Write or Precharge Command is prohibited.

2. A Write Burst of 8 can only be interrupted by another Write command. Write burst interruption by a Read or Precharge Command is prohibited.

3. Read burst interrupt must occur exactly two clocks after the previous Read command. Any other Read burst interrupt timings are prohibited.

4. Write burst interrupt must occur exactly two clocks after the previous Write command. Any other Read burst interrupt timings are prohibited.

5. Read or Write burst interruption is allowed to any bank inside the DDR2 SDRAM.

6. Read or Write burst with Auto-Precharge enabled is not allowed to be interrupted.

7. Read burst interruption is allowed by a Read with Auto-Precharge command.

8. Write burst interruption is allowed by a Write with Auto-Precharge command.

9. All command timings are referenced to burst length set in the mode register. They are not referenced to the actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt). Minimum Write to Precharge timing is WL + BL/ 2 + tWR, where tWR starts with the rising clock after the un-interrupted burst end and not form the end of the actual burst end.

Examples:

Read Burst Interrupt Timing Example : (CL = 3, AL = 0, RL = 3, BL = 8)
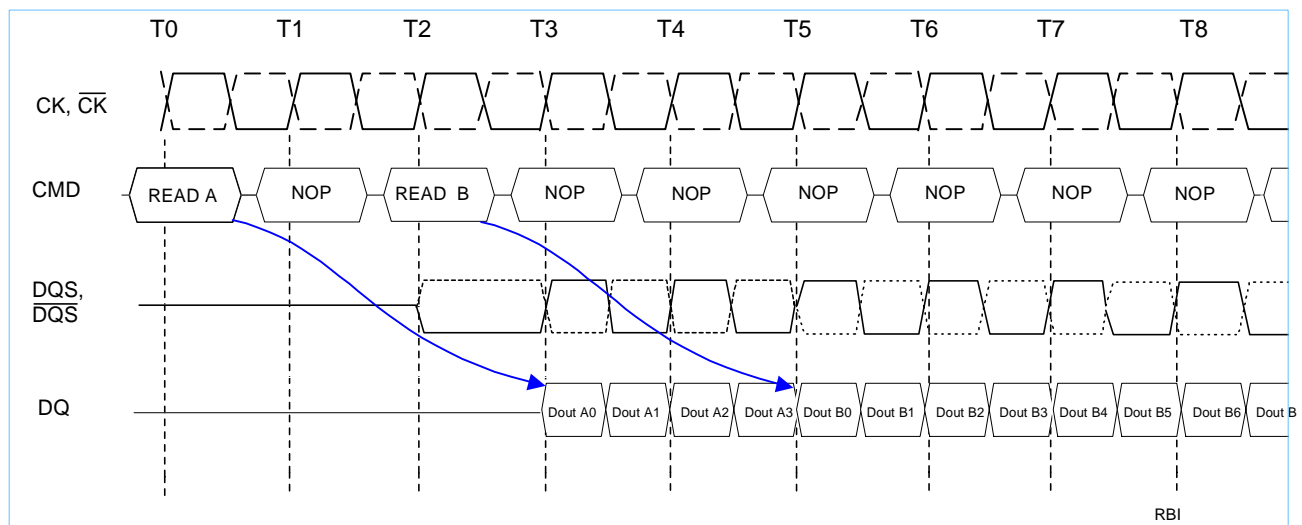
Write Burst Interrupt Timing Example : (CL = 3, AL = 0, WL = 2, BL = 8)
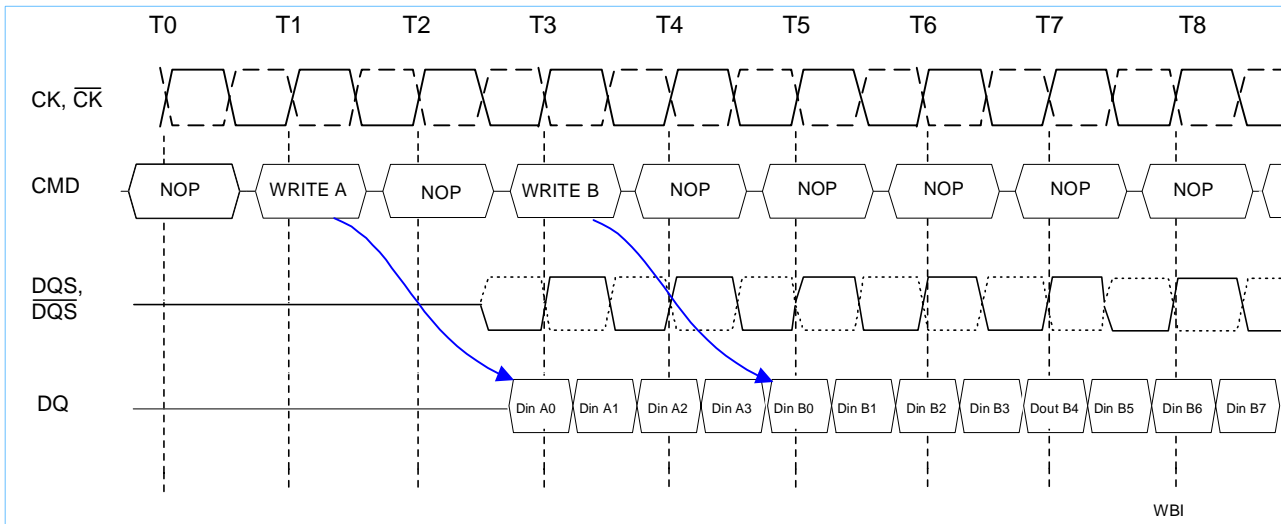
2.5 Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 ~ BA2 are used to define which bank to precharge when the command is issued.

Bank Selection for Precharge by Address Bits

A10	BA0	BA1	BA2	Precharge Bank(s)
LOW	LOW	LOW	LOW	Bank 0 only
LOW	LOW	HIGH	LOW	Bank 1 only
LOW	HIGH	LOW	LOW	Bank 2 only
LOW	HIGH	HIGH	LOW	Bank 3 only
LOW	LOW	LOW	HIGH	Bank 4 only
LOW	LOW	HIGH	HIGH	Bank 5 only
LOW	HIGH	LOW	HIGH	Bank 6 only
LOW	HIGH	HIGH	HIGH	Bank 7 only
HIGH	Don't Care	Don't Care	Don't Care	all banks

Burst Read Operation Followed by a Precharge

The following rules apply as long as the tRTP timing parameter - Internal Read to Precharge Command delay time - is less or equal two clocks, which is the case for operating frequencies less or equal 266 Mhz (DDR2 400 and 533 speed sorts):

Minimum Read to Precharge command spacing to the same bank = AL + BL/2 clocks. For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive Latency (AL) + BL/2 clocks" after a Read Command, as long as the minimum tRAS timing is satisfied.

A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

(1) The RAS precharge time (tRP) has been satisfied from the clock at which the precharge begins.

(2) The RAS cycle time (tRCmin) from the previous bank activation has been satisfied.

For operating frequencies higher than 266 MHz, tRTP becomes > 2 clocks and one additional clock cycle has to be added for the minimum Read to Precharge command spacing, which now becomes AL + BL/2 + 1 clocks.
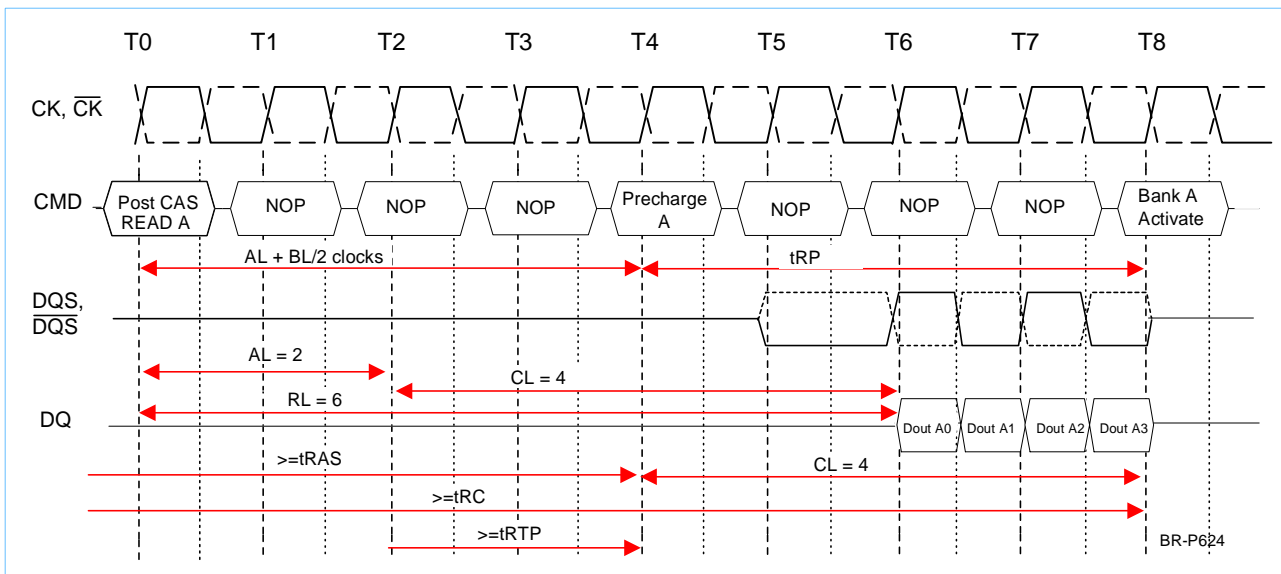
Examples:

Burst Read Operation Followed by Precharge: RL = 4 (AL = 1, CL = 3), BL = 4, tRTP <= 2 clocks
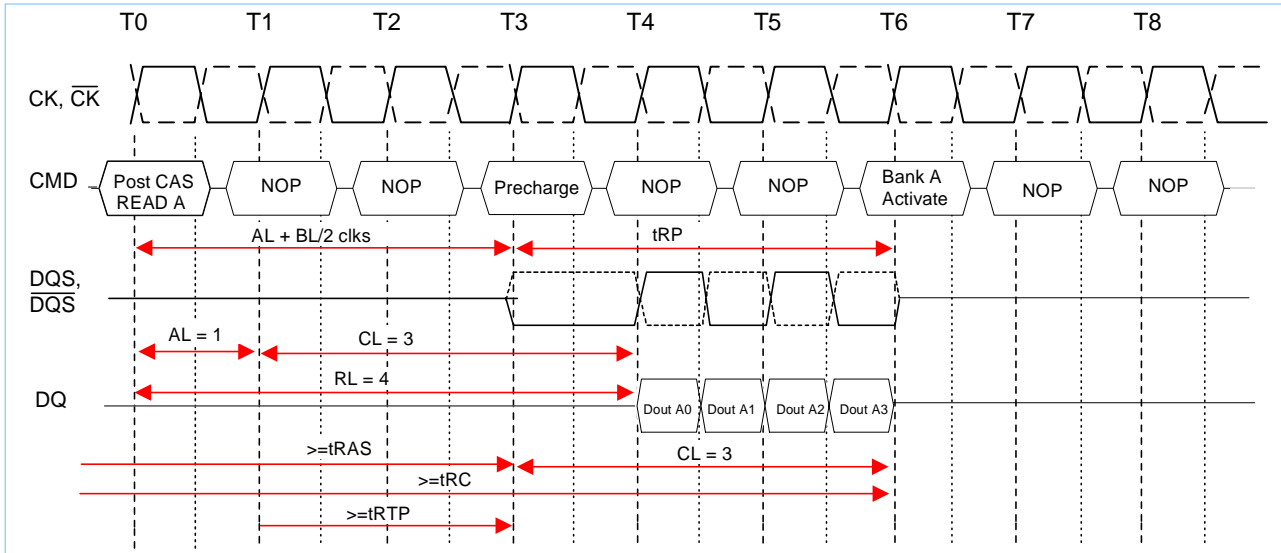
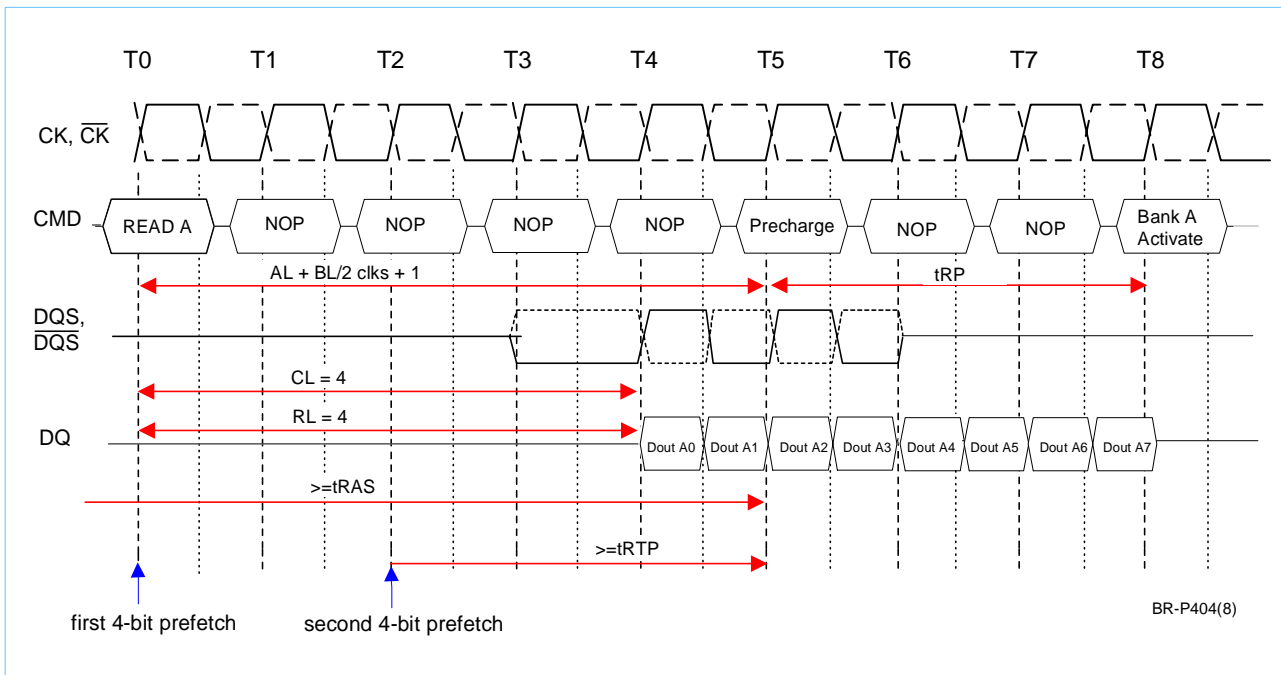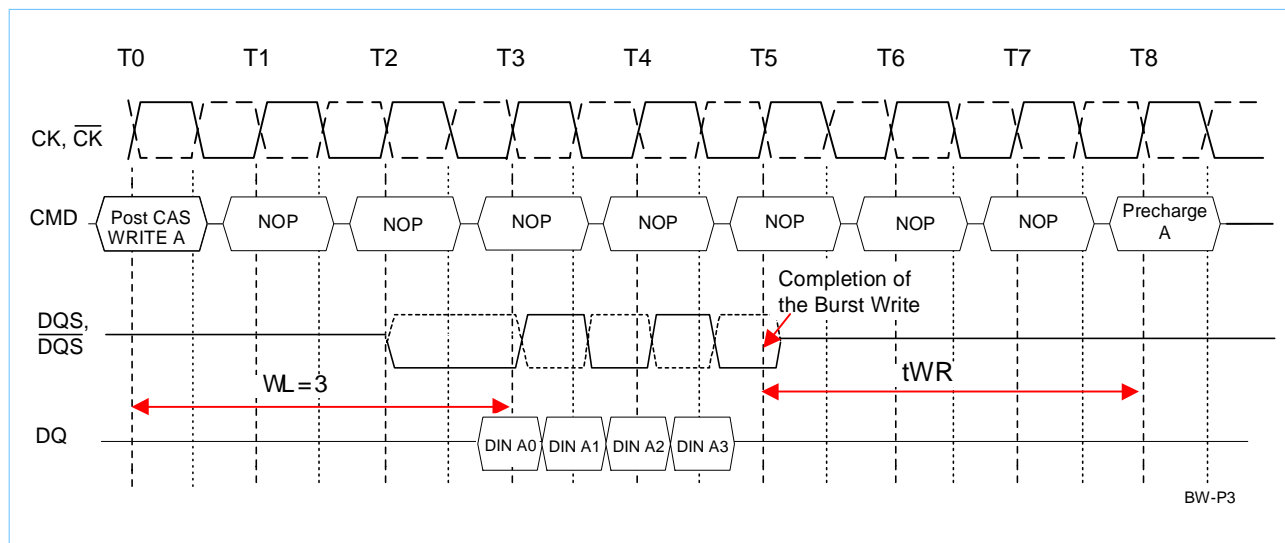**Burst Read Operation Followed by Precharge: RL = 4 (AL = 1, CL = 3), BL = 8, tRTP <= 2 clocks**

BR-P413(8)
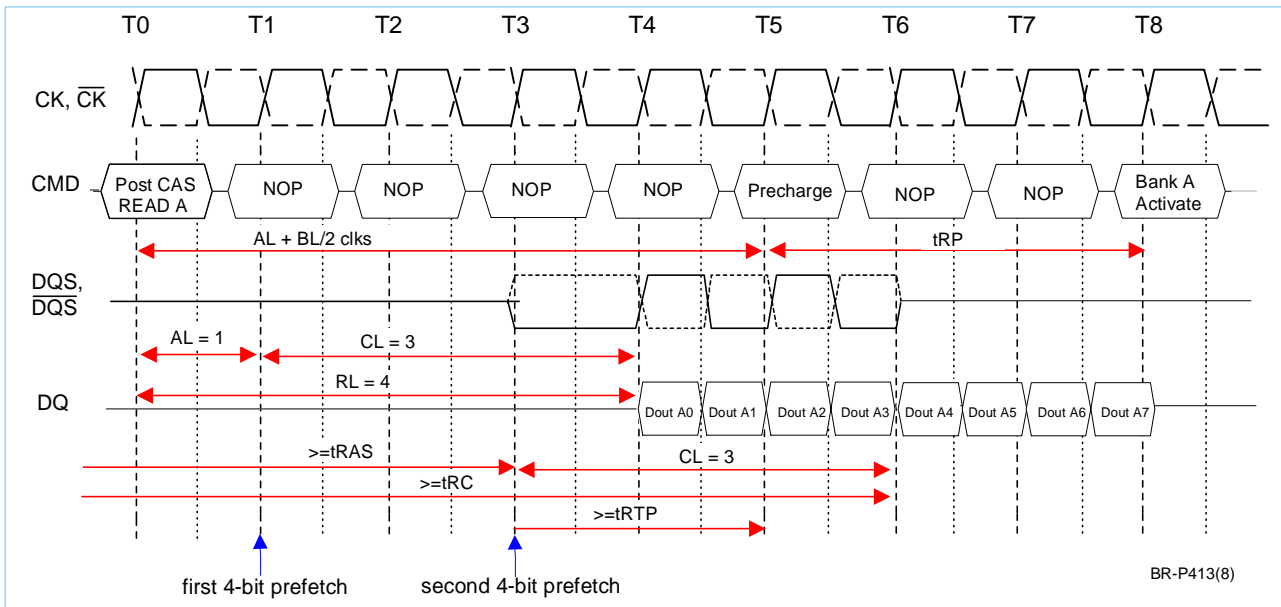
Burst Read Operation Followed by Precharge: RL = 5 (AL = 2, CL = 3), BL = 4, tRTP <= 2 clocks
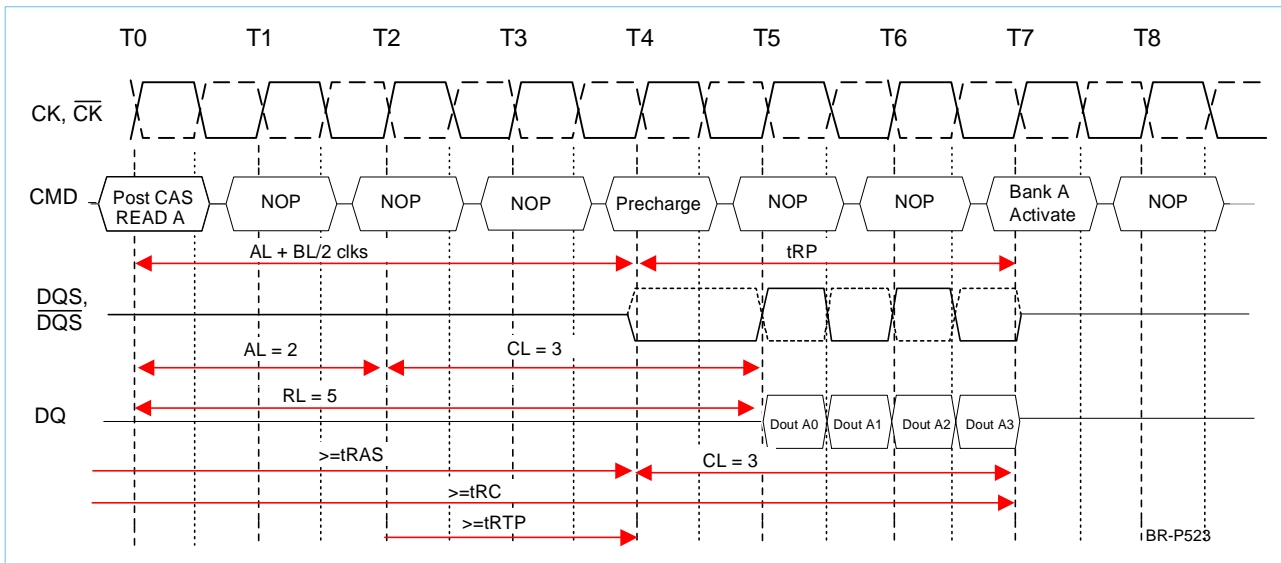
Burst Read Operation Followed by Precharge: RL = 6, (AL = 2, CL = 4), BL = 4, tRTP <= 2 clocks

Burst Read Operation Followed by Precharge: RL = 4, (AL = 0, CL = 4), BL = 8, tRTP > 2 clocks

BR-P404(8)

Burst Write followed by Precharge

Minimum Write to Precharge command spacing to the same bank = **WL + BL/2 + tWR**. For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (t WR) referenced from the completion of the burst write to the Precharge command. No Precharge command should be issued prior to the tWR delay, as DDR2 SDRAM does not support any burst interrupt by a Precharge command. tWR is an analog timing parameter (see the AC table in this datasheet) and is not the programmed value for tWR in the MRS.

Examples:.

Burst Write followed by Precharge : WL = (RL - 1) = 3, BL = 4, tWR = 3

Burst Write followed by Precharge : WL = (RL - 1) = 4, BL = 4, tWR = 3
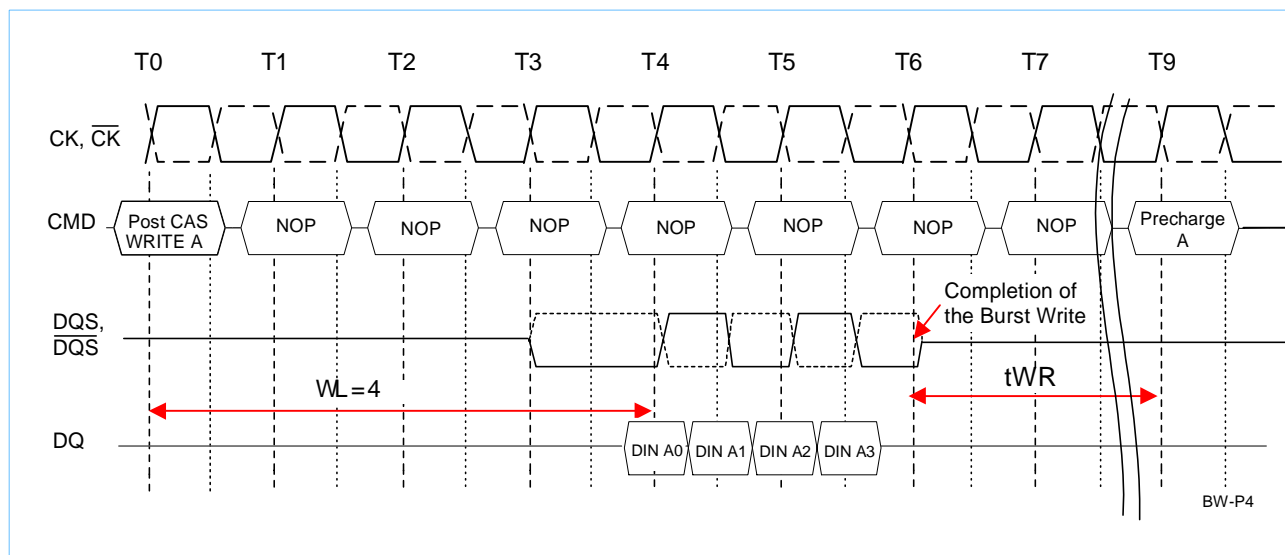
2.6 Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Pre-charge Command or the Auto-Precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to auto-matically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Com-mand is issued, then the Auto-Precharge function is enabled. During Auto-Precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge internally on the rising edge which is CAS Latency (CL) clock cycles before the end of the read burst. Auto-Precharge is also implemented for Write Commands.The precharge operation engaged by the Auto_precharge command will not begin until the last datga of the write burst sequence is properly stored in the memory array. This feature allows the pre-charge operation to be partially or completely hidden during burst read cycles (dependent upon CAS Latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the Auto-Precharge com-mand may be issied with any read or write command.

Burst Read with Auto-Precharge

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if tRAS(min) and tRTP are satisfied. If tRAS(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until tRAS(min) is satisfied. If tRTP(min) is not satis-fied at the edge, the start point of Auto-precharge operation will be delayed until tRTP(min) is satisfied.
In case the internal precharge is pushed out by tRTP, tRP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Auto-Precharge to the next Activate command becomes AL + tRTP + tRP. For BL = 8 the time from Read with Auto-Precharge to the next Activate command is AL + 2 + tRTP + tRP. Note that both parameters tRTP and tRP have to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously:

(1) The $\overline{RAS}$ precharge time (tRP) has been satisfied from the clock at which the Auto-Precharge begins.

(2) The $\overline{RAS}$ cycle time (tRC) from the previous bank activation has been satisfied.
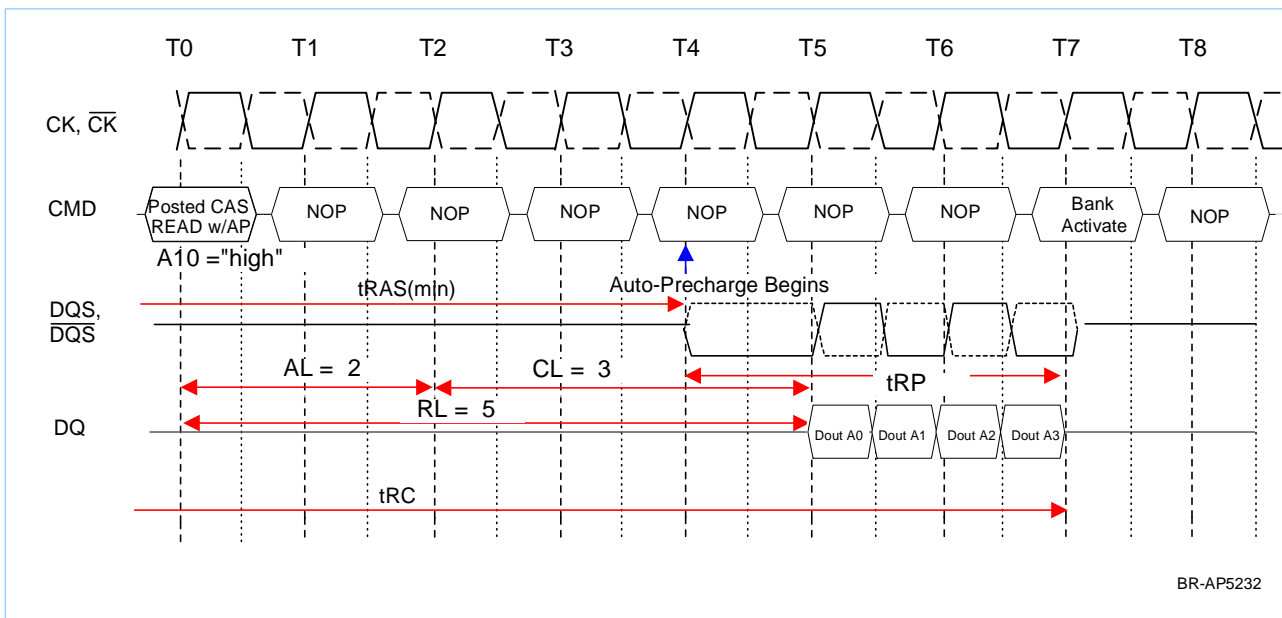
Examples:

Burst Read with Auto-Precharge followed by an activation to the Same Bank (tRC Limit)

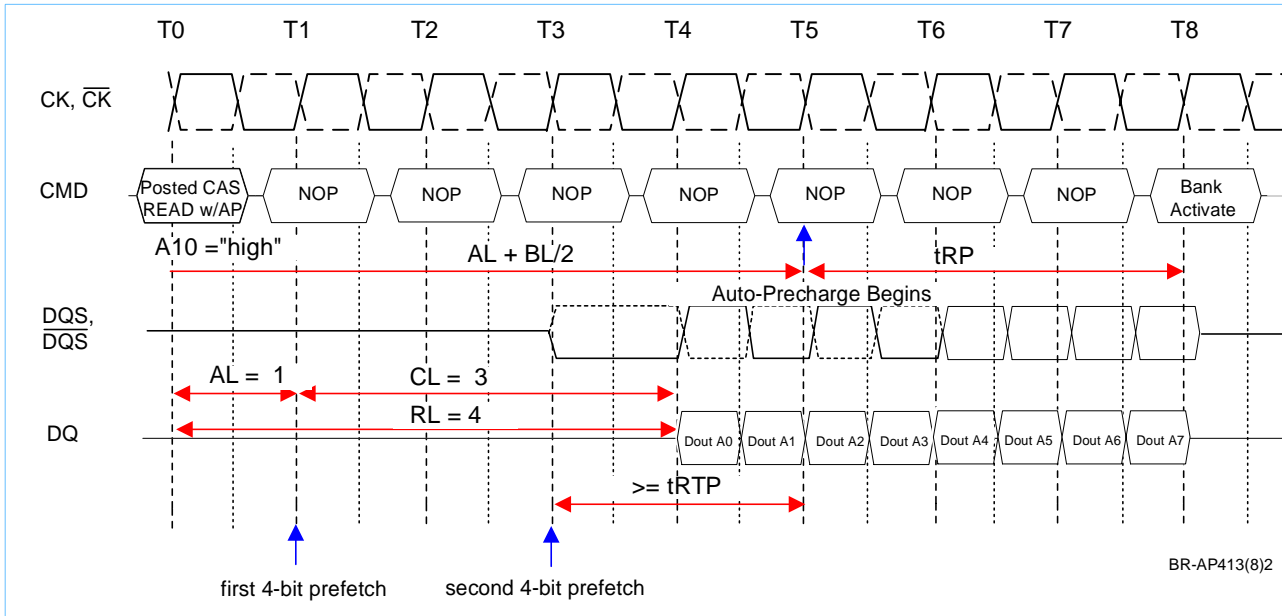**RL = 5 (AL = 2, CL = 3), BL = 4, tRTP <= 2 clocks**

BR-AP5231
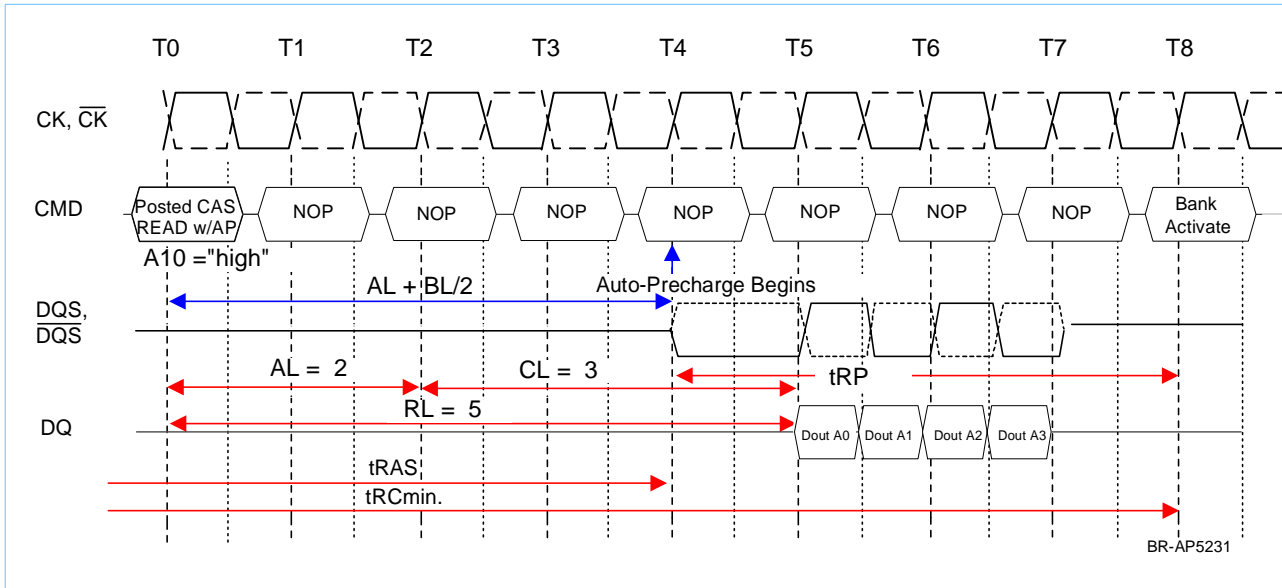
Burst Read with Auto-Precharge followed by an Activation to the Same Bank (tRAS Limit):
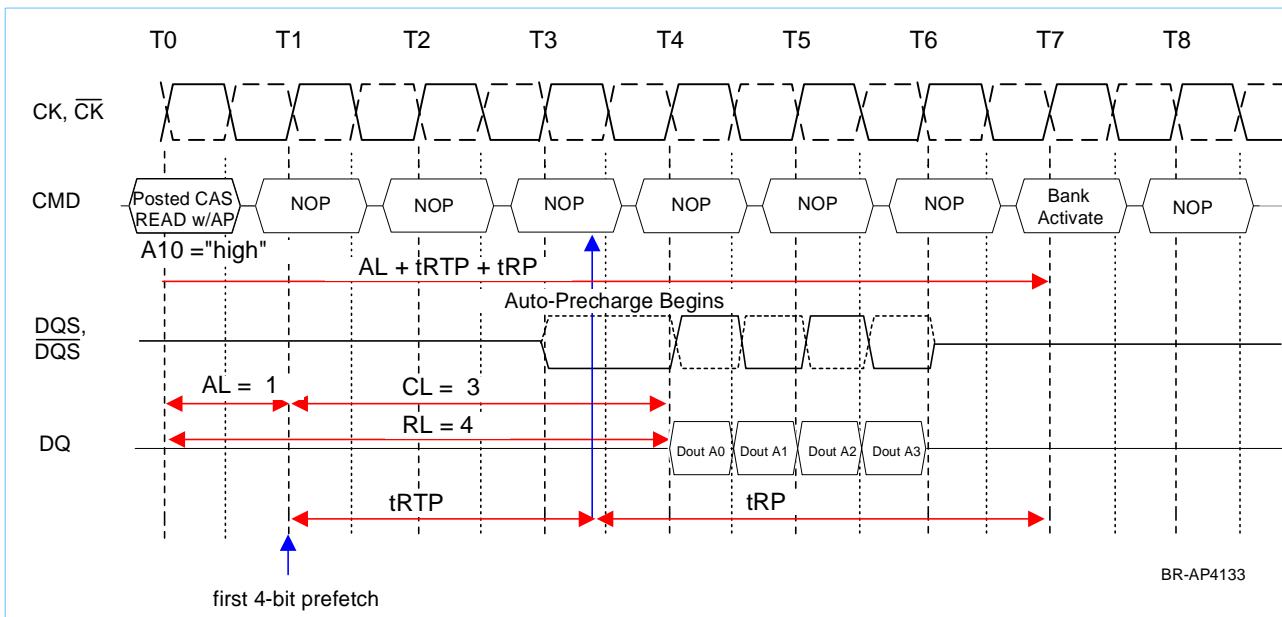
RL = 5 (AL = 2, CL = 3), BL = 4, tRTP <= 2 clocks

BR-AP5232

Burst Read with Auto-Precharge followed by an Activation to the Same Bank:

RL = 4 (AL = 1, CL = 3), BL = 8, tRTP <= 2 clocks

BR-AP413(8)2

Burst Read with Auto-Precharge followed by an Activation to the Same Bank:

RL = 4 (AL = 1, CL = 3), BL = 4, tRTP > 2 clocks


BR-AP4133

Burst Write with Auto-Precharge

If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the write burst plus the write recovery time delay (WR), programmed in the MRS register, as long as tRAS is satisfied. The bank undergoing Auto-Precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

(1) The last data-in to bank activate delay time (tDAL = WR + tRP) has been satisfied.

(2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

In DDR2 SDRAMs the write recovery time delay (WR) has to be programmed into the MRS mode register. As long as the analog twr timing parameter is not violated, WR can be programmed between 2 and 6 clock cycles. Minimum Write to Activate command spacing to the same bank = **WL + BL/2 + tDAL.**

Examples:

Burst Write with Auto-Precharge (tRC Limit) : WL = 2, tDAL = 6 (WR = 3, tRP = 3) , BL = 4

BW-AP223
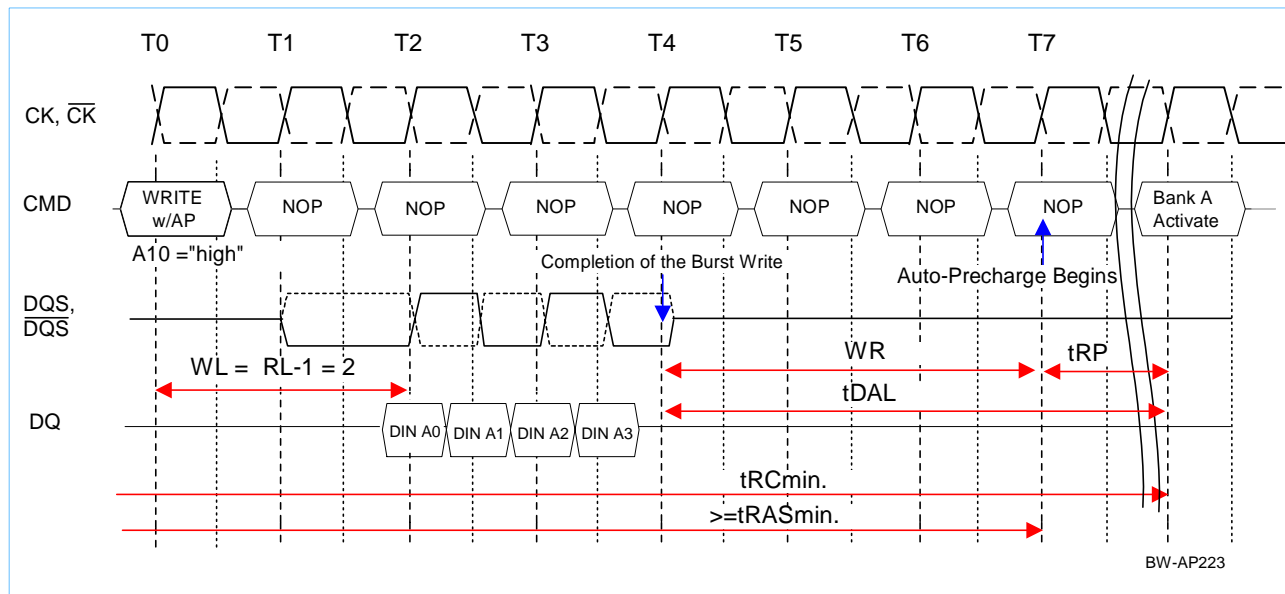
Burst Write with Auto-Precharge (WR + tRP Limit) : WL = 4, tDAL = 6 (WR = 3, tRP = 3), BL = 4

BW-AP423
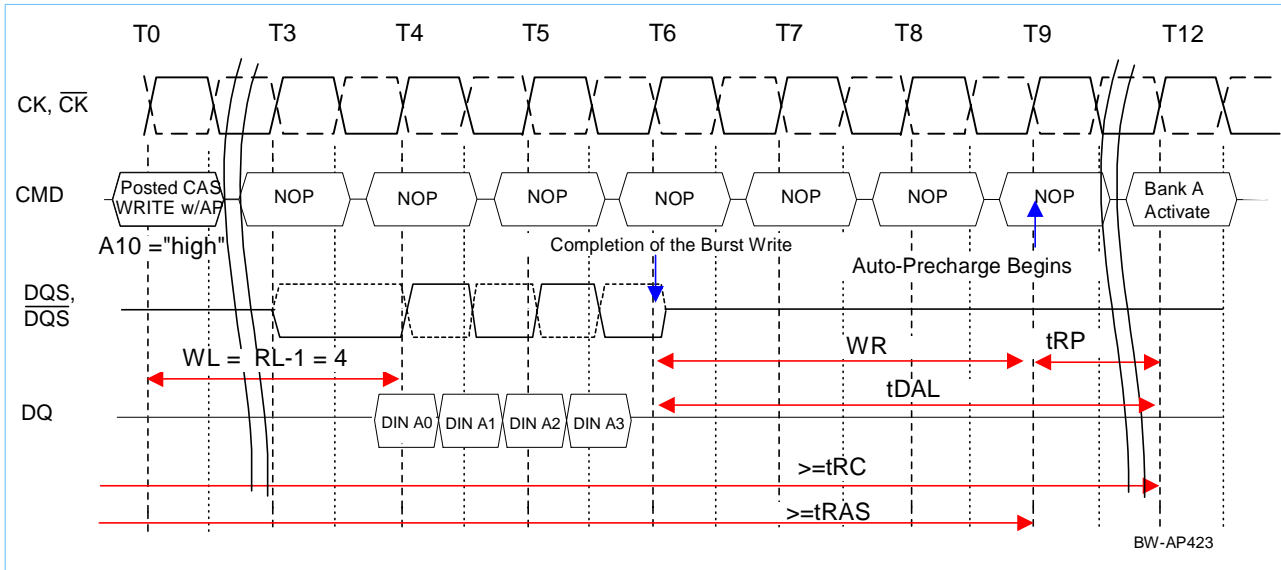
2.7 Refresh

SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways : by an explicit Auto-Refresh command, or by an internally timed event in Self-Refresh mode. Dividing the number of device rows into the rolling 64 ms interval defined the average refresh interval tREFI, which is a guideline to controlles for distributed refresh timing.
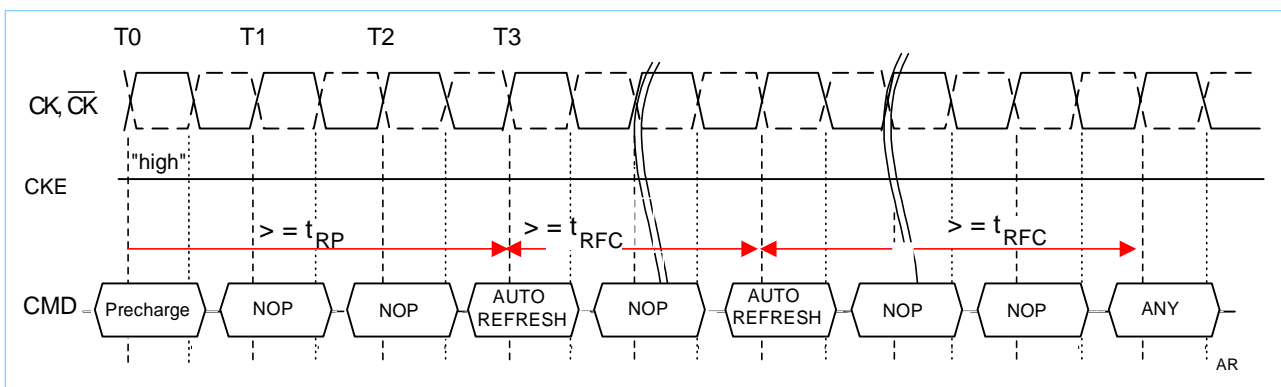
2.7.1 Auto-Refresh Command

Auto-Refresh is used during normal operation of the DDR2 SDRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto-Refresh command. The DDR2 SDRAM requires Auto-Refresh cycles at an average periodic interval of tREFI (maximum).

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Auto-Refresh mode. All banks of the SDRAM must be precharged and idle for a minimum of the Precharge time (t_{RP}) before the Auto-Refresh Command can be applied. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto-Refresh Command and the next Activate Command or subsequent Auto-Refresh Command must be greater than or equal to the Auto-Refresh cycle time (t_{RFC}).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Auto-Refresh command and the next Auto-Refresh command is 9 * tREFI.

2.7.2 Self-Refresh Command

The Self-Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR2 SDRAM retains data without external clocking.

The DDR2 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS(1) command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the DDR2 SDRAM has entered Self-Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self-Refresh Operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self-Refresh operation. Once Self-Refresh Exit command is registered, a delay equal or longer than the tXSNR or tXSRD must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire Self-Refresh exit period (tXSNR or tXSRD) for proper operation. NOP or DESELECT commands must be registered on each positive clock edge during the Self-Refresh exit interval. Since the ODT function is not supported during Self-Refresh operation, ODT has to be turned off tAOFD before entering Self-Refresh Mode and can be turned on again when the tXSRD timing is satisfied.
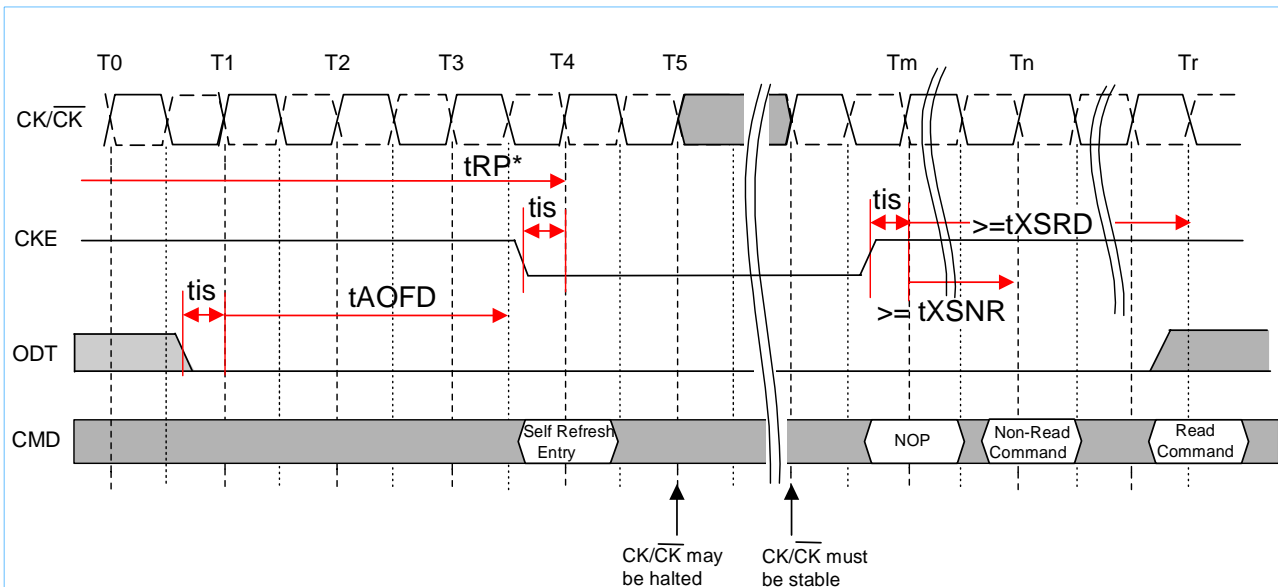
* = Device must be in the "All banks idle" state to entering Self Refresh mode.
ODT must be turned off prior to entering Self Refresh mode.
tXSRD has to be satisfied for a Read or a Read with Auto-Precharge command.
tXSNR has to be satisfied for any command except a Read or a Read with Auto-Precharge command.

2.8 Power-Down

Power-down is synchronously entered when CKE is registered low, along with NOP or Deselect command. CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any other operation such as row activation, pre-charge, auto-precharge or auto-refresh is in progress, but power-down IDD specification will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are precharged, this mode is referred to as *Precharge Power-down*; if power-down occurs when there is a row active in any bank, this mode is referred to as *Active Power-down*. For *Active Power-down* two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to "low" this mode is referred as "standard active power-down mode" and a fast power-down exit timing defined by the tXARD timing parameter can be used. When A12 is set to "high" this mode is referred as a power saving "low power active power-down mode". This mode takes longer to exit from the power-down mode and the tXARDS timing parameter has to be satisfied.
Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are "Don't Care". Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, tXP, tXARD or tXARDS, after CKE goes high. Power-down exit latencies are defined in the AC spec table of this data sheet.

Power-Down Entry

Active Power-down mode can be entered after an activate command. *Precharge Power-down* mode can be entered after a precharge, precharge-all or internal precharge command. It is also allowed to enter power-mode after an Auto-Refresh command or MRS / EMRS(1) command when tMRD is satisfied.
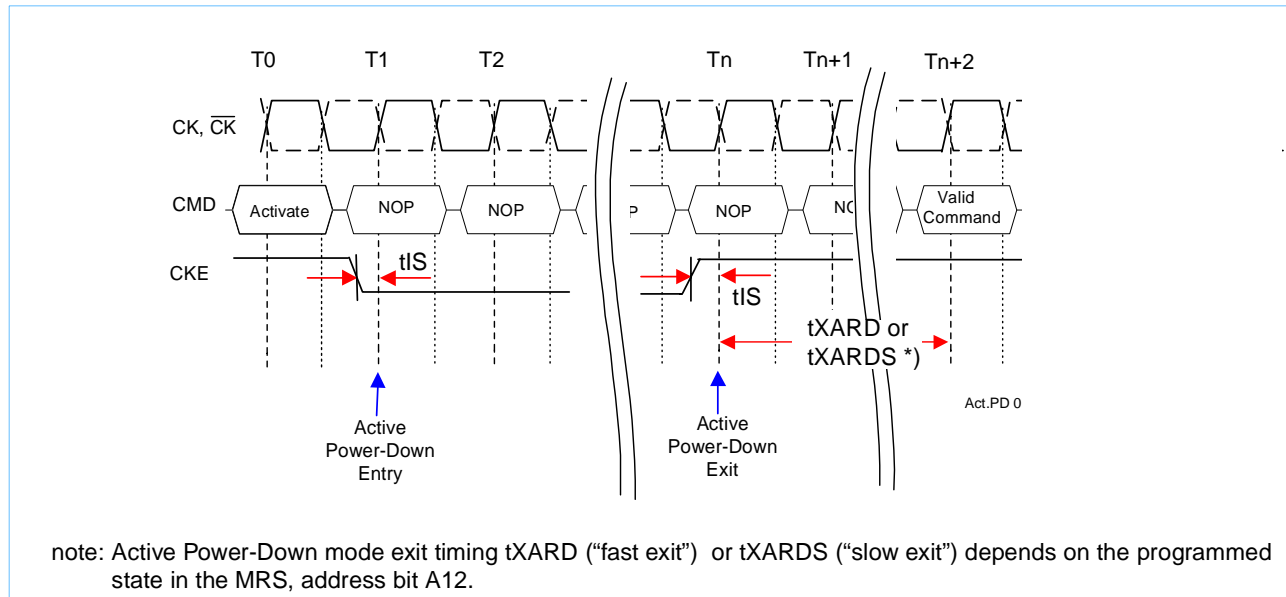
Active Power-down mode entry is prohibited as long as a Read Burst is in progress, meaning CKE should be kept high until the burst operation is finished. Therefore Active Power-Down mode entry after a Read or Read with Auto-Precharge command is allowed after RL + BL/2 is satisfied.

Active Power-down mode entry is prohibited as long as a Write Burst and the internal write recovery is in progress. In case of a write command, active power-down mode entry is allowed when WL + BL/2 + tWTR is satisfied.
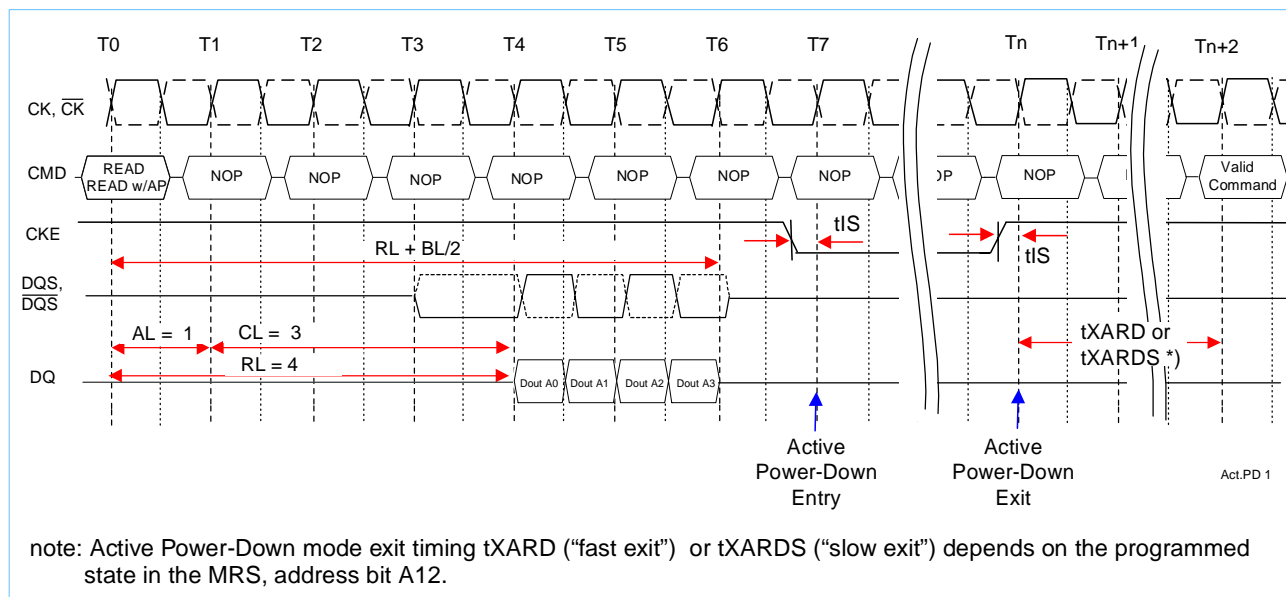
In case of a write command with auto-precharge, power-down mode entry is allowed after the internal precharge command has been executed, which is WL + BL/2 + WR starting from the write with auto-precharge command. In case the DDR2 SDRAM enters the *Precharge Power-down* mode.

Examples:

Active Power-Down Mode Entry and Exit after an Activate Command

note: Active Power-Down mode exit timing tXARD ("fast exit") or tXARDS ("slow exit") depends on the programmed state in the MRS, address bit A12.

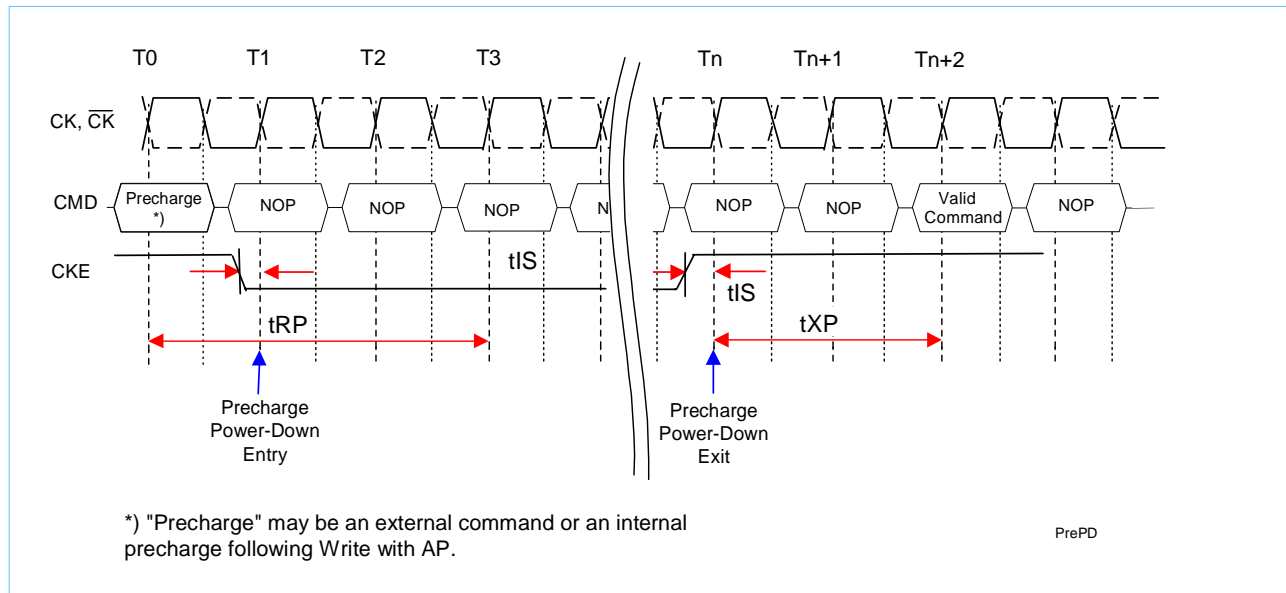**Active Power-Down Mode Entry and Exit after a Read Burst: RL = 4 (AL = 1, CL =3), BL = 4**

note: Active Power-Down mode exit timing tXARD ("fast exit") or tXARDS ("slow exit") depends on the programmed state in the MRS, address bit A12.

Active Power-Down Mode Entry and Exit after a Write Burst: WL = 2, tWTR = 2, BL = 4

note: Active Power-Down mode exit timing tXARD ("fast exit") or tXARDS ("slow exit") depends on the programmed state in the MRS, address bit A12.

Precharge Power Down Mode Entry and Exit

*) "Precharge" may be an external command or an internal precharge following Write with AP.
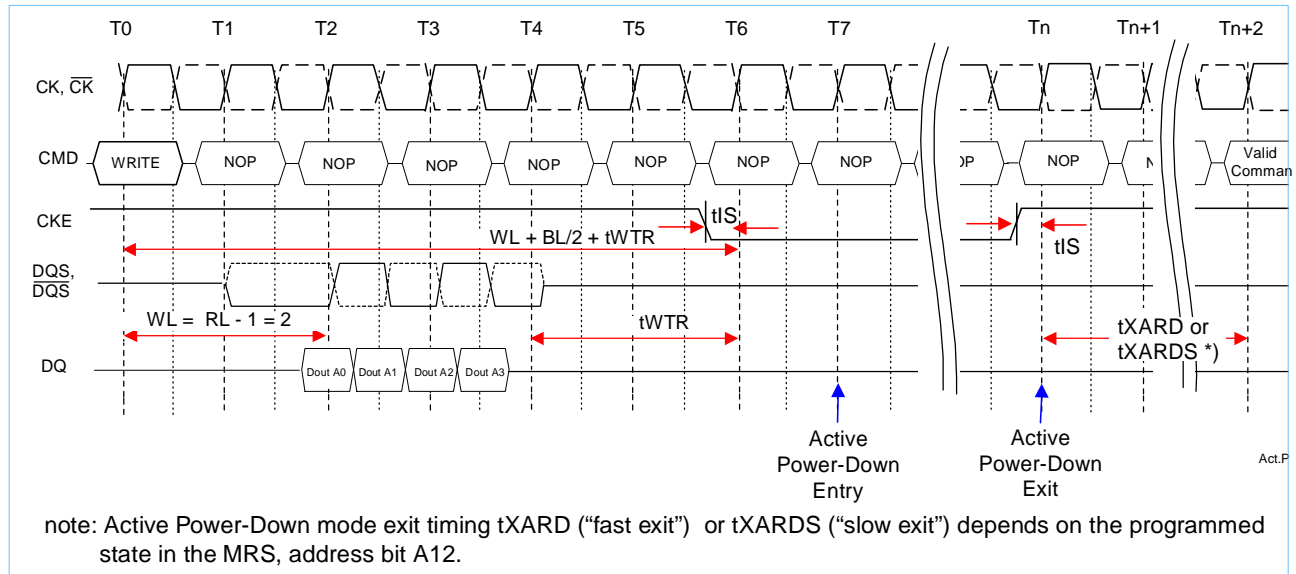
2.9 No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

2.10 Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't care.

2.11 Input Clock Frequency Change

During operation the DRAM input clock frequency can be changed under the following conditions:

a) During Self-Refresh operation

b) DRAM is in precharged power-down mode and ODT is completely turned off.

The DDR2-SDRAM has to be in precharged power-down mode and idle. ODT must be allready turned off and CKE must be at a logic "low" state. After a minimum of two clock cycles after tRP and tAOFD have been satisfied the input clock frequency can be changed. A stable new clock frequency has to be provided, before CKE can be changed to a "high" logic level again. After tXP has been satisfied a DLL RESET command via EMRS(1) has to be issued. During the following DLL re-lock period of 200 clock cycles, ODT must remain off. After the DLL-re-lock period the DRAM is ready to operate with the new clock frequency.

Example:

Input frequency change during Precharge Power-Down mode
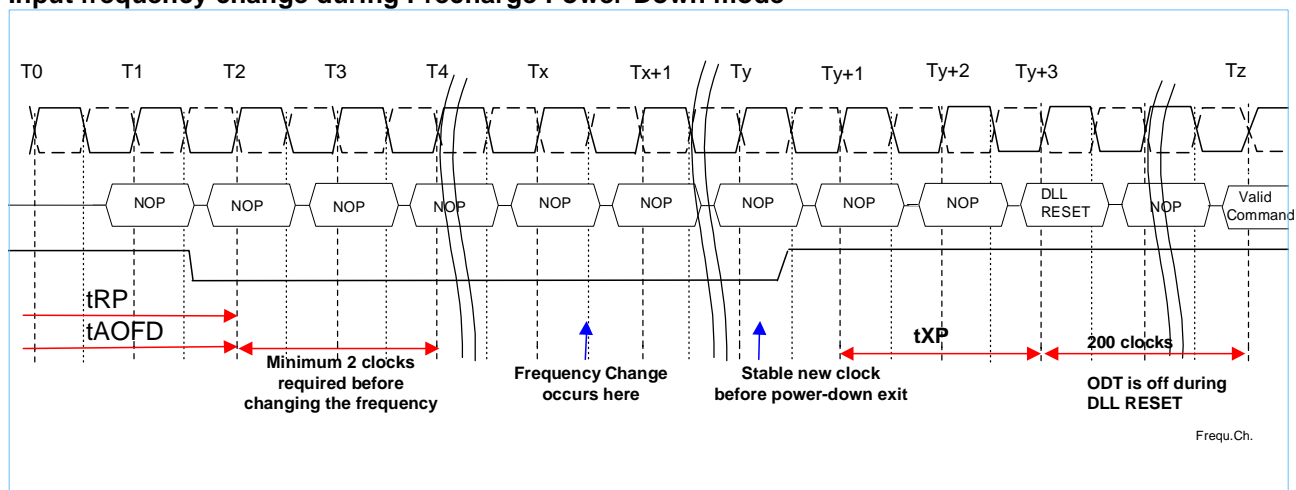
2.12 Asynchronous CKE Low Event

DRAM requires CKE to be maintained "high" for all valid operations as defined in this data sheet. If CKE asynchronously drops "low" during any valid operation DRAM is not guaranteed to preserve the contents of the memory array. If this event occurs, the memory controller must satisfy a time delay (t_{delay}) before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised "high" again. The DRAM must be fully re-initialized as described the the initialization sequence (section 2.2.1, step 4 thru 13). DRAM is ready for normal operation after the initialization sequence. See AC timing parametric table for t_{delay} specification.

Asynchronous CKE Low Event
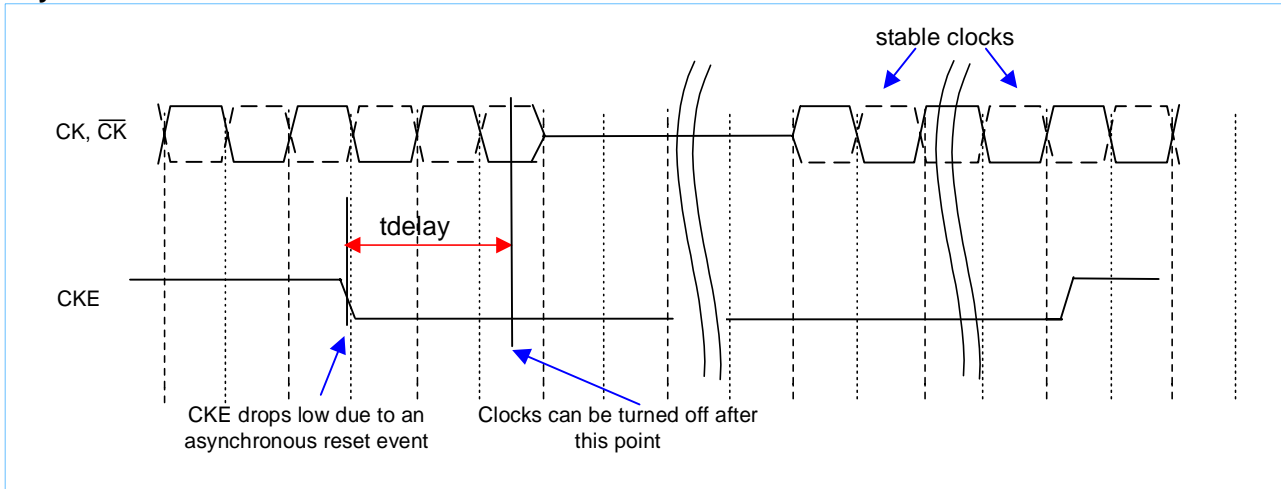
3. Truth Tables

3.1 Command Truth Table

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A13-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1, 2
Auto-Refresh	H	H	L	L	L	H	X	X	X	X	1
Self-Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self-Refresh Exit	L	H	H	X	X	X	X	X	X	X	1
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1, 2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

1. All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and CKE at the rising edge of the clock.
2. Bank addresses (BA0 ~ BA2) determine which bank is to be operated upon. For (E)MRS BAx selects an (Extended) Mode Register.
3. Burst reads or writes at BL = 4 cannot be terminated. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" insection 2.4.6 for details.
4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.7.
5. The state of ODT does not affect the states decribed in this table. The ODT function is not available during Self Refresh.
6. "X" means "H or L (but a defined logic level)".
7. Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restartet through the specified initialization sequence before normal operation can continue.

3.2 Clock Enable (CKE) Truth Table for Synchronous Transistions

Current State[2]	CKE		Command (N) [3,12] $\overline{RAS}, \overline{CAS}, \overline{WE}, \overline{CS}$	Action (N) [3]	Notes
	Previous Cycle [1] (N-1)	Current Cycle [1] (N)			
Power-Down	L	L	X	Maintain Power-Down	11, 13, 15
	L	H	DESELECT or NOP	Power-Down Exit	4, 8, 11, 13
Self Refresh	L	L	X	Maintain Self Refresh	11, 15
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5, 9
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	4,8,10,11, 13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	4,8,10,11
	H	L	AUTOREFRESH	Self Refresh Entry	6, 9, 11, 13
Any State other than listed above	H	H	Refer to the Command Truth Table		7

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
3. Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N).
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occuring during the tXSNR period.
   Read commands may be issued only after tXSRD (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELCT only.
10. Power-Down and Self Refresh can not be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress. See section 2.8 "Power Down" and section 2.7.2 "Self Refresh Command" for a detailed list of restrictions.
11. Minimum CKE high time is 3 clocks, minimum CKE low time is 3 clocks.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
13. The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefor limited by the refresh requirements.
14. CKE must be maintained high while the device is in OCD calibration mode.
15. "X" means "don't care (including floating around VREF)" in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMRS(1)).
16. Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restartet through the specified initialization sequence before normal operation can continue.

3.3 Data Mask (DM) Truth Table

Name (Function)	DM	DQs	Notes
Write Enable	L	Valid	1
Write Inhibit	H	X	1

1. Used to mask write data; provided coincident with the corresponding data.

4. Operating Conditions

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to VSS	-1.0 to + 2.3	V	1
VDDQ	Voltage on VDDQ pin relative to VSS	-0.5 to + 2.3	V	1
VDDL	Voltage on VDDL pin relative to VSS	-0.5 to + 2.3	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to VSS	-0.5 to + 2.3	V	1
T_{STG}	Storage Temperature	-55 to + 100	°C	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4.2 DRAM Component Operating Temperature Range

Symbol	Parameter	min.	max.	Units
TCASE	Component Case Temperature	0	+85	°C

5. AC & DC Operating Conditions

5.1 DC Operating Conditions

5.1.1 Recommended DC Operating Conditions (SSTL_18)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	1
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1
VREF	Input Reference Voltage	0.49 * VDDQ	0.5 * VDDQ	0.51 * VDDQ	V	2, 3
VTT	Termination Voltage	VREF - 0.04	VREF	VREF + 0.04	V	4

1. VDDQ tracks with VDD, VDDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak ac noise on VREF may not exceed +/- 2% VREF (dc).
4. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in die dc level of VREF.

5.1.2 ODT DC Electrical Characteristrics:

Parameter / Condition	Symbol	min.	nom.	max.	Units	Notes
Rtt eff. impedance value for EMRS(1)(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	Ω	1
Rtt eff. impedance value for EMRS(1)(A6,A2)=0,1; 150 ohm	Rtt2(eff)	120	150	180	Ω	1
Deviation of VM with respect to VDDQ / 2	delta VM	- 3.75		+ 3.75	%	2

1) Measurement Definition for Rtt(eff):
        Apply VIHac and VILac to test pin seperately, then measure current I(VIHac) and I(VILac) respectively.

$$Rtt(eff) = (VIHac - VILac) /(I(VIHac) - I(VILac))$$

2) Measurement Defintion for VM:
        Measure voltage (VM) at test pin (midpoint) with no load:

$$delta\ VM =((2* VM / VDDQ) - 1)\ x\ 100\%$$

5.2 DC & AC Logic Input Levels

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) "Enable $\overline{DQS}$" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterisation. In single ended mode, the $\overline{DQS}$ (and $\overline{RDQS}$) signals are internally disabled and don't care.
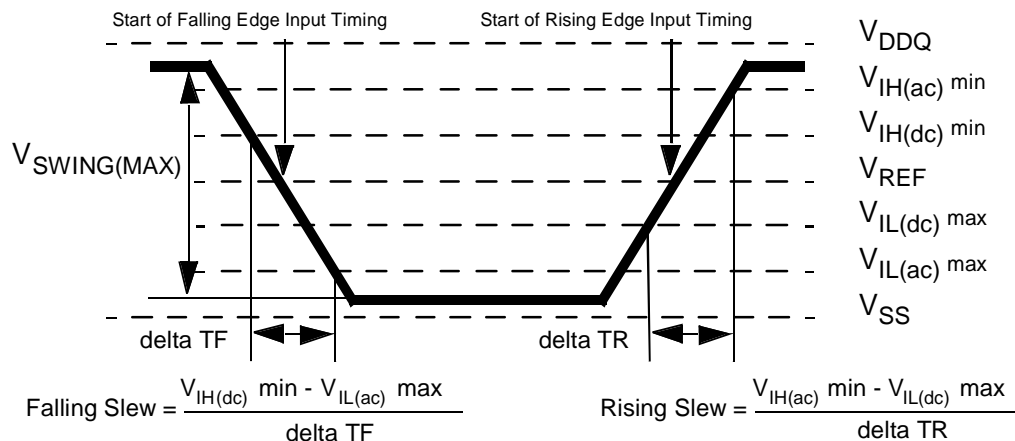
5.2.1 Single-ended DC & AC Logic Input Levels.

Symbol	Parameter	Min.	Max.	Units
VIH (dc)	DC input logic high	VREF + 0.125	VDDQ + 0.3	V
VIL (dc)	DC input low	- 0.3	VREF - 0.125	V
VIH (ac)	AC input logic high	VREF + 0.250	-	V
VIL (ac)	AC input low	-	VREF - 0.250	V

5.2.2 Single-ended AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
VREF	Input reference voltage	0.5 * VDDQ	V	1
VSWING(max)	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V / ns	2, 3

1. Input waveform timing is referenced to the input signal crossing through the VREF level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VIL(dc)max to VIH(ac)min for rising edges and the range from VIH(dc)min to VIL(ac)max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.


$$\text{Falling Slew} = \frac{V_{IH(dc)}\text{ min} - V_{IL(ac)}\text{ max}}{\text{delta TF}}$$

$$\text{Rising Slew} = \frac{V_{IH(ac)}\text{ min} - V_{IL(dc)}\text{ max}}{\text{delta TR}}$$

5.2.3 Differential DC and AC Input and Output Logic Levels

Symbol	Parameter	min.	max.	Units	Notes
VIN(dc)	DC input signal voltage	-0.3	VDDQ + 0.3		1
VID(dc)	DC differential input voltage	0.25	VDDQ + 0.6		2
VID(ac)	AC differential input voltage	0.5	VDDQ + 0.6	V	3
VIX(ac)	AC differential cross point input voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	4
VOX(ac)	AC differential cross point output voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	5

notes:
1) VIN(dc) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$,etc.
2) VID(dc) specifies the input differential voltage VTR - VCP required for switching. The minimum value is equal to VIH(dc) - VIL(dc).
3) VID(ac) specifies the input differential voltage VTR - VCP required for switching. The minimum value is equal to VIH(ac) - VIL(ac).
4) The value of VIX(ac) is expected to equal 0.5 x VDDQ of the transmitting device and VIX(ac) is expected to track variations in VDDQ. VIX(ac) indicates the voltage at which differential input signals must cross.
5) The value of VOX(ac) is expected to equal 0.5 x VDDQ of the transmitting device and VOX(ac) is expected to track variations in VDDQ. VOX(ac) indicates the voltage at which differential input signals must cross.
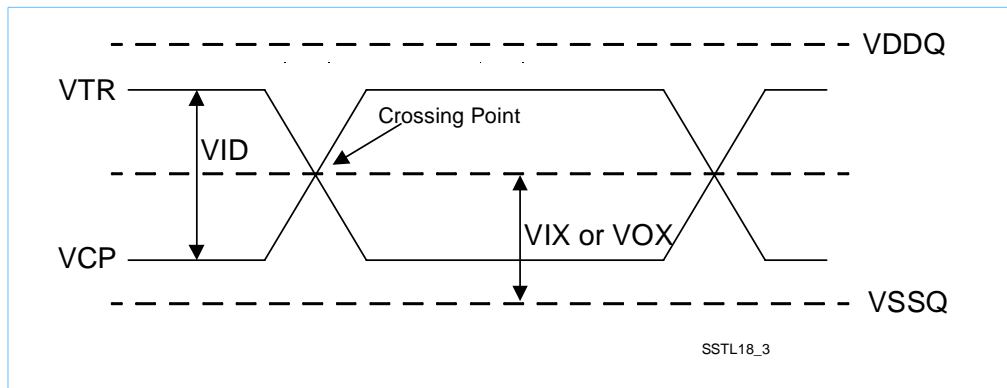
SSTL18_3

5.3 Output Buffer Levels

5.3.1 Output AC Test Conditions

Symbol	Parameter	SSTL_18 Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	$V_{TT} + 0.603$	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	$V_{TT} - 0.603$	V	
V_{OTR}	Output Timing Measurement Reference Level	$0.5 * V_{DDQ}$	V	1

1. The VDDQ of the device under test is referenced.

5.3.2 Output DC Current Drive

Symbol	Parameter	Class II	Units	Notes
I_{OH}	Output Minimum Source DC Current, nominal	-13.4	mA	1, 3, 4
I_{OL}	Output Minimum Sink DC Current, nominal	13.4	mA	2, 3, 4

1. VDDQ = 1.7 V ; V_{OUT} = 1.42 V. (V_{OUT}-VDDQ) / IOH must be less than 21 ohm for values of V_{OUT} between VDDQ and VDDQ - 280 mV.
2. VDDQ = 1.7 V ; V_{OUT} = 280 mV. V_{OUT} / IOL must be less than 21 ohm for values of VOUT between 0V and 280 mV.
3. The dc value of VREF applied to the receiving device is set to VTT
4. The values of I_{OH}(dc) and I_{OL}(dc) are based on the conditions given in note 1 and 2. They are used to test drive current capability to ensure VIHmin. plus a noise margin and VILmax. minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating points along 21 ohm load line to define a convenient current for measurement.

5.3.3 OCD Default Setting Table

Symbol	Description	min.	nominal	max.	Unit	Notes
	Output Impedance	12.6	18	23.4	Ohms	1,2
	Pull-up / Pull down mismatch	0	-	4	Ohms	1,2, 3
	Output Slew Rate	1.5	-	6	V / ns	1, 4, 5

1) Absolute Specification: 0 °C $\leq T_{CASE} \leq$ 85 °C ; V_{DDQ} = 1.8V $\pm$ 0.1V; V_{DD} = 1.8V $\pm$ 0.1V.

2) Impedance measurement condition for output source dc current : VDDQ = 1.7V, VOUT = 1420 mV; (VOUT-VDDQ)/IOH must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current : VDDQ = 1.7 V; VOUT = -280mV; VOUT / IOL must be less than 23.4 ohms for values of VOUT between 0V and 280 mV.

3) Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.

4) Slew rates measured from Vil(AC) to Vih(AC) with the load specified in Section 8.2.

5) The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterisation.

5.3.4 Default Output V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS(1) bits A7~A9 = '111'. Figures in Section 5.3.5 and 5.3.6 show the driver characteristics graphically and the tables sow the same data suitable for input into simulation tools.

5.3.5 Full Strength Default Pullup Driver Characteristics

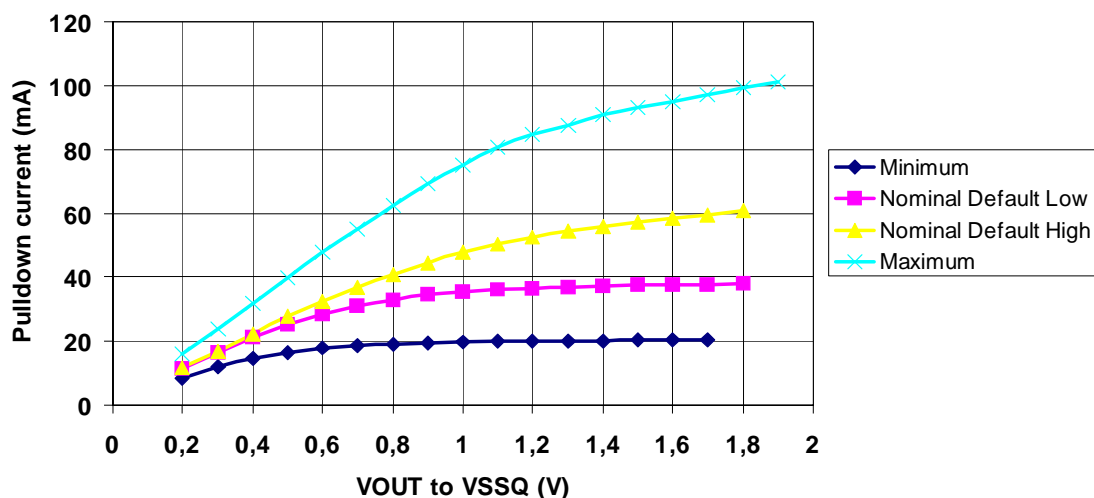| Voltage (V)	Minimum (23.4 Ohms)	Nomal Default low (18 Ohms)	Nomal Default high (18 Ohms)	Maximum (12.6 Ohms)
0.2	-8.5	-11.1	-11.8	-15.9
0.3	-12.1	-16.0	-17.0	-23.8
0.4	-14.7	-20.3	-22.2	-31.8
0.5	-16.4	-24.0	-27.5	-39.7
0.6	-17.8	-27.2	-32.4	-47.7
0.7	-18.6	-29.8	-36.9	-55.0
0.8	-19.0	-31.9	-40.8	-62.3
0.9	-19.3	-33.4	-44.5	-69.4
1.0	-19.7	-34.6	-47.7	-75.3
1.1	-19.9	-35.5	-50.4	-80.5
1.2	-20.0	-36.2	-52.5	-84.6
1.3	-20.1	-36.8	-54.2	-87.7
1.4	-20.2	-37.2	-55.9	-90.8
1.5	-20.3	-37.7	-57.1	-92.9
1.6	-20.4	-38.0	-58.4	-94.9
1.7	-20.6	-38.4	-59.6	-97.0
1.8		-38.6	-60.8	-99.1
1.9				-101.1

The driver characteristics evaluetion conditions are:
Nominal Default 25°C (Tcase) , VDDQ = 1.8 V, typical process
Minimum tbd. °C (Tcase), VDDQ = 1.7V, slow-slow process
Maximum 0 °C (Tcase). VDDQ = 1.9 V, fast-fast process
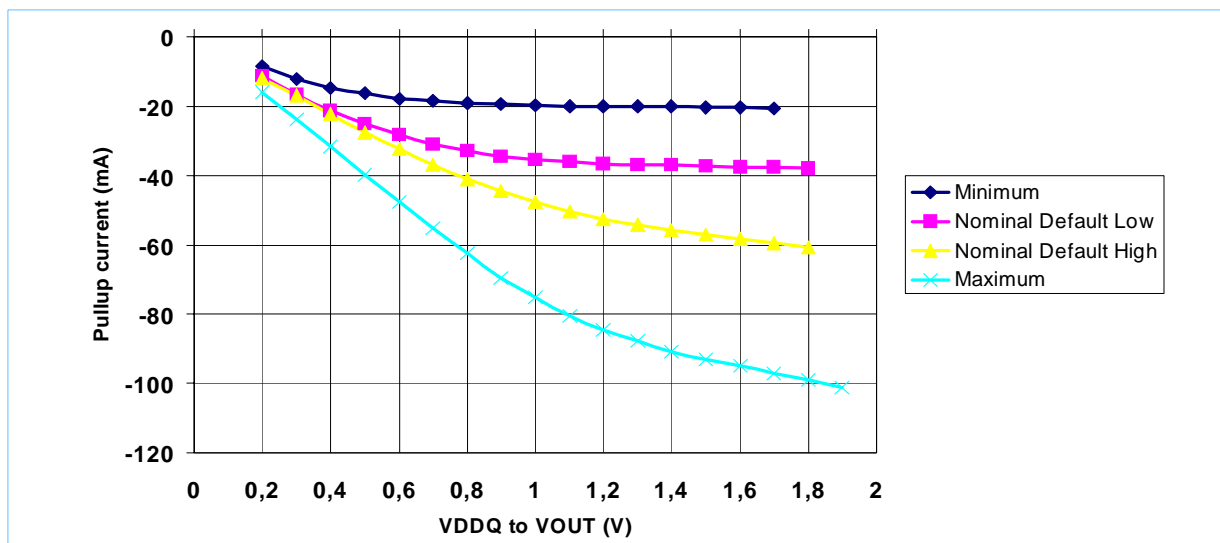
5.3.6 Full Strength Default Pulldown Driver Characteristics

Voltage (V)	Minimum (23.4 Ohms)	Nomal Default low (18 Ohms)	Nomal Default high (18 Ohms)	Maximum (12.6 Ohms)
0.2	8.5	11.3	11.8	15.9
0.3	12.1	16.5	16.8	23.8
0.4	14.7	21.2	22.1	31.8
0.5	16.4	25.0	27.6	39.7
0.6	17.8	28.3	32.4	47.7
0.7	18.6	30.9	36.9	55.0
0.8	19.0	33.0	40.9	62.3
0.9	19.3	34.5	44.6	69.4
1.0	19.7	35.5	47.7	75.3
1.1	19.9	36.1	50.4	80.5
1.2	20.0	36.6	52.6	84.6
1.3	20.1	36.9	54.2	87.7
1.4	20.2	37.1	55.9	90.8
1.5	20.3	37.4	57.1	92.9
1.6	20.4	37.6	58.4	94.9
1.7	20.6	37.7	59.6	97.0
1.8		37.9	60.9	99.1
1.9				101.1

The driver characteristics evaluetion conditions are:
Nominal Default 25°C (Tcase) , VDDQ = 1.8 V, typical process
Minimum tbd. ^{o}C (Tcase), VDDQ = 1.7V, slow-slow process
Maximum 0 ^{o}C (Tcase). VDDQ = 1.9 V, fast-fast process

5.3.7 Calibrated Output Driver V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in the Off-Chip Driver (OCD) Impedance Adjustment. The following tables show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohms step size with no calibration error at the exact nominal conditions only (i.e. perfect calibration procedire, 1.5 ohm maximum step size guaranedd by specification). Real system calibration error needs to be added to these values. It must be understodd that these V-I curves are represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this a system specific phenomena, it cannot be quantified here. the values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characterisitcs tables and figure. in such a situation, the timing paramters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy and uncertainty with DQ to DQ variation, the it is recommende that only the default values to be used. The nominal maximum ad minmum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa.

Full Strength Calibrated Pulldown Driver Characteristics

Voltage (V)	Nominal Minimum (21 Ohms)	Nomal Low (18.75 Ohms)	Nominal (18 ohms)	Nomal High (17.25 Ohms)	Nominal Maximum (15 Ohms)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

The driver characteristics evaluetion conditions are:
Nominal 25°C (Tcase) , VDDQ = 1.8 V, typical process
Nominal Low and Nominal High 25°C (Tcase), VDDQ = 1.8V, any process
Nominal Minimum tbd. ^{o}C (Tcase). VDDQ = 1.7 V, any process
Nominal Maximum 0°C (Tcase), VDDQ = 1.9 V, any process

Full Strength Calibrated Pullup Driver Characteristics

Voltage (V)	Nominal Minimum (21 Ohms)	Nomal Low (18.75 Ohms)	Nominal (18 ohms)	Nomal High (17.25 Ohms)	Nominal Maximum (15 Ohms)
0.2	-9.5	-10.7	-11.4	-11.8	-13.3
0.3	-14.3	-16.0	-16.5	-17.4	-20.0
0.4	-18.3	-21.0	-21.2	-23.0	-27.0

The driver characteristics evaluetion conditions are:
Nominal 25°C (Tcase) , VDDQ = 1.8 V, typical process
Nominal Low and Nominal High 25°C (Tcase), VDDQ = 1.8V, any process
Nominal Minimum tbd. ^{o}C (Tcase). VDDQ = 1.7 V, any process
Nominal Maximum 0°C (Tcase), VDDQ = 1.9 V, any process

5.4 Input / Output Capacitance

Symbol	Parameter	min.	max.	Units
CCK	Input capacitance, CK and $\overline{CK}$	1.5	2.5	pF
CDCK	Input capacitance delta, CK and $\overline{CK}$	-	0.25	pF
CI	Input capacitance, all other input-only pins	1.5	2.5	pF
CDI	Input capacitance delta, all other input-only pins	-	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$	3.0	4.0	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$	-	0.5	pF

5.5 Power & Ground Clamp V-I Characteristics

Power and Ground clamps are provided on address (A0~A13, BA0~BA2), $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, $\overline{WE}$ and ODT pins. The V-I characterisitcs for pins with clamps is shown in the following table :

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

6. IDD Specifications and Measurement Conditions

6.1 IDD Specifications

(VDDQ = 1.8V $\pm$ 0.1V; VDD = 1.8V $\pm$ 0.1V)

Symbol	Parameter/Condition		I/O	-5 DDR2 -400		-3.7 DDR2 -533		-3 DDR2 - 667		Unit	Notes
				typ.	max.	typ.	max.	typ.	max.		
I_{DD0}	Operating Current		x4/ x8 x16	tbd.	80 85	tbd.	85 90	tbd.	95 100	mA	1, 2
I_{DD1}	Operating Current		x4/ x8 x16	tbd.	90 95	tbd.	95 105	tbd.	105 115	mA	1, 2
I_{DD2P}	Precharge Power-Down Current		x4/ x8 x16	tbd.	3.5 4.0	tbd.	5.0 5.0	tbd.	6.0 6.5	mA	1, 2
I_{DD2F}	Precharge Floating Standby Current		x4/ x8 x16	tbd.	32 32	tbd.	40 42	tbd.	51 52	mA	1, 2
I_{DD2Q}	Precharge Quiet Standby Current:		x4/ x8 x16	tbd.	19 19	tbd.	25 25	tbd.	30 32	mA	1, 2
I_{DD3P}	Active Power- Down Standby Current	MRS(12)=0	all	tbd.	12	tbd.	16	tbd.	20	mA	1, 2
		MRS(12)=1	all	tbd.	tbd.	tbd.	tbd.	tbd.	tbd.	mA	1, 2
I_{DD3N}	Active Standby Current		x4/ x8 x16	tbd.	37 39	tbd.	48 50	tbd.	59 63	mA	1, 2
I_{DD4R}	Operating Current Burst Read		x4/x8 x16	tbd.	95 115	tbd.	120 145	tbd.	140 170	mA	1, 2
I_{DD4W}	Operating Current Burst Write		x4/x8 x16	tbd.	100 120	tbd.	125 150	tbd.	150 180	mA	1, 2
I_{DD5B}	Burst Auto-Refresh Current (tRFC=tRFCmin)		x4/x8 x16	tbd.	175 180	tbd.	185 190	tbd.	190 195	mA	1, 2
I_{DD5D}	Distributed Auto-Refresh Current (tRFC=7.8μs)		all	tbd.	5	tbd.	5	tbd.	5	mA	1, 2
I_{DD6}	Self-Refresh Current for standard products		x4/x8 x16	tbd.	3.0 3.1	tbd.	3.0 3.1	tbd.	3.1 3.2	mA	1, 2
I_{DD6}	Self-Refresh Current for low power products		all	tbd.	tbd.	tbd.	tbd.	tbd.	tbd.	mA	1, 2
I_{DD7}	Operating Current		x4/x8 x16	tbd.	220 250	tbd.	240 270	tbd.	265 295	mA	1

1. IDD specifications are tested after the device is properly initialized. IDD parameters are specified with ODT disabled.
2. Input slew rate = 1 V/ns.

6.2 IDD Measurement Conditions

(VDDQ = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V)

Symbol	Parameter/Condition
I_{DD0}	**Operating Current** - **One bank Active - Precharge** tRC = tRCmin; tCK =tCKmin. ; Databus inputs are SWITCHING; Address and control inputs are SWITCHING, $\overline{CS}$ = HIGH between valid commands.
I_{DD1}	**Operating Current** - **One bank Active - Read - Precharge** One bank is accessed with tRCmin , BL = 4, tCK = tCKmin, AL = 0, CL = CLmin.; Address and control inputs are SWITCHING, $\overline{CS}$ = HIGH between valid commands; I_{out} = 0 mA.
I_{DD2P}	**Precharge Power-Down Current:** all banks idle; power-down mode; CKE is LOW; tCK = tCKmin.; Data Bus inputs are FLOATING.
I_{DD2F}	**Precharge Floating Standby Current**: all banks idle; $\overline{CS}$ is LOW; CKE is HIGH; tCK = tCKmin.; Address and control inputs are SWITCHING; Data Bus inputs are FLOATING.
I_{DD2Q}	**Precharge Quiet Standby Current**: all banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Address and control inputs are STABLE; Data Bus inputs are FLOATING.
I_{DD3P}	**Active Power-Down Current**: all banks open; CKE is LOW; Address and control inputs are STABLE; Data Bus inputs are FLOATING. MRS A12 bit is set to "0"(Fast Power-down Exit);
I_{DD3P}	**Active Power-Down Current**: all banks open; CKE is LOW; Address and control inputs are STABLE; Data Bus inputs are FLOATING. MRS A12 bit is set to "1"(Slow Power-down Exit);
I_{DD3N}	**Active Standby Current**: all banks open; $\overline{CS}$ is HIGH; CKE is HIGH; tRC = tRASmax; tCK = tCKmin.; Address and control inputs are SWITCHING; Data Bus inputs are SWITCHING.
I_{DD4R}	**Operating Current - Burst Read:** all banks active; continuous burst reads; BL = 4;AL = 0, CL = CLmin.; tCK = tCKmin.; Address and control inputs are SWITCHING; Data Bus inputs are SWITCHING; IOUT = 0mA.
I_{DD4W}	**Operating Current - Burst Write:** all banks active; continuous burst writes; BL = 4;AL = 0, CL = CLmin.; tCK = tCKmin.; Address and control inputs are SWITCHING; Data Bus inputs are SWITCHING; IOUT = 0mA.
I_{DD5B}	**Burst Auto-Refresh Current**: Refresh command at tRFC = tRFCmin, tCK = tCKmin, $\overline{CS}$ is HIGH between valid commands
I_{DD5D}	**Distributed Auto-Refresh Current**: Refresh command at tREFI; tCK = tCKmin, $\overline{CS}$ is HIGH between valid commands; CKE is LOW except during tRFCmin.
I_{DD6}	**Self-Refresh Current**: CKE ≤ 0.2V; external clock off, CK and $\overline{CK}$ at 0V; tCK = tCKmin; Address and control inputs are FLOATING; Data Bus inputs are FLOATING.

I_{DD7}	**Operating Bank Interleave Read Current:**
	
	1. All bank interleaving with BL = 4; BL = 4, CL = CLmin.;tRCD = tRCDmin.; tRRD = tRRDmin.;AL = tRCD - 1, Iout = 0 mA.
	  Address and control inputs are stable during DESELECT; Data Bus inputs are SWITCHING.
	
	2. Timing pattern:
	    - **_DDR2 -400_** (200Mhz, CL=3) : tck = 5 ns, BL = 4, tRCD = 3 * tck, AL = 2 * tck, tRC = 12 * tck
	     Read : A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D
	    - **_DDR2 -533_** (266Mhz, CL=4) : tck = 3.7 ns, BL = 4, tRCD = 4 * tck, AL = 3 * tck, tRC = 16 * tck
	     Read : A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D
	    - **_DDR2 -667_** (333Mhz, CL=4) : tck = 3 ns, BL = 4, tRCD = 4 * tck, AL = 3 * tck, tRC = 19 * tck
	     Read : A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D

  1. Data Bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
  2. Definitions for IDD :
    LOW is defined as VIN <= VILAC(max.); HIGH is defined as VIN >= VIHAC(min.);
    STABLE is defined as inputs are stable at a HIGH or LOW level
    FLOATING is defined as inputs are VREF
    SWITCHING is defined as inputs are changing between HIGH and LOW every other clock for adress and control signals, and
     inputs changing 50% of each data trasnfer for DQ signals.
  3. Legend : A=Activate, RA=Read with Auto-Precharge, D=DESELECT

6.3 ODT (On Die Termination) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A6 & A2 in the EMRS(1) a "week" or "strong" termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-strate or driving "0" or "1", as long a ODT is enabled during a given periode of time.

ODT current per terminated input pin :

		EMRS(1) State	min.	typ.	max.	Unit
Enabled ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; Data Bus inputs are FLOATING	IODTO	A6 = 0, A2 = 1	tbd.	tbd.	7.5	mA/DQ
		A6 = 1, A2 = 0	tbd.	tbd.	3.75	mA/DQ
Active ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	IODTT	A6 = 0, A2 = 1	tbd.	tbd.	15	mA/DQ
		A6 = 1, A2 = 0	tbd.	tbd.	7.5	mA/DQ
note: For power consumption calculations the ODT duty cycle has to be taken into account						

7. Electrical Characteristics & AC Timing - Absolute Specification

7.1 Timing Parameter by Speed Grade

(V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V) (notes 1-4)

Symbol	Parameter		-5 DDR2 -400		-3.7 DDR2 -533		-3 DDR2 -667		Unit	Notes
			min	max	min	max	min	max		
t_{AC}	DQ output access time from CK / $\overline{CK}$		- 600	+ 600	-500	+500	tbd	tbd	ps	
t_{DQSCK}	DQS output access time from CK / $\overline{CK}$		- 500	+ 500	-450	+450	tbd	tbd	ps	
t_{CH}	CK, $\overline{CK}$ high-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
t_{CL}	CK, $\overline{CK}$ low-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
t_{HP}	Clock Half Period		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})			5
t_{CK}	Clock cycle time	CL = 3	5000	8000	5000	8000	5000	8000	ps	6
		CL = 4 & 5	5000	8000	3750	8000	3000	8000	ps	6
t_{IS}	Address and control input setup time		600	-	600	-	tbd	-	ps	15,17
t_{IH}	Address and control input hold time		600	-	600	-	tbd	-	ps	15,17
t_{DH}	DQ and DM input hold time		400	-	350	-	tbd	-	ps	16,17,18
t_{DS}	DQ and DM input setup time		400	-	350	-	tbd	-	ps	16,17,18
t_{IPW}	Control and Addr. input pulse width (each input)		0.6	-	0.6	-	0.6	-	t_{CK}	
t_{DIPW}	DQ and DM input pulse width (each input)		0.35	-	0.35	-	0.35	-	t_{CK}	
t_{HZ}	Data-out high-impedance time from CK / $\overline{CK}$		-	tACmax	-	tACmax	-	tACmax	ps	7
t_{LZ}	Data-out low-impedance time from CK / $\overline{CK}$		tACmin	tACmax	tACmin	tACmax	tACmin	tACmax	ps	7
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)		-	350	-	300	-	tbd	ps	8
t_{QHS}	Data hold skew factor		-	450	-	400	-	tbd	ps	8
t_{QH}	Data Output hold time from DQS		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}			
t_{DQSS}	Write command to 1st DQS latching transition		WL -0.25	WL +0.25	WL -0.25	WL +0.25	WL -0.25	WL +0.25	t_{CK}	
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35	-	0.35	-	0.35	-	t_{CK}	
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2	-	0.2	-	0.2	-	t_{CK}	
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2	-	0.2	-	0.2	-	t_{CK}	
t_{MRD}	Mode register set command cycle time		2	-	2	-	2	-	t_{CK}	
t_{WPRES}	Write preamble setup time		0	-	0	-	0	-	ps	9
t_{WPRE}	Write preamble		0.25	-	0.25	-	0.25	-	t_{CK}	
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	10
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
t_{RPST}	Read postamble		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	
t_{RAS}	Active to Precharge command		45	70000	45	70000	45	70000	ns	20

7.1 Timing Parameter by Speed Grade

(V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V) (notes 1-4)

Symbol	Parameter		-5 DDR2 -400		-3.7 DDR2 -533		-3 DDR2 -667		Unit	Notes
			min	max	min	max	min	max		
t_{RC}	Active to Active/Auto-Refresh command period		60	-	60	-	57	-	ns	
t_{RFC}	Auto-Refresh to Active/Auto-Refresh command period		127.5	-	127.5	-	127.5	-	ns	11
t_{RCD}	Active to Read or Write (with and without Auto-Precharge) delay		15	-	15	-	12	-	ns	10
t_{RP}	Precharge command period (single bank)		15	-	15	-	12	-	ns	21
$t_{RP(A)}$	Precharge-All (8 banks) command period		tRP+1t$_{CK}$	-	tRP+1t$_{CK}$	-	tRP+1t$_{CK}$	-	ns	21
t_{RRD}	Active bank A to Active bank B command	x4 & x8 (1k page size)	7.5	-	7.5	-	7.5	-	ns	
		x16 (2k page size)	10	-	10	-	10		ns	
t_{CCD}	$\overline{CAS}$ A to $\overline{CAS}$ B Command Period		2		2		2		t$_{CK}$	
t_{WR}	Write recovery time		15	-	15	-	12	-	ns	
t_{DAL}	Auto-Precharge write recovery + precharge time		WR+tRP	-	WR+tRP	-	WR+tRP	-	t$_{CK}$	12
t_{WTR}	Internal write to read command delay		10	-	7.5	-	7.5	-	ns	13
t_{RTP}	Internal read to precharge command delay		7.5	-	7.5	-	7.5	-	ns	
t_{XARD}	Exit power down to any valid command (other than NOP or Deselect)		2	-	2	-	2	-	t$_{CK}$	14
t_{XARDS}	Exit active power-down mode to read command (slow exit, lower power)		6 - AL	-	6 - AL	-	6 - AL	-	t$_{CK}$	14
t_{XP}	Exit precharge power-down to any valid command (other than NOP or Deselect)		2	-	2	-	2	-	t$_{CK}$	
t_{XSRD}	Exit Self-Refresh to read command		200	-	200	-	200	-	t$_{CK}$	
t_{XSNR}	Exit Self-Refresh to non-read command		tRFC+10	-	tRFC+10	-	tRFC+10	-	ns	
t_{CKE}	CKE minimum high and low pulse width		3	-	3	-	3	-	t$_{CK}$	
t_{REFI}	Average Periodic Refresh Interval		-	7.8	-	7.8	-	7.8	µs	18
t_{OIT}	OCD drive mode output delay		0	12	0	12	0	12	ns	
t_{DELAY}	Minimum time clocks remain ON after CKE asynchronously drops LOW		tIS+tCK +tIH	-	tIS+tCK +tIH	-	tIS+tCK +tIH	-	ns	21

Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restartet through the specified initialization sequence before normal operation can continue.

7.2 ODT AC Electrical Characteristics and Operating Conditions (all speed bins)

Symbol	Parameter / Condition	min.	max.	Units	Notes
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	tAC(min)	tAC(max) + 1ns	ns	23
t_{AONPD}	ODT turn-on (Power-Down Modes)	tAC(min) + 2ns	2 t_{CK} + tAC(max) + 1ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	tAC(min)	tAC(max) + 0.6ns	ns	24
t_{AOFPD}	ODT turn-off (Power-Down Modes)	tAC(min) + 2ns	2.5 t_{CK} + tAC(max) + 1ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	-	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	-	t_{CK}	

7.3 Notes for Electrical Characteristics & AC Timing

1. Input slew rate is 1 V/ns and AC timings are guaranteedd for linear signal transitions.
For other slew rates see the derating tables on the next pages.

2. The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross:the DQS / $\overline{DQS}$ input reference level is the crosspoint when in differential strobe mode; the input reference level for signals other than CK/$\overline{CK}$, or DQS / $\overline{DQS}$ is VREF.

3. Inputs are not recognized as valid until VREF stabilizes. During the period before VREF stabilizes, CKE = 0.2 x VDDQ is recognized as LOW.

4. The output timing reference voltage level is VTT.

5. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH.

6. For input frequency change during DRAM operation, see the 2.11 section of this datasheet..

7. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8. These parameters guarantee device timing, but they are not necessarily tested on each device.

9. The specific requirement is that DQS and $\overline{DQS}$ be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}. When programmed in differential strobe mode, DQS is always the logic complement of DQS except when both are in high-Z.

10. The maximum limit for this parameter is not a device limit. The device operate with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

11. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
(Note that tRFC depends on DRAM density)

12. For each of the terms, if not allready an integer, round to the next highest integer. tCK refers to the application clock period. WR refers to the WR parameter stored in the MRS.

13. tWTR is at least two clocks independent of operation frequency.

14. User can choose two different active power-down modes for additional power saving via MRS address bit A12.
In "standard active power-down mode" (MRS, A12 = "0") a fast power-down exit timing tXARD can be used. In "low active power-down mode" (MRS, A12 ="1") a slow power-down exit timing tXARDS has to be satisfied.

15. Timings are guaranteed with command / address input slew rate of 1.0 V/ns. (see the Section 8.3 for derating values)

16. Timings are guaranteed with data / mask input slew rate of 1.0 V/ns.(see the Section 8.3 for derating values)

17. Timings are guaranteed with CK /$\overline{CK}$ differential slew rate 2.0 V/ns, and DQS/$\overline{DQS}$ (and RDQS/$\overline{RDQS}$) differential slew rate 2.0 V/ns in differential strobe mode.(see the Section 8.3 for derating values)

18. If refresh timing or tDS / tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

19. The tRCD timing parameter is valid for both activate command to read or write command with and without Auto-Precharge. Therefore a separate parameter tRAP for activate command to read or write command with Auto-Precharge is not neccessary anymore.

20. tRAS(max) is calculated from the maximum amount of time a DDR2 device can operate without a Refresh command which is equal to 9 * tREFI.

21. tRP(A) for a Prechall-All command for an 8 bank device is equal to trp + 1 * tck, where trp are the values for a single bank precharge.

22. The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during power-down, a specific procedure is required as describes in section 2.12.

23. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max is when the ODT resistance is fully on. Both are measure from tAOND.

24. ODT turn off time min is when the device starts to turn off ODT resistance
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

8. Reference Loads, Slew Rates and Slew Rate Derating

8.1 Reference Load for Timing Measurements

The figure represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. This load circuit is also used for output slew rate measurements.

Note: The output timing reference voltage level for single ended signals is the crosspoint with VTT.
The output timing reference voltage level for differential signals is the crosspoint of the
true (e.g. DQS) and the complement (e.g. DQS) signal.
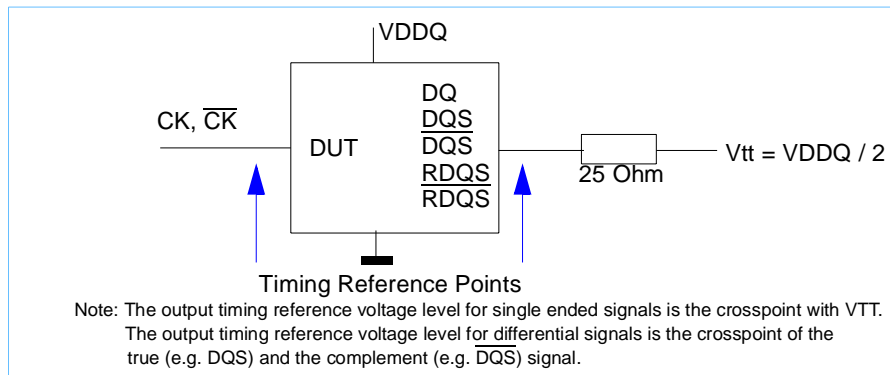
8.2 Slew Rate Measurements and Derating
8.2.1 Output Slew Rate

Output slew rate is characterized under the test conditions as shown in the figure below
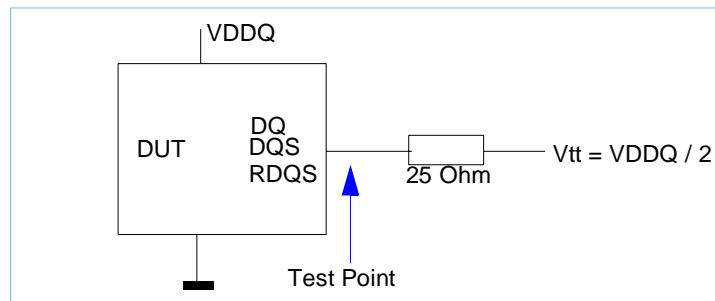
Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals.For differential signals (e.g. DQS - DQS) output slew rate is measured between DQS - DQS = - 500 mV and DQS - DQS = + 500 mV.Output slew rate is guaranteed by design, but is not necessarilty tested on each device.

8.2.2 Input Slew Rate

Input slew for single ended signals is measured from dc-level to ac-level from VREF - 125 mV to VERF + 250 mV for rising edges and from VREF + 125 mV to VREF - 250 mV for falling edges.
For differential signals (e.g. CK - CK) slew rate for rising edges is measured from CK - CK = -250 mV to
CK -CK = +500 mV (250 mV to -500 mV for falling edges). Test conditions are the same as for timing measurements.

8.3 Slew Rate Derating Tables

8.3.1 Data Setup and Hold Time Derating Tables

DDR2-400		DQS Single-ended Slew Rate												
		0.4 V/ns		0.5 V/ns		0.6 V/ns		0.7V/ns		0.8 V/ns		0.9 V/ns		1.0 V/ns	
		Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)
DQ/DM Slewrate (V/ns)	1.0	-	-	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD
	0.9	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	0.8	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	0.7	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-
	0.6	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-
	0.5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-
	0.4	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-	-	-

Note: Slew rate is measured using AC Parametric test condition definition and does not vary more than +/- TBD % from linear signal

DDR2-400		DQS, DQS Differential Slew Rate												
		0.8 V/ns		1.0 V/ns		1.2 V/ns		1.4 V/ns		1.6 V/ns		1.8 V/ns		2.0 V/ns	
		Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)
DQ/DM Slewrate (V/ns)	1.0	-	-	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD
	0.9	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	0.8	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	0.7	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-
	0.6	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-
	0.5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-
	0.4	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-	-	-

Note: Slew rate is measured using AC Parametric test condition definition and does not vary more than +/- TBD % from linear signal

DDR2-533		DQS Single-ended Slew Rate												
		0.4 V/ns		0.5 V/ns		0.6 V/ns		0.7V/ns		0.8 V/ns		0.9 V/ns		1.0 V/ns	
		Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)
DQ/DM Slewrate (V/ns)	1.0	-	-	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD
	0.9	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	0.8	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	0.7	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-
	0.6	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-
	0.5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-
	0.4	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-	-	-

Note: Slew rate is measured using AC Parametric test condition definition and does not vary more than +/- TBD % from linear signal

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DDR2-533		DQS, DQS Differential Slew Rate												
		0.8 V/ns		1.0 V/ns		1.2 V/ns		1.4 V/ns		1.6 V/ns		1.8 V/ns		2.0 V/ns	
		Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)	Δ tDS (ns)	Δ tDH (ns)
DQ/DM Slewrate (V/ns)	1.0	-	-	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD
	0.9	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	0.8	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	0.7	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-
	0.6	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-
	0.5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-
	0.4	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-	-	-
Note: Slew rate is measured using AC Parametric test condition definition and does not vary more than +/- TBD % from linear signal															

8.3.2 Input Setup and Hold Time Derating Tables

DDR2-400		CK, CK Differential Slew Rate					
		1.0 V/ns		1.5 V/ns		2.0 V/ns	
		Δ tIS (ns)	Δ tIH (ns)	Δ tIS (ns)	Δ tIH (ns)	Δ tIS (ns)	Δ tIH (ns)
Command/Address Slewrate (V/ns)	1.0	TBD	TBD	TBD	TBD	TBD	TBD
	0.5	TBD	TBD	TBD	TBD	TBD	TBD
	0.4	TBD	TBD	TBD	TBD	TBD	TBD
	0.3	TBD	TBD	TBD	TBD	TBD	TBD
	0.2	TBD	TBD	TBD	TBD	TBD	TBD
	0.15	TBD	TBD	TBD	TBD	TBD	TBD
	0.1	TBD	TBD	TBD	TBD	TBD	TBD
Note: Slew rate is measured using AC Parametric test condition definition and does not vary more than +/- TBD % from linear signal							

DDR2-533		CK, CK Differential Slew Rate					
		1.0 V/ns		1.5 V/ns		2.0 V/ns	
		Δ tIS (ns)	Δ tIH (ns)	Δ tIS (ns)	Δ tIH (ns)	Δ tIS (ns)	Δ tIH (ns)
Command/Address Slewrate (V/ns)	1.0	TBD	TBD	TBD	TBD	TBD	TBD
	0.5	TBD	TBD	TBD	TBD	TBD	TBD
	0.4	TBD	TBD	TBD	TBD	TBD	TBD
	0.3	TBD	TBD	TBD	TBD	TBD	TBD
	0.2	TBD	TBD	TBD	TBD	TBD	TBD
	0.15	TBD	TBD	TBD	TBD	TBD	TBD
	0.1	TBD	TBD	TBD	TBD	TBD	TBD
Note: Slew rate is measured using AC Parametric test condition definition and does not vary more than +/- TBD % from linear signal							

8.4 Overshoot and Undershoot Specification

8.4.1 AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	DDR2 -400	DDR2 -533	DDR2 -667	Units
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	V
Maximum overshoot area above VDD	0.75	0.56	0.45	V.ns
Maximum undershoot area below VSS	0.75	0.56	0.45	V.ns
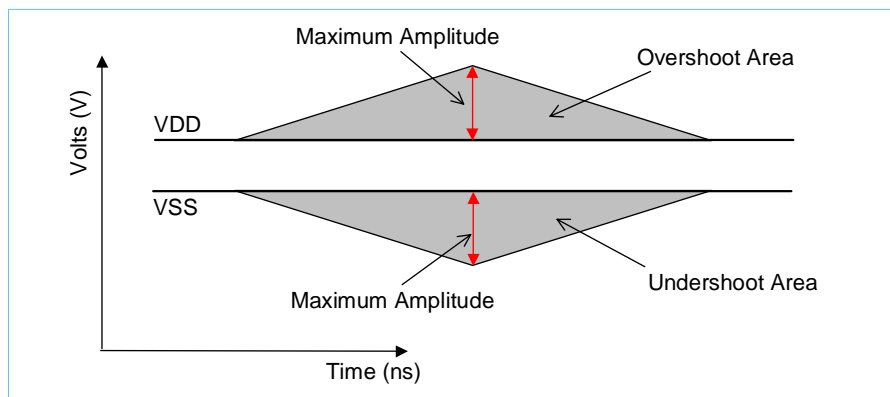
8.4.2 AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	DDR2 -400	DDR2 -533	DDR2 -667	Units
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	V
Maximum overshoot area above VDDQ	0.38	0.28	0.23	V.ns
Maximum undershoot area below VSSQ	0.38	0.28	0.23	V.ns
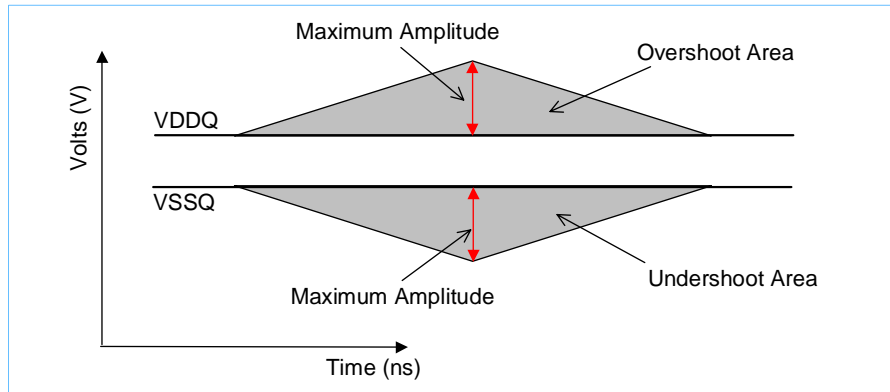
9.0 Package Dimensions

60 balls PTFBGA-Package
10,0 mm x 20,0 mm
MO-207 Variation DM-z (x4, x8)
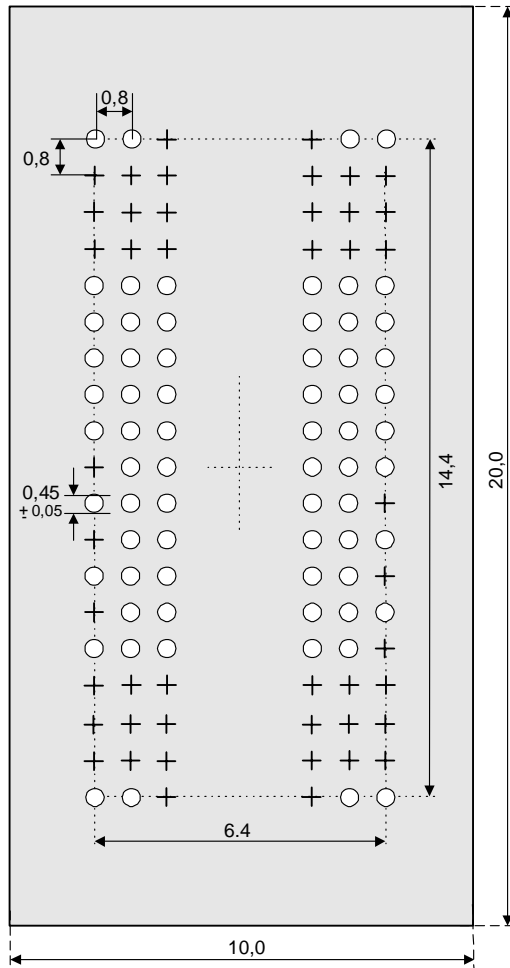
84 balls PTFBGA-Package
10,0 mm x 20,0 mm
MO-207 Variation DL-z (x16)
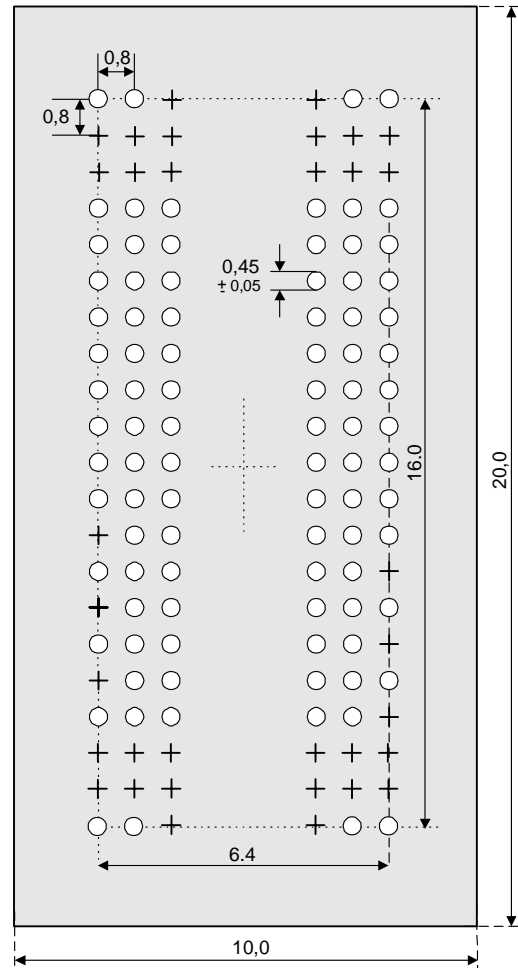
(see balls through package)

Package is lead and halogen free

10. DDR2 Component Nomenclature

		1	2	3	4	5	6	7	8	9
Example :		HYB	18	T	1G	40	0	A	F	-5

1	INFINEON Component Prefix	HYB for DRAM Components	6	Product Variations	0 = standard 2 = two dies in one package
2	Power Supply Voltage	18 = 1.8 V Power Supply	7	Die Revision	A = 1st Generation B = 2nd Generation C = 3rd Generation
3	DRAM Technology	T = DDR2	8	Package Type	F = lead and halogen free BGA packages
4	Memory Density	256 = 256 Mb 512 = 512 Mb 1G = 1024Mb 2G = 2048 Mb	9	Speed Grade	-5 = DDR2-400 -3.7 = DDR2-533 -3 = DDR2-667
5	Memory Organisation	40 = x4, 4 data in/outputs 80 = x8, 8 data in/outpus 16 = x16, 16 data in/ouputs			

11. Content

Content

Attention please !

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies. This information describes the type of components and shall not be considered as assured characteristics. Terms of delivery and rights to change design reserved.

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Please use the recycling operators known to you. We can help you - get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport. For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

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1. A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system.

2. Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.