National Semiconductor

PRELIMINARY

GAL6001® Generic Array Logic

General Description

Using a high performance E²CMOS™ technology, National Semiconductor has produced a next-generation programmable logic device, the GAL6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL6001 offers the highest degree of functional integration, flexibility, and speed currently available in a 24 pin, 300-mil package.

The GAL6001 has ten programmable Output Logic MacroCells (OLMC) and eight programmable "buried" State Logic MacroCells (SLMC). In addition, there are ten input Logic MacroCells (ILMC) and ten I/O Logic MacroCells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

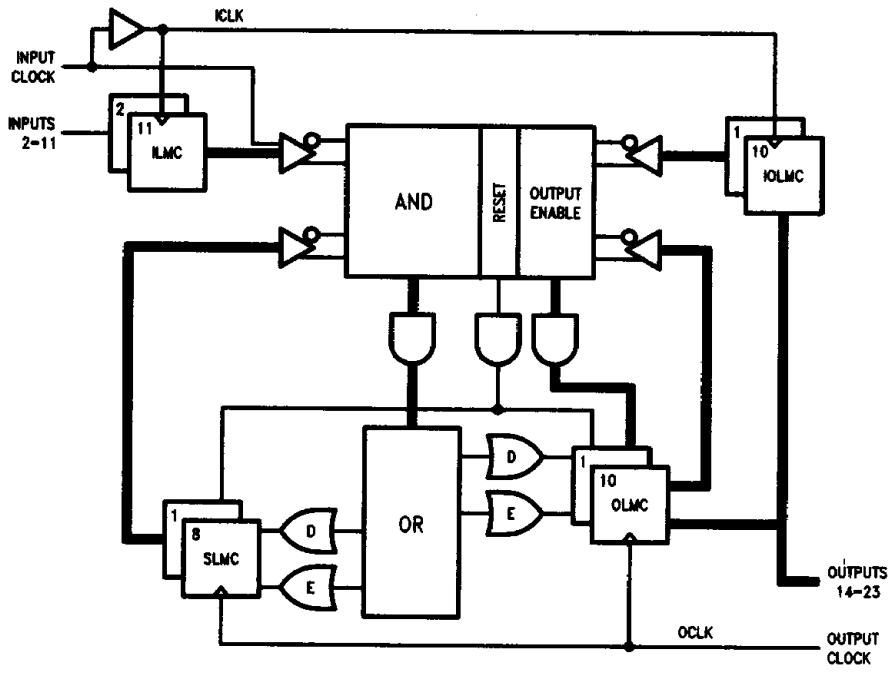
Advanced features that simplify programming and reduce test time, coupled with E²CMOS reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL6001 during manufacture. This allows National to guarantee 100% performance to specifications. In addition, data retention of 20 years and a minimum of 100 erase/write cycles are guaranteed.

Programming is accomplished using standard hardware and software tools. In addition, an Electronic Signature word is available for storage of user specified data, and a security cell is provided to protect proprietary designs.

Features

- Electrically erasable cell technology
  - — Instantly reconfigurable logic
  - — Instantly reprogrammable cells
  - — Guaranteed 100% yields
- High performance E²CMOS technology
  - — Low power: 150 mA maximum
  - — High speed:
    - 15 ns max. clock to output delay
    - 25 ns max. setup time
    - 30 ns max. propagation delay
- TTL compatible inputs and outputs
- Unprecedented functional density
  - — 10 output logic macrocells
  - — 8 state logic macrocells
  - — 20 input and I/O logic macrocells
- High-level design flexibility
  - — 78 x 64 x 36 FPLA architecture
  - — Separate state register and input clock pins
  - — Functionally supersets existing 24-pin PAL® and IFL™ devices
  - — Asynchronous clocking
- 24-pin, 300-mil DIP or 28-lead PLCC
- High speed programming algorithm
- 20-year data retention

Block Diagram - GAL6001



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Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.5 to +7V
Input Voltage Applied	−0.5 to V_{CC} +1.0V
Off-state Output Voltage Applied	−0.5 to V_{CC} +1.0V
Storage Temperature	−40°C to +85°C

Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

SUPPLY VOLTAGE AND TEMPERATURE

Symbol	Parameter	Temperature Range						Units
		Commercial			Industrial			
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	4.5	5	5.5	V
T_A	Ambient Temperture	0		75	−40		85	°C
T_C	Case Temperature	0		75	−40		85	°C

Capacitance (Note 1) (T_A = 25°C, f = 1.0 MHz)

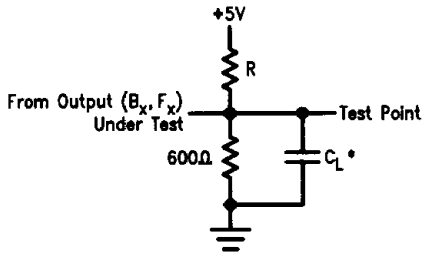
Symbol	Parameter	Test Conditions	Maximum*	Units
C_I	Input Capacitance	V_{CC} = 5.0V, V_I = 2.0V	8	pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V	10	pF
CB	Bidirectional Pin Cap	V_{CC} = 5.0V, V_B = 2.0V	10	pF

*Guaranteed but not 100% tested.

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns (0.3V to 2.7V)
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.



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*C_L includes jig and probe total capacitance

GAL6001 Reset Timing Specifications

Symbol	Parameter	Min	Typ	Max	Units
tPR	Reset Circuit Power-Up			100	ns
tRESET	Register Reset Time from Valid V_{CC}			45	μs

Electrical Characteristics over recommended operating conditions

Symbol	Parameter	Test Conditions		Temp Range	Min	Max	Units
I_{IH}, I_{IL}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC} Max				±10	μA
I_{BZH}, I_{BZL}	Bidirectional Pin Leakage Current	GND ≤ V_{IN} ≤ V_{CC} Max				±10	μA
I_{CC}	Operating Power Supply Current	F = 15 MHz V_{CC} = V_{CC} Max		COM'L		150	mA
				IND		180	mA
I_{OS}	Output Short Circuit (Note 1)	V_{CC} = 5.0V, V_{OUT} = GND			−30	−130	mA
V_{OL}	Output Low Voltage	V_{CC} = V_{CC} Min	I_{OL} = 16 mA	COM/IND		0.5	V
V_{OH}	Output High Voltage	V_{CC} = V_{CC} Min	I_{OH} = −3.2 mA	COM/IND	2.4		V
V_{IH}	Input High Voltage				2.0	V_{CC}+1	V
V_{IL}	Input Low Voltage					0.8	V

Note 1: One Output at a time for a maximum duration of one second.

Switching Characteristics over recommended operating conditions

Symbol	Parameter	Test Conditions		6001-30 COM		6001-35 COMM		Units
		R(Ω)	C_L (pF)	Min	Max	Min	Max	
t_{DVQV1}	Delay from Input or I/O to Output (Note 1)	300	50		30		3540	ns
t_{DVQZ}	Delay from Input or I/O to Outputs Off (Disable)	Infinite	5		25		3035	ns
t_{DVQV2}	Delay from Input or I/O to Outputs On (Enable)	Infinite	50		25		3035	ns
t_{DVC1H}	Input or I/O Setup Time to OCLK	300	50	25		30		ns
t_{C1HDX}	Input or I/O Hold Time after OCLK	300	50	−5		−5		ns
t_{C1HQV}	OCLK to Output Valid Delay	300	50		15		17.5	ns
Period 1	OCLK Cycle Time (t_{DVC1H} + t_{C1HQV})	300	50	40		47.5		ns
t_{DVD1V}	Input or I/O Setup Time to Sumterm CLK	300	50	7.5		8		ns
t_{D1VDX}	Input or I/O Hold Time after Sumterm CLK	300	50		12.5		15	ns
t_{D1VQV}	Sumterm CLK to Output Delay	300	50		35		40	ns
Period 2	STCLK Cycle Time (t_{DVD1V} + t_{D1VQV})	300	50	42.5		48.5		ns
t_{DVC2H}	Input or I/O Setup Time to ICLK	300	50	2.5		3.5		ns
t_{C2HDX}	Input or I/O Hold Time after ICLK	300	50		5		6	ns
t_{C2HQV}	Delay from ICLK to Asynchronous Output Valid	300	50		35		40	ns
t_{C2HC1H}	Register Setup Time after ICLK	300	50	30		35		ns
t_{DVC2L}	Input or I/O Setup Time to Latch	300	50	2.5		3.5		ns
t_{C2LDX}	Input or I/O Hold Time after Latch	300	50		5		6	ns
tRESET	Input, I/O or Feedback to Reset				40		45	ns

Note 1: T = Time D = Data Q = Output Z = Hi-Z V = Valid H = High L = Low X = Change C1 = OCLK C2 = ICLK D1 = Sumterm Clock Input

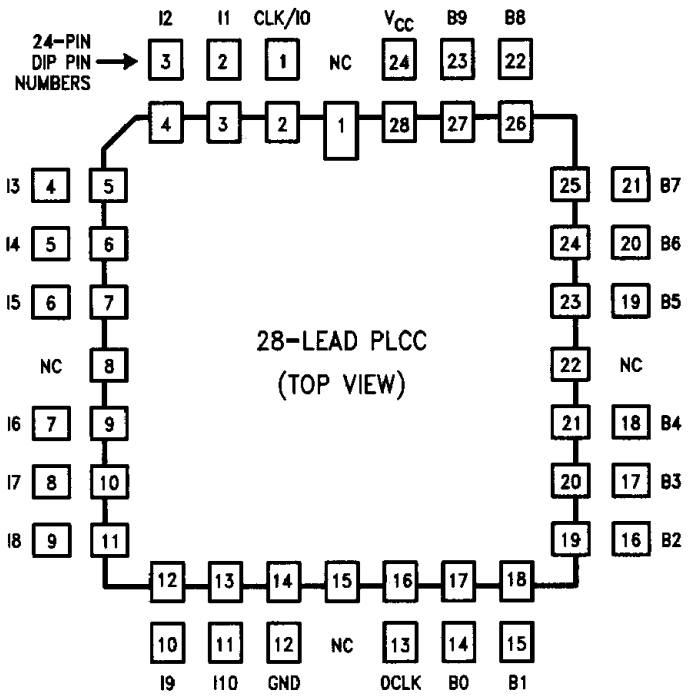
Differential Product Term (DPT) Switching Characteristics

The number of DPT that may switch in the same direction at the same time is limited to a maximum of 15.

The number of DPT for a given design is calculated by subtracting the total number of Product-Terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5 ns period.

$$DPT = (\text{P-Terms})_{LH}\text{-}(\text{P-Terms})_{HL}$$

28-Lead PLCC Connection Diagram



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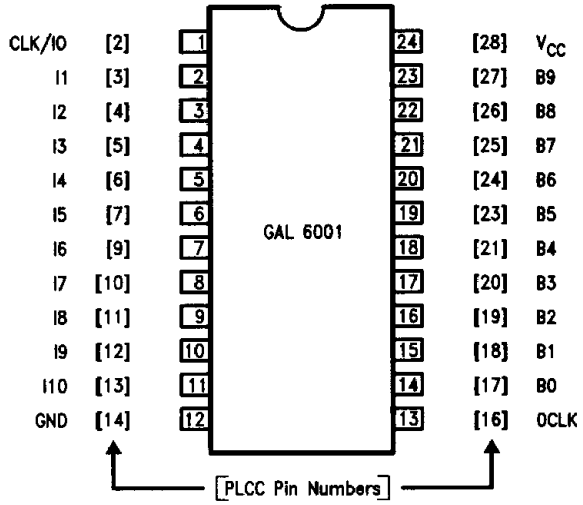
GAL6001 Block Diagram—DIP Connections



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Input Logic MacroCell (ILMC) and I/O Logic MacroCell (IOLMC)

The GAL6001 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2–11) and the IOLMC to the I/O pins (14–23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells (transparent when high) and as a clock for registered macrocells (positive edge triggered).

Configurable input blocks can be used to advantage by system designers. Registered inputs are popular for synchronization and data merging. Transparent latches are useful when the input data is invalid outside a known time window. Direct inputs are used in systems where the input data is well ordered in time. With the GAL6001, external registers and latches are not necessary.

The various configurations of the input and I/O macrocells are controlled by programming four architecture control bits (INLATCH, INSYN, IOLATCH, and IOSYN) within the 68-bit architecture control word. The SYN bits determine whether the macrocells will have register/latch capability or will be strictly asynchronous. The LATCH bits select between latched and registered inputs.

The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages. The truth table associated with each diagram shows the values of the LATCH and SYN bits required to set the macrocell to the configuration shown.

Output Logic MacroCell (OLMC) and State Logic MacroCell (SLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the State Logic MacroCells (SLMC), as they are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic MacroCells (OLMC).

Like the ILMC and IOLMC discussed above, output and state logic macrocells are configured by programming specific bits in the architecture control word (CKS(i), OUTSYN(i), XORD(i), XORE(i)), but unlike the input macrocells which must be configured in blocks, these macrocells are configurable on a macrocell-by-macrocell basis. Throughout this datasheet, i = [14 . . . 23] for OLMCs and i = [0 . . . 7] for SLMCs.

State and Output Logic MacroCells may be set to one of three valid configurations: combinational, D-type registered with sum term (asynchronous) clock, or D/E-type registered. Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selectable through the XORD(i) architecture bits. Polarity selection is not necessary for SLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all "E" sum terms is selectable through the XORE(i) architecture control bits.

When CKS(i) = 1 and OUTSYN(i) = 0, macrocell "i" is set as "D/E-type registered". In this configuration, the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with state hold functions.

When CKS(i) = 0 and OUTSYN(i) = 0, macrocell "i" is set as "D-type registered with sum term clock". In this configuration, the register is enabled and its "E" sum term is routed directly to the clock input. This allows for the popular "asynchronous programmable clock" feature, selectable on a register-by-register basis.

When CKS(i) = 0 and OUTSYN(i) = 1, macrocell "i" is set as "combinatorial". Configuring a SLMC in this manner turns it into a complement array. Complement arrays are used to construct multi-level logic.

Registers in both the Output and State Logic MacroCells feature a RESET input. This active high input allows the registers to be simultaneously and asynchronously reset from a common signal. The source of this signal is the RESET product term. Registers reset to a logic zero, but since the output buffers invert, a logic one will be present at the device pins.

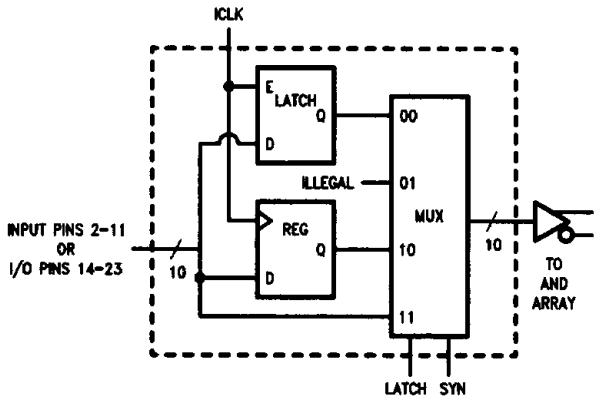
There are two possible feedback paths from each OLMC: one from before the output buffer (this is the normal path) and one from after the output buffer, through the IOLMCs. The second path is usable as a feedback only when the associated bi-directional pin is being used as an output; during input operations it becomes the input data path, turning the associated OLMC into an additional buried state macrocell.

The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register construct can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK- or T-register.

The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages. The truth table associated with each diagram shows the bit value of CKS(i) and OUTSYN(i) required to set the macrocell to the configuration shown.

ILMC/IOLMC Configurations

ILMC/IOLMC Generic Block Diagram



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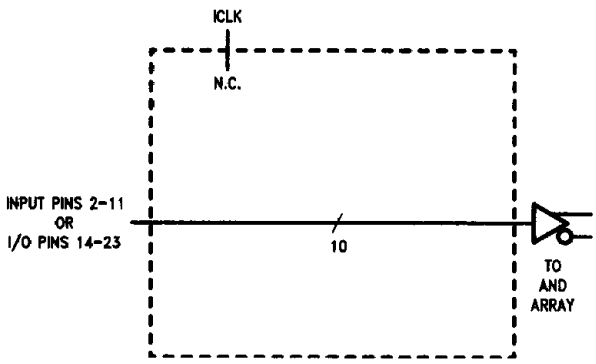
Asynchronous Input



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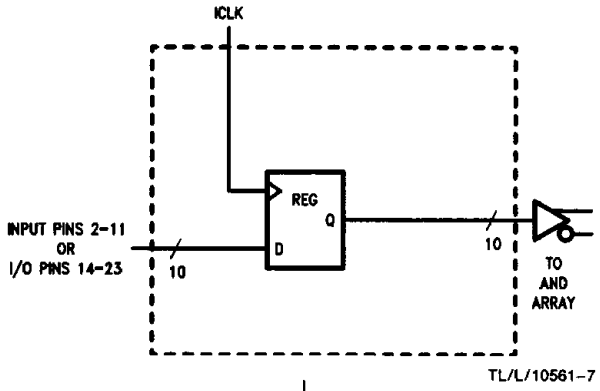
LATCH	SYN
1	1

Registered Input



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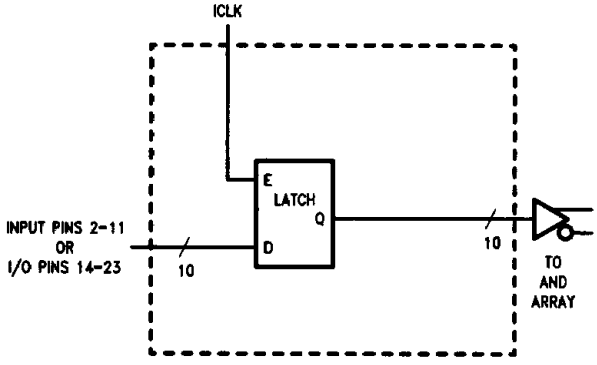
LATCH	SYN
1	0

Latched Input



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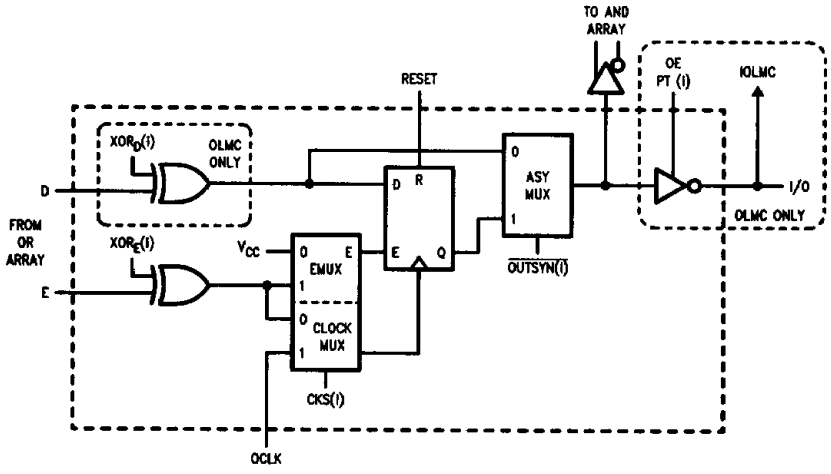
LATCH	SYN
0	0

OLMC/SLMC Configurations

OLMC/SLMC Block Diagram



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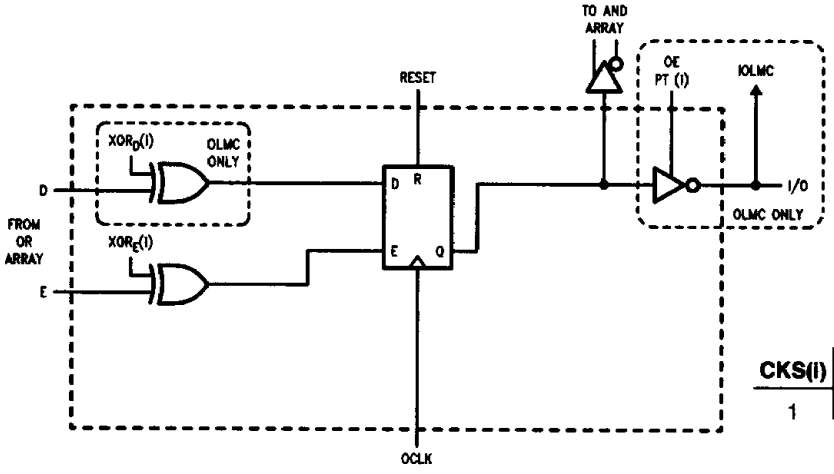
D/E Type Registered



CKS(I)	OUTSYN(I)
1	0

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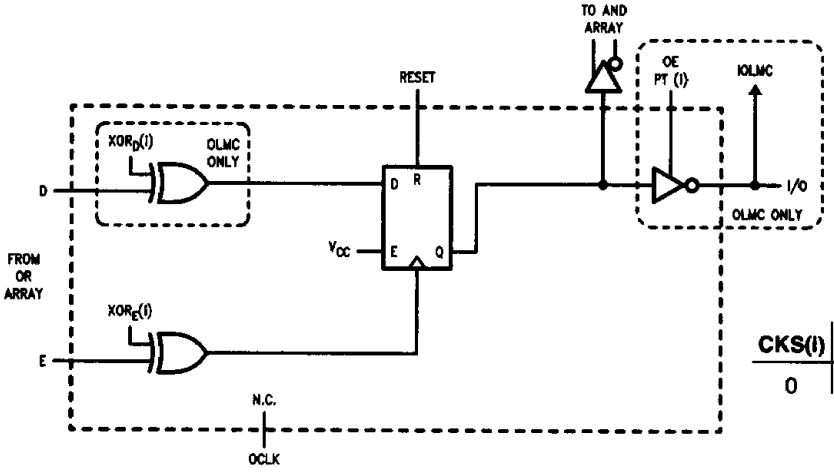
D-Type Registered with Sum Term Asynchronous Clock



CKS(I)	OUTSYN(I)
0	0

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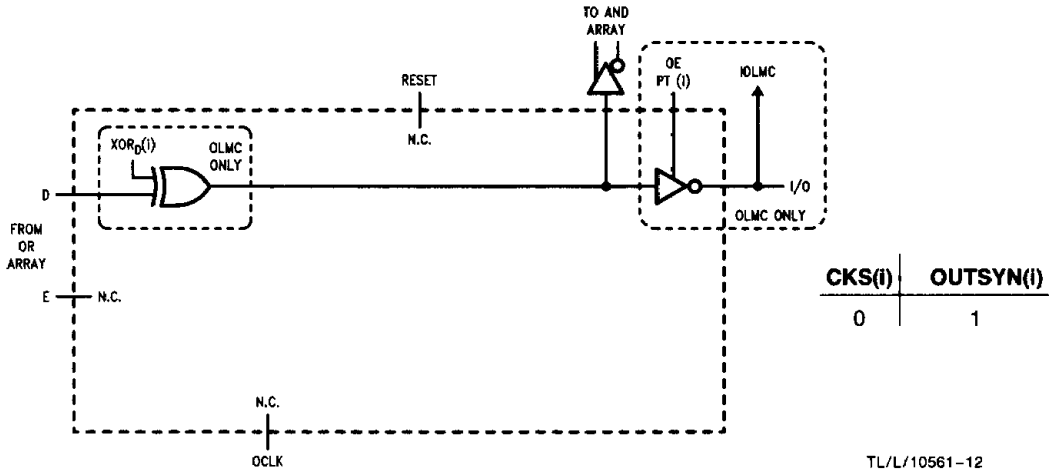
OLMC/SLMC Configurations (Continued)

Combinatorial



CKS(i)	OUTSYN(i)
0	1

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Array Description

The GAL6001 E^2 reprogrammable array is subdivided into three smaller arrays: AND, OR and Architecture. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 input terms by 75 product term outputs. The 20 input and I/O logic macrocells, 8 SLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise a total of 39 inputs to this array (each available in true and complemented forms). Product terms 0–63 serve as inputs to the OR array. Product term 64 is the RESET PT; it generates the RESET signal described in the earlier discussion of output and state logic macrocells. Product terms 65–74 are the output enable product terms; they control the output buffers, thus enabling device pins 14–23 to be bi-direction or TRI-STATE®.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. Product terms 0–63 of the AND array serve as the inputs to this array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 SLMCs, one "D" term and one "E" term to each.

ARCHITECTURE ARRAY

The various configurations of the GAL6001 are enabled by programming cells within the architecture control word. This 68-bit word contains all of the chip configuration data. This data includes: XORD(i), XORE(i), CKS(i), OUTSYN(i), INLATCH, INSYN, IOLATCH, and IOSYN. The function of each of these bits has been previously explained.

Electronic Signature Word

Every GAL6001 device contains an electronic signature word. The Electronic Signature word is a 72-bit user definable storage area, which can be used to store inventory control data, pattern revision numbers, manufacture date, etc. Signature data is always available to the user, regardless of the state of the security cell.

Security Cell

A security cell is provided with every GAL6001 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND, OR and architecture arrays. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. Electronic Signature data is always available to the user, regardless of the state of this control cell.

Bulk Erase

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 ms.

Register Preload

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal machine operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6001 can be preloaded, including the input, I/O, and state registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

Input Buffers

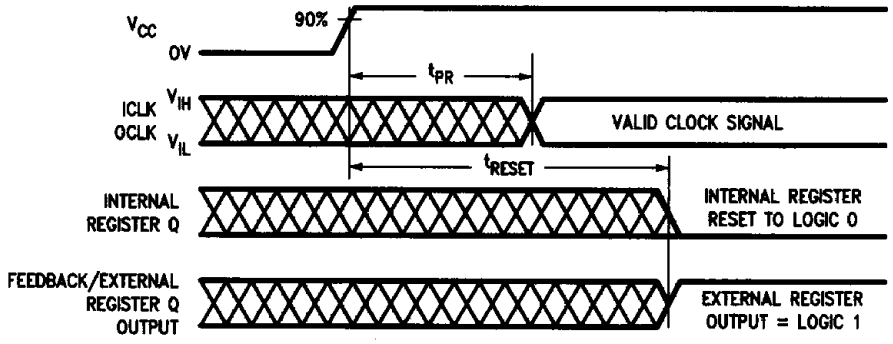
GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than "traditional bipolar devices". This allows for a greater fan out from the driving logic.

GAL devices do not possess active pull-ups within their input structures. As a result, National recommends that all unused inputs and TRI-STATE I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Power-Up Reset

Circuitry within the GAL6001 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tRESET). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, the following conditions must be met to guarantee a valid power-up reset of the GAL6001. First, the V_{CC} rise must be monotonic. Second, the clock inputs must become a proper TTL level within the specified time (tPR). The registers will reset within a maximum of tRESET time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.



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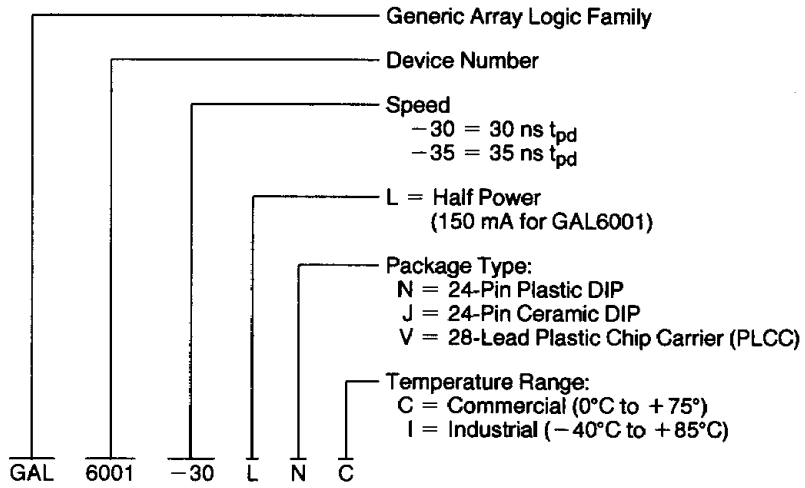
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



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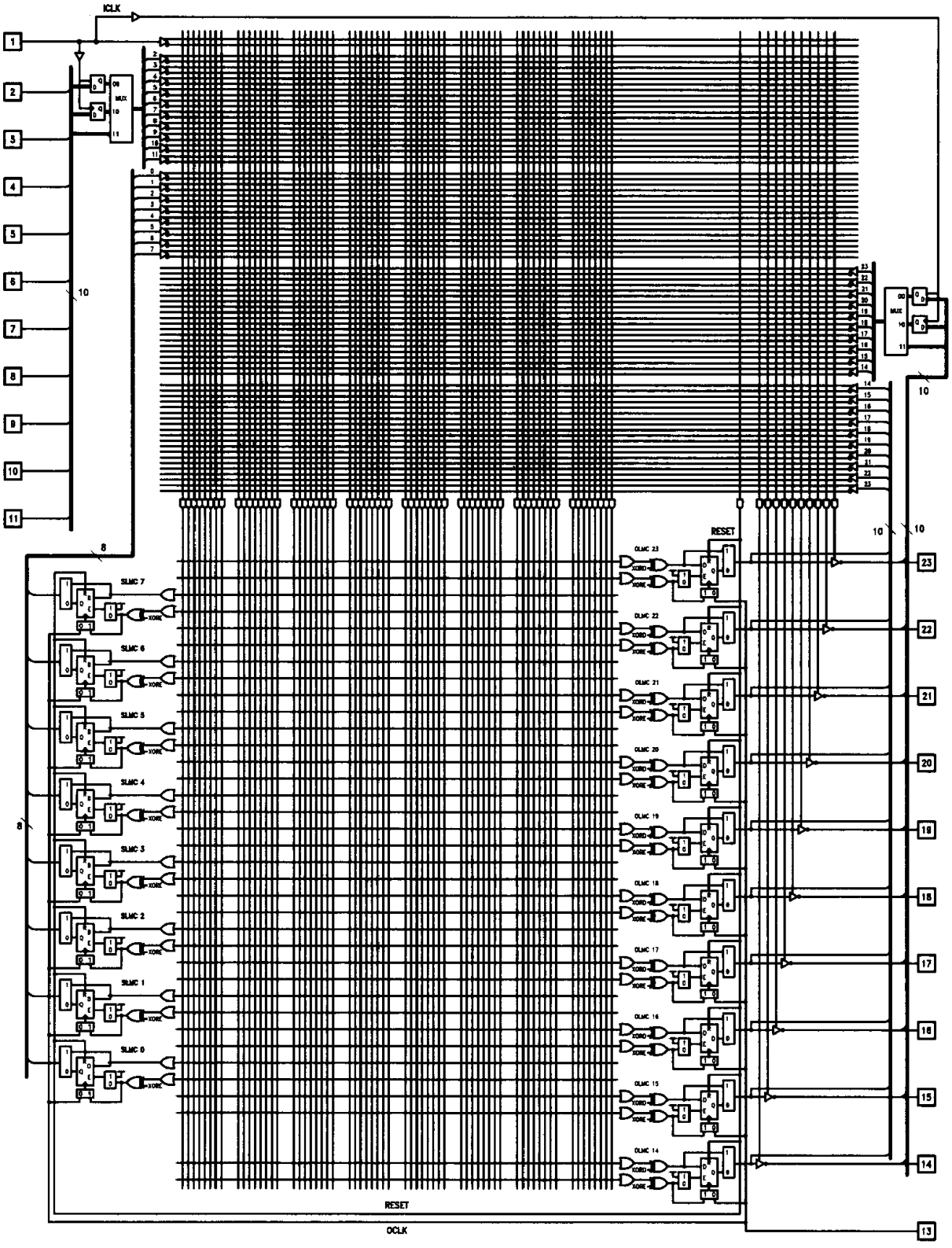
GAL6001 Logic Diagram



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