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MuxIt™ Evaluation Module (EVM)

User's Guide

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Preface

Read This First

About This Manual

This manual describes the MuxIt™ Evaluation Module (MuxIt™ EVM) and introduces the reader to the MuxIt™ concept, components, and theory of operation. It also describes the EVM serializer and deserializer circuit boards and provides instructions on their use.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1—Introduction
- ❏ Chapter 2—EVM Hardware Contents
- ❏ Chapter 3—Test Equipment
- ❏ Chapter 4—Operation
- ❏ Chapter 5—System Design Issues
- ❏ Appendix A—Bill of Materials and Schematics

Related Documentation From Texas Instruments

The following documents describe the MuxIt™ and related support tools. To obtain a copy of any of these TI documents call the Texas Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

1) *The Muxit™ Data Transmission System Applications, Examples, And Design Guidelines (LVDS),* Literature No. SLLA093
2) *Interface Circuits For TIA/EIA–644 (LVDS)* Literature No. SLLA038
3) *Low Voltage Differential Signaling (LVDS) Evaluation Module (EVM)* Literature No. SLLA033A
4) *Low-Voltage Differential Signaling (LVDS) Design Notes* Literature No. SLLA014A

5) *LVD Devices Operate With Vcc = 2.5–Vdc* Literature No. SLLA046

6) *LVDS In Harsh Environments With The Next Generation Receivers From TI* Literature No. SLLA061

7) *LVDS Multidrop Connections* Literature No. SLLA054

8) *Measuring Crosstalk In LVDS Systems* Literature No. SLLA064

9) *Performance Of LVDS With Different Cables* Literature No. SLLA053

10) *Slew Rate Control Of LVDS Circuits* Literature No. SLLA034A

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Chapter 1

Introduction

This chapter provides a basic introduction to MuxIt™ and the EVM.

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1.1 What is MuxIt? 1-2

1.1 What is MuxIt?

MuxIt is a family of general-purpose building blocks designed to serialize and deserialize parallel data. This family includes three types of devices supporting simplex communications: A PLL frequency multiplier (SN65LVDS150), a serializer-transmitter (SN65LVDS151), and a receiver-deserializer (SN65LVDS152).

The key feature of MuxIt is that it is general-purpose, providing flexibility while maintaining throughput capability. The MuxIt EVM demonstrates this flexibility by allowing the user to select and evaluate different operating modes, bandwidths, and interconnecting configurations. The MuxIt EVM also allows the user to become familiar with the MuxIt devices, to understand how they operate, and to understand how to design a serializer/deserializer (serdes) interface using them. Design guidelines for a MuxIt interface are also provided in SLLA093, *The Muxit Data Transmission System Applications, Examples, And Design Guidelines*.

The MuxIt operations are referred to as basic, cascade, and parallel. This EVM is designed so that the three different operations may be readily tested. The basic operation is used when the input data into a single serializer-transmitter has a bit width between 4 and 10. This operation utilizes an LVDS link, comprised of two LVDS pairs, for communication between the serializer and the deserializer. One LVDS pair is the clock and the other pair is the serialized data. Like the basic operation, the cascade operation uses an LVDS link made up of only two LVDS pairs. The cascade capability of MuxIt allows wider parallel data to be transmitted across the LVDS link. Larger width input data that has a higher throughput requirement can be serialized using multiple LVDS data pairs in parallel to transmit data. The parallel input data is equally divided between available serializers. In this parallel operation, the LVDS link consists of multiple LVDS data pairs along with the single LVDS clock pair.

Chapter 2

EVM Hardware Contents

This chapter describes the EVM hardware. The MuxIt EVM kit allows system designers to become familiar with the operation and features of MuxIt quickly and easily. This kit consists of the following items:

- ❑ Serializer board with jumpers
- ❑ Deserializer board with jumpers
- ❑ Adapter header

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2.1 Serializer Board

The serializer board (P/N 6422795A) uses three SN65LVDS151 MuxIt serializer-transmitter devices (U2–U4) and an SN65LVDS150 phase-locked loop (PLL) frequency multiplier (U1) to convert parallel single-ended inputs to a serialized LVDS link containing one or two data pairs and a clock pair. The serializer board will be referred to as A1 and the deserializer board will be referred to as A2 throughout this document to identify jumper, connector, test point, and device references with the appropriate board. A block diagram and photograph of the serializer board is provided in Figures 2–1 and 2–2.

2.1.1 Clock and Data Input Signals

The clock reference into the serializer board can be either single-ended (LVTTL) or differential (LVDS). The inputs A1:J3 and A1:J4 are terminated (50 ohms) for a differential input, but a single-ended input can be applied to A1:J3 when A1:JMP-1 is installed. This jumper connects the VT signal out of the PLL (pin 4 of A1:U1) to the CRI– input (pin 3 of A1:U1), biasing the unused A1:J4 input to VCC/2. Note that the VT signal cannot drive a 50 Ω load, so when providing a single-ended input with jumper A1:JMP-1 installed, resistor R2 must be removed to maintain the Vcc/2 reference level.

The EVM also includes thirty jumper shorts that can be installed on the serializer board data input pins (connectors A1:P1–P3) if the user wants to apply static inputs (fixed logic 1 or 0). Each input connector is a 3×10 header. The center pins of each connector are connected to the input pins of a SN65LVDS151 serializer-transmitter. A1:P1 is connected to A1:U2, A1:P2 is connected to A1:U3, and A1:P3 is connected to A1:U4. The row of pins near the center of the board is connected to VCC, and the row nearest the edge of the board is connected to GND. These connections are marked on the boards.

In addition to static inputs, external devices can also drive the data inputs. When a 5 V device supplies TTL inputs, a 5-V bias ($V_{CC)}$ needs to be provided to the serializer board at Test Point 2 (A1:TP-2) and the jumper short at A1:JMP-5 moved to the External VCC5 position.

2.1.2 Output Signals

The output signals generated by the serializer board are LVDS pairs: LCO± (link clock output), CASCADE_DO± (cascade data output), and SERIAL_DO± (serial data output). Both LCO and CASCADE_DO are outputs of A1:U3 and SERIAL_DO is output from A1:U4.

2.1.3 Power Supply

The standard method for providing power to the boards is via J1 (the compression terminal) located at the top of each board. 3.3 Vdc is applied to the red terminal (labeled VCC) and GND is applied to the black terminal (labeled GND). When the two boards are connected using the 12-pin adapter header, the boards can be powered using a single 3.3-Vdc supply. The power can be applied to J1 on just one board, either serializer or deserializer, and the

other can be remotely powered through the J2 connector. The GND connection between the two boards can be established by installing A1:JMP-11 and A2:JMP-3 on the deserializer. The VCC connection between the two can be established by installing A1:JMP-12 and A2:JMP-2 on the deserializer. These jumpers can also be used when V_{CC} and GND are provided through a cable instead of the adapter header, and the serializer and deserializer boards are located several meters away from each other. These jumpers must be removed when powering the serializer and deserializer boards from separate power supplies. The following table shows the serializer board jumper configurations.

Table 2–1. Serializer Board Jumpers

Jumper Number	Jumper Type	As Shipped	Description
A1:JMP–1	One position	Installed	This jumper can be used when a single–ended clock is input to the SN65LVDS150 PLL, A1:U1, or removed when a differential clock is input.
A1:JMP–2	Two position	VCC	Enables the A1:U1, SN65LVDS150 PLL. VCC = Enabled; GND = Disabled.
A1:JMP–3	Two position	VCC	Enables the link clock reference output of the A1:U1. VCC = Enabled; GND = Disabled.
A1:JMP–4	Two position	VCC	Enables the A1:U2, SN65LVDS151 serializer-transmitter. VCC = Enabled; GND = Disabled.
A1:JMP–5	Two position	ExtVCC5	Input bias for all three SN65LVDS151 data inputs. ExtVCC5 = voltage level on Test Point 2 (A1:TP2); VCC = Power Plane of board.
A1:JMP–6	Two position	VCC	Enables the A1:U3, SN65LVDS151 serializer-transmitter. VCC = Enabled; GND = Disabled.
A1:JMP–7	Two position	VCC	Enables the link clock output of the A1:U3. VCC = Enabled; GND = Disabled.
A1:JMP–8	Two position	VCC	Enables the A1:U4, SN65LVDS151 serializer-transmitter. VCC = Enabled; GND = Disabled.
A1:JMP–11	One position	Installed	When installed, remote ground, A1:J2 pin 2, is connected to the serializer board GND plane.
A1:JMP–12	One position	Installed	When installed, remote VCC, A1:J2 pin 1, is connected to the serializer board VCC plane.

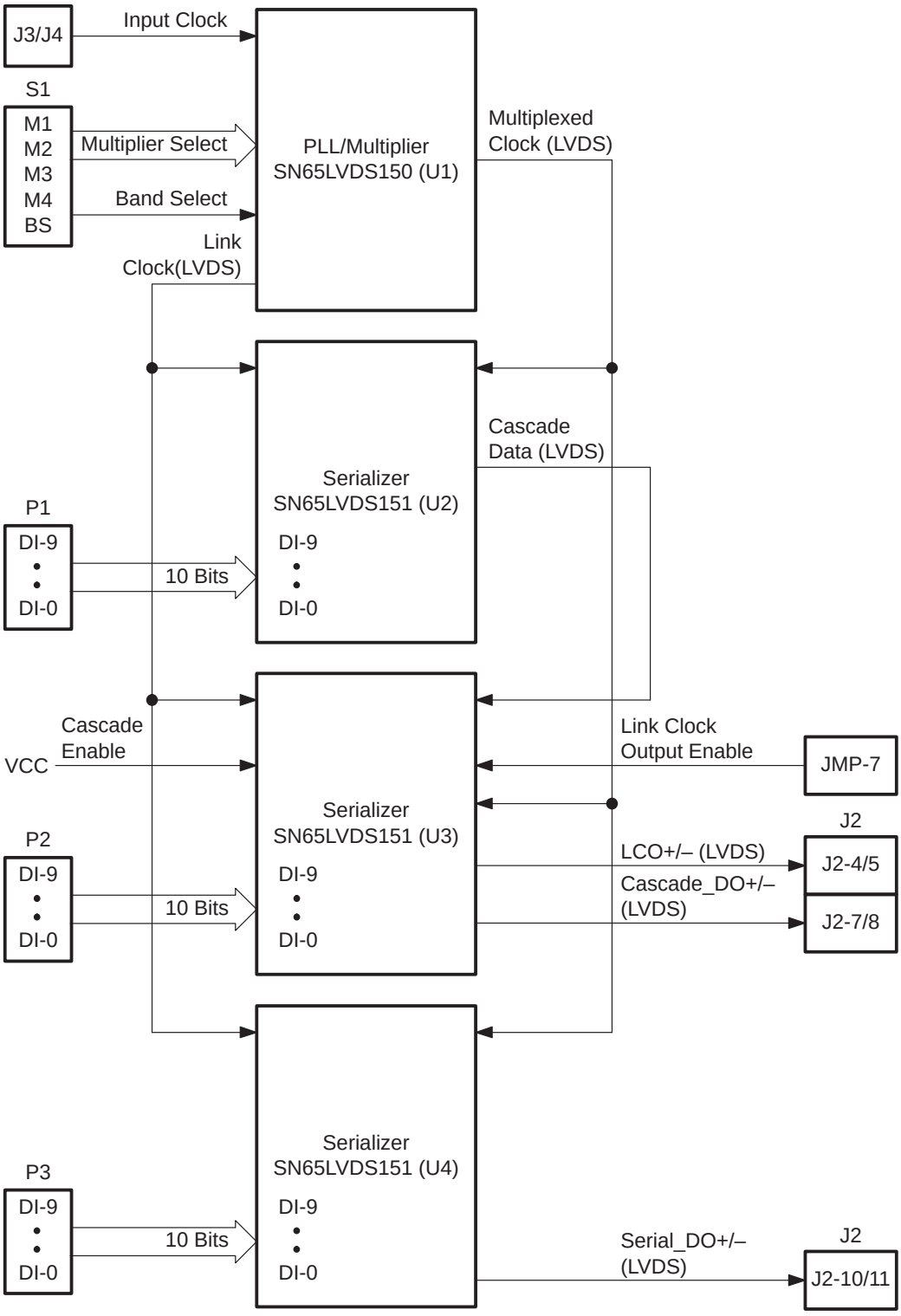
2.1.4 Operations Supported by the Serializer Board

The basic operation is supported by A1:U3. The inputs are parallel data on A1:P2 and clock on A1:J3 and A1:J4. A1:J3 and A1:J4 are the clock inputs used for each operation. The differential outputs of A1:U3 are on A1:J2 pins 4–5 and 7–8, the clock and data respectively.

For cascaded operation, parallel data from A1:P1 and A1:P2 are input to A1:U2 and A1:U3. The data is output on the same clock and data lines as in the basic operation, A1:J2 pins 4–5 and pins 7–8, respectively.

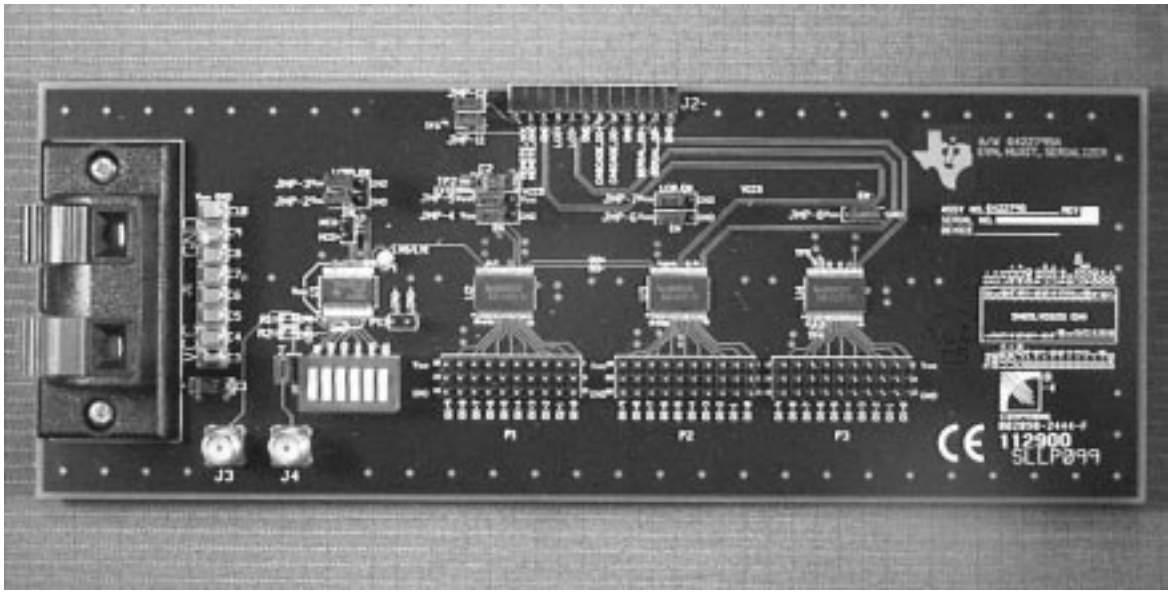
Parallel operation is achieved with inputs A1:P2 and A1:P3 to devices A1:U3 and A1:U4. The output LVDS links are A1:J2 pins 4–5 for the clock, pins 7–8 for data, and pins 10–11 also for data.

Figure 2–1. Serializer Board Simplified Block Diagram



Board layer art, bill of materials and a schematic diagram for the serializer board are shown in Appendix A.

Figure 2–2. Serializer Board



2.2 Deserializer Board

The deserializer board (P/N 6422796A) uses three SN65LVDS152 receiver-deserializers (A2:U2–U4) and a SN65LVDS150 PLL frequency multiplier (A2:U1) to accept the serialized data and clock signals and convert this serialized data stream back to the original parallel single-ended outputs. A block diagram and photograph of the deserializer board is provided in Figures 2–3 and 2–4, respectively.

2.2.1 Clock and Data Input Signals

The input signals are all LVDS. They are the same three output signals from the Serializer: LCI+/LCI–, CASCADE_DI+/CASCADE_DI–, and SERIAL_DI+/SERIAL_DI–. LCI is input into A2:U1, CASCADE_DI is input into A2:U2, and SERIAL_DI is input into A2:U4.

2.2.2 Output Signals

The data and clock output signals provided on connectors A2:P1 through A2:P3 are LVTTL signals. The output clock signal is provided on DCO of A2:P1, A2:P2, and A2:P3 and any of the three can be used. Each output connector is a 2x10 header. The side closest to the components is connected to a resistor in series with the outputs of the SN65LVDS152 devices. The side of the connector closest to the edge of the board is connected to GND.

2.2.3 Power Supply

The following table shows the deserializer board jumper configurations. Refer to section 2.1.3 for power supply information.

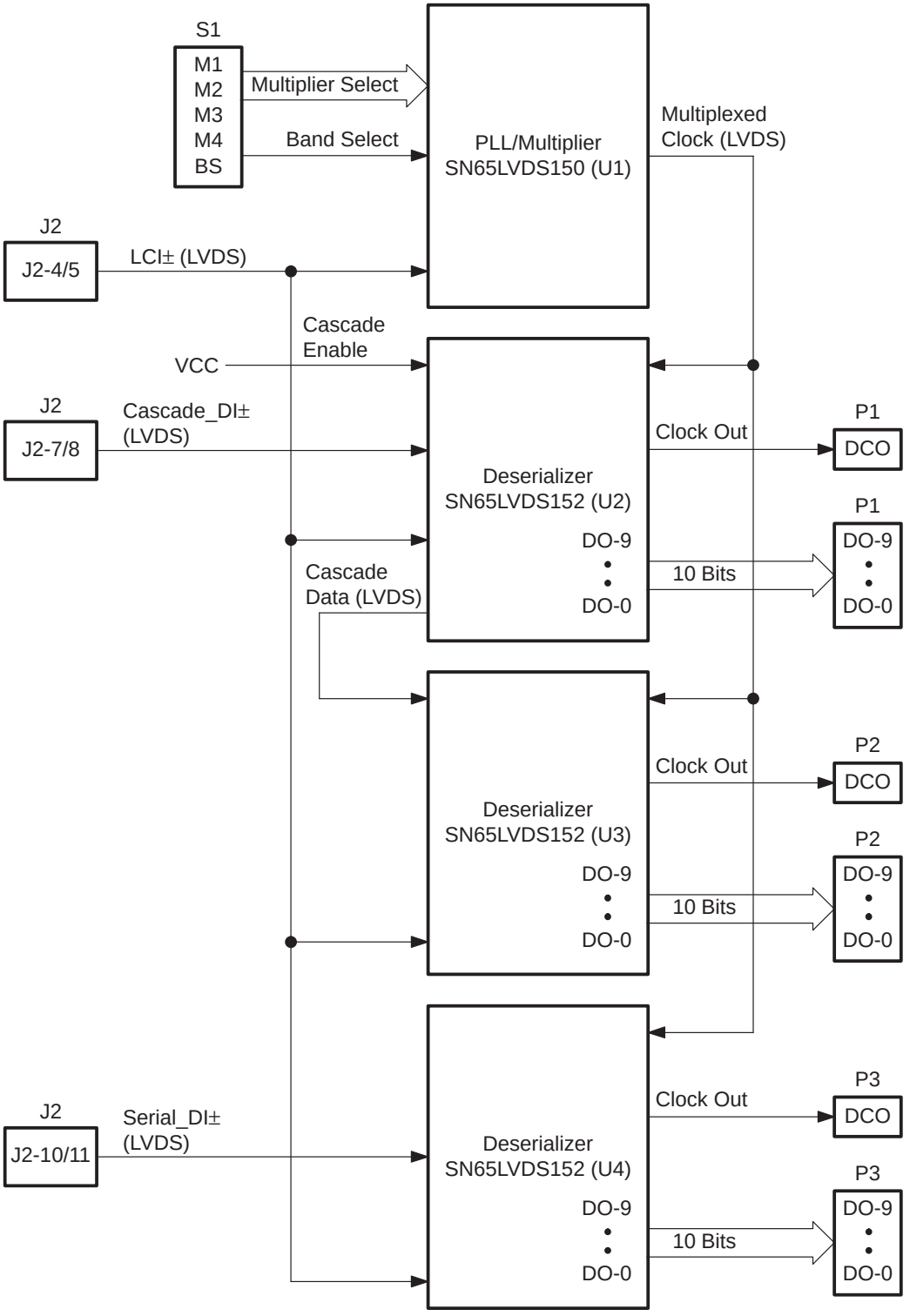
Table 2–2. Deserializer Board Jumpers

Jumper Number	Jumper Type	As Shipped	Description
A2:JMP–2	One position	Installed	When installed Remote VCC, A2:J2 pin 1, is connected to the deserializer board VCC plane.
A2:JMP–3	One position	Installed	When installed remote ground, A2:J2 pin 2, is connected to the deserializer board GND plane.
A2:JMP–4	Two position	VCC	Enables the A2:U1. VCC = Enabled; GND = Disabled.
A2:JMP–5	Two position	GND	Enables the link clock reference output of the A2:U1. VCC = Enabled; GND = Disabled.
A2:JMP–6	Two position	VCC	Enables the SN65LVDS152 receiver-deserializer, A2:U2, cascaded output. VCC = Enabled; GND = Disabled.
A2:JMP–7	Two position	VCC	Enables the A2:U2. VCC = Enabled; GND = Disabled.
A2:JMP–8	Two position	VCC	Enables the SN65LVDS152 receiver-deserializer, A2:U3. VCC = Enabled; GND = Disabled.
A2:JMP–9	Two position	VCC	Enables the SN65LVDS152 receiver-deserializer, A2:U4. VCC = Enabled; GND = Disabled.

2.2.4 Operations Supported by the Deserializer Board

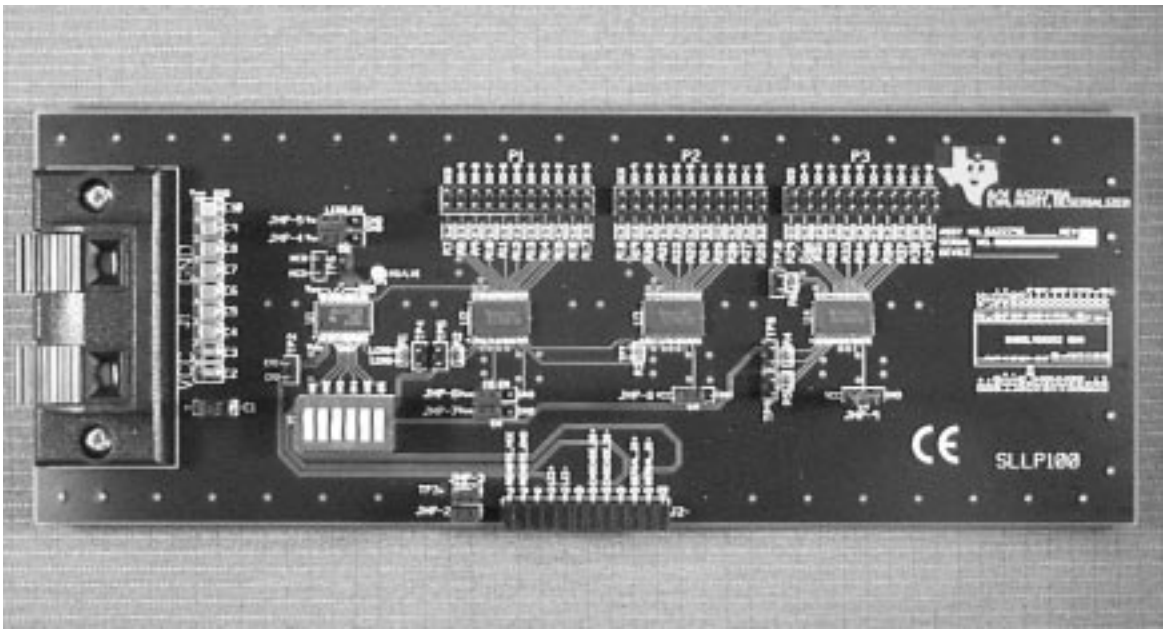
As was done with the serializer board, two SN65LVDS152 receiver-deserializer devices are used in the cascade operation (A2:U2 and A2:U3), two for parallel operation (A2:U2 and A2:U4), and one (A2:U2) is used for basic.

Figure 2–3. Deserializer Board Simplified Block Diagram



Board layer art, bill of materials and a schematic diagram for the deserializer board are shown in Appendix A.

Figure 2–4. Deserializer Board



2.3 Adapter Header

Two connectors are included, one on each board, so the user can use his own interconnect to evaluate and predict performance. The user can connect the two boards using any suitable cable of their choice, such as UTP CAT-5, or the two boards may be connected directly using the adapter header provided.

Chapter 3

Test Equipment

This chapter describes the test equipment used with the MuxIt EVM.

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3.3	Cables	3-2

3.1 Pattern Generator

A signal or pattern generator can provide a clock reference input signal to the serializer board.

Twenty simultaneous inputs are required to fully exercise the cascade inputs, so a pattern generator with 20 parallel outputs and a clock rate range up to 50 MHz is suggested. The Tektronix HFS–9009 series of pattern generators, or equivalent, can be used to provide the inputs signals. The inputs to the serializer board are not terminated with 50-Ω resistors, therefore the lead length and output impedance of the source must be accounted for when driving these inputs.

3.2 Oscilloscope and Scope Probes

The signaling rates and LVDS signal transitions are very fast (transitions less than 1 nsec). To adequately monitor these signals the oscilloscope must have a minimum bandwidth of 1 GHz. The probes need to have similar bandwidth to prevent measurement errors. The Tektronix 784C oscilloscope with P6243 or P6245 single-ended, and P6247 differential probes, or equivalent are suggested.

3.3 Cables

No cables are provided with the MuxIt EVM kit. The adapter header can be used as a connector or can be removed to evaluate system performance of a variety of cable types and lengths. Signal integrity between the serializer and the deserializer boards is dependent upon both the cable type and length. Any standard EIA-568A Category 5 (CAT-5) cable is recommended for use. The four twisted pairs contained in a standard CAT-5 cable can be used in place of or in conjunction with the adapter header. Three pairs can be used for the serial data, cascade data, and link clock signals. The fourth pair may be used for VCC and GND when powering one of the boards remotely from a single power supply. The cable selected should have a characteristic impedance of 110 Ω ±20% as recommended in TIA/EIA-644.

Chapter 4

Operation

This chapter describes the operation of the MuxIt EVM.

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4.1 Before Operating the EVM

Before operating the MuxIt EVM the user should become familiar with the schematics, data sheets, and *The MuxIt Data Transmission System Applications, Examples, and Design Guidelines* (SLLA093). The user should locate each connector, test point, and jumper on each board and on each schematic. Tables 2-1 and 2-2 show the *as-shipped* configuration of the jumpers on each board. The user should notice the position of the rocker switches on the S1 switch for both the serializer and deserializer. The rocker switch will be set to a multiplier of 20 on both boards as the default.

It is suggested that the EVM users first connect the serializer board and deserializer boards using the adapter header in order to become familiar with the modes of operation. Connect 3.3 Vdc supply to either A1:J1 or A2:J1. The remote power jumpers (A1:JMP-11, A1:JMP-12, A2:JMP-2, A2:JMP-3) should be installed to power both boards. The dc current from the power supply will be less than 200 mA. Apply a single-ended 10 MHz clock reference (CRI+) to A1:J3. Ensure A1:JMP-1 is installed to allow operation using a single-ended clock source.

Before connecting a pattern generator to the A1:P1, A1:P2, or A1:P3 input pins, it is suggested that the provided jumper shorts be installed to create *static* input levels. The jumper shorts can be pushed down onto the A1:P1, A1:P2, or A1:P3 connector pins. The user can install any combination of 1s and 0s on the input and verify that the output pin on the deserializer board is at the same logic level as the corresponding input pin on the serializer board.

After becoming familiar with the basic operation, the user can try different multiplier factors, change the various enable/disable jumpers, apply different input patterns, and change the clock reference frequency and duty cycle. The user can also remove the adapter header and evaluate performance using different cables. The pattern generator can be used to provide dynamic input data into the serializer input connectors, and the deserialize output connectors may be monitored to see that the outputs are correct.

Designers may want to investigate enable/disable response times, and the EVM has been designed to allow easy access and control of these functions. The jumpers for enabling devices are 2-pin 0.100″ headers that can be used to connect test and measurement equipment to the boards in place of the jumper shorts that are provided. Refer to sections 2.1.3 and 2.2.3 for lists of the enable jumpers for the serializer and deserializer boards.

4.2 Basic Operation Using a Single LVDS Data Pair

Basic 10:1 serial operation, shown in Figure 4–1, is set up by setting the multiplier to 10 on both the serializer and deserializer boards. The rockers M1 through M5 of switch S1 control the multiplier factor pins to the PLL on both boards. The BS rocker controls the band select input to the PLL on both boards. As shown in Figure 4–2, the five (5) multiplier pins (M1–M5) are pulled low internally in the PLL device. Therefore, an OPEN position switch for S1 corresponds to a LOW. Closing a rocker switch connects the pin to VCC and creates a HIGH. The opposite is true for the BSEL pin, which is connected to the BS rocker. It is pulled up internally, so the BS rocker in the OPEN position creates a HIGH B_SEL signal. Refer to either SLLA093 or the SN65LVDS150 datasheet for setting the multiplier and band select inputs.

Figure 4–1. Basic 10:1 Serial Operation

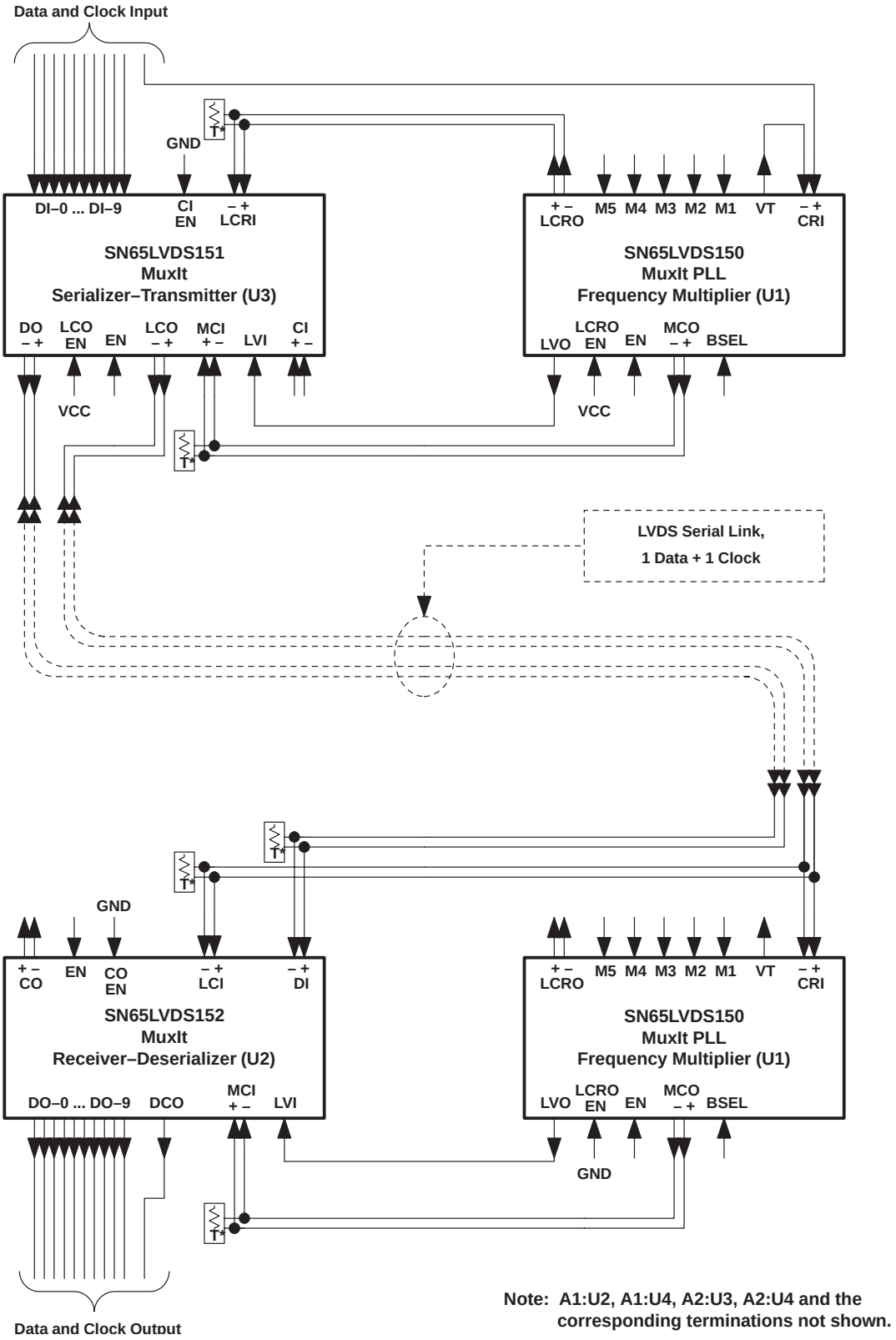
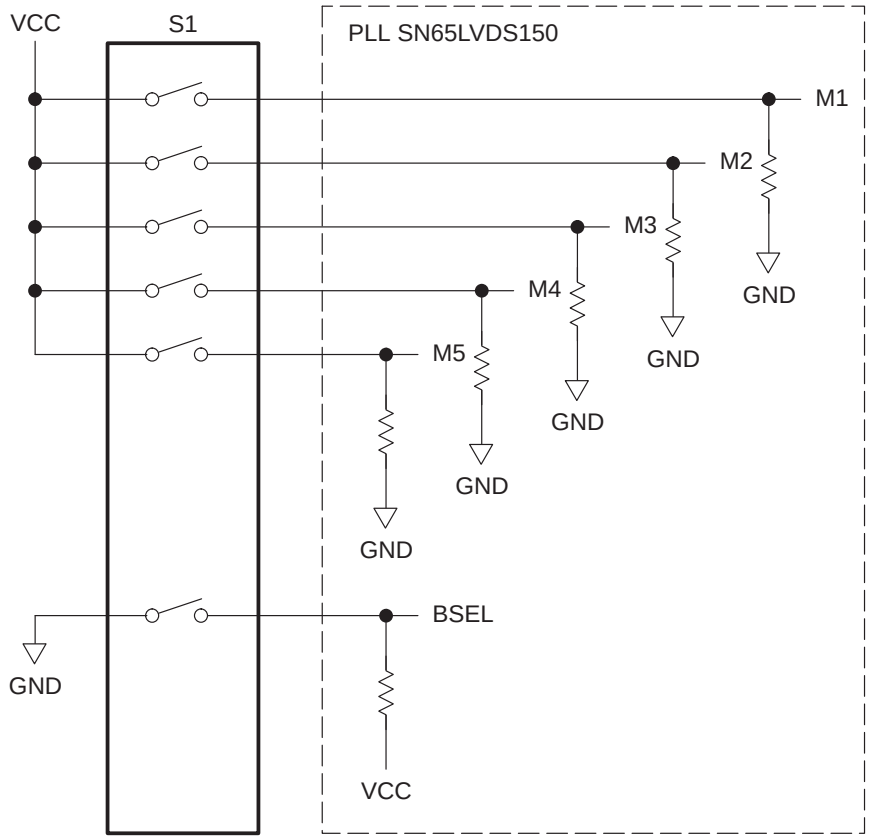


Figure 4–2. Multiplier and Band Select Switch to PLL



Basic serial operation is the simplest of the MuxIt capabilities. For 10:1 serial data, the Clock Reference input can be increased to 1/10th the serial LVDS signaling rate. Assuming a 200Mbps serial LVDS signaling rate between the serializer and deserializer, the input clock reference can be 20 MHz (200 Mbps ÷ 10 bits). Only inputs on A1:P2 are serialized, and the cascaded inputs from A1:U2 are not of concern when using a 10X or less PLL multiplier ratio. The multiplier ratio also prevents data from being cascaded in the deserializer board, and the serial data stream is converted back to parallel data by A2:U2 only. The input-to-output bit mapping is shown in the Table 4–1. Note that inputs into A1:P2 are output on A2:P1.

Table 4–1. Input–to-Output Bit Mapping for 4–10 Bit Serial Operation

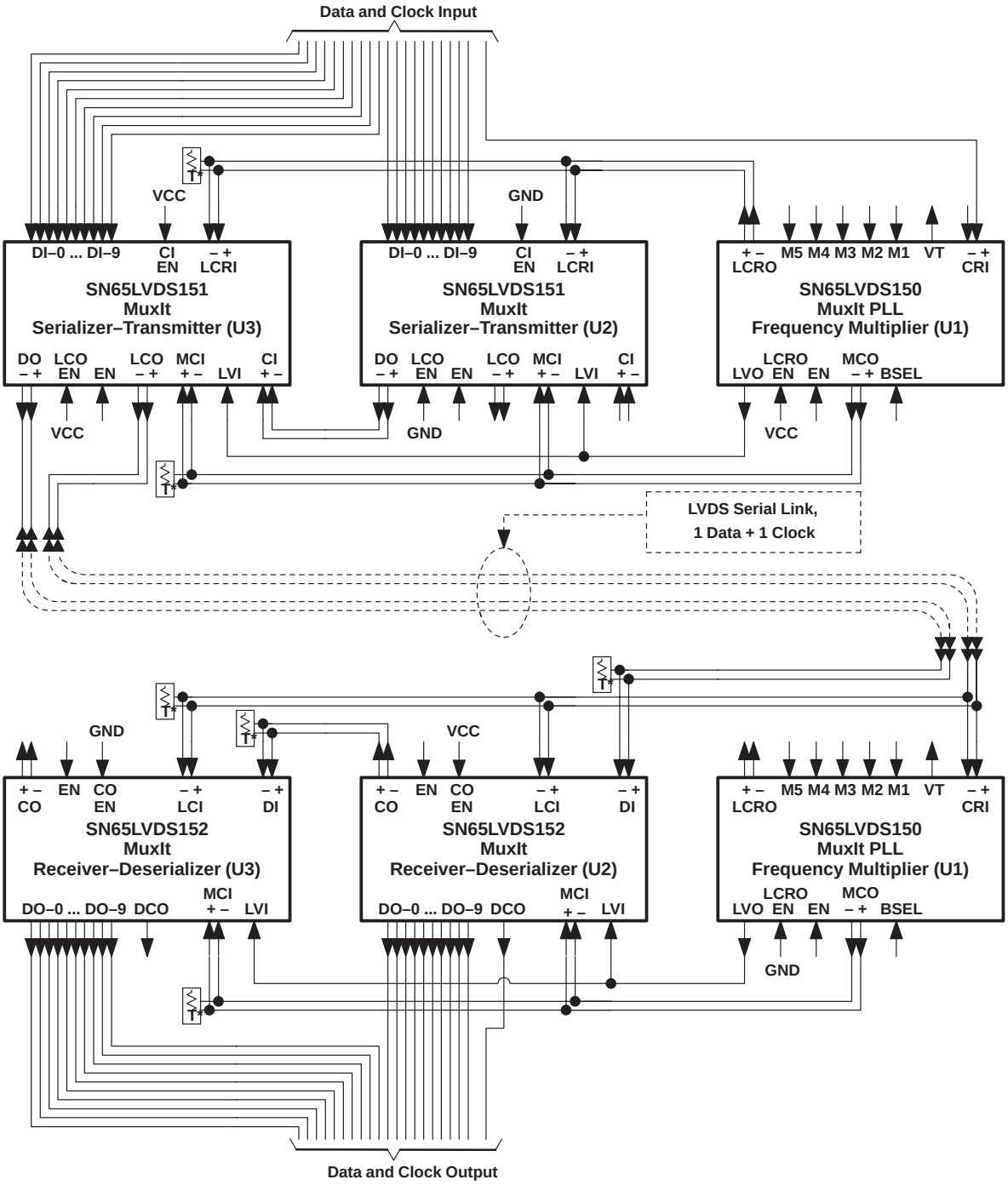
Inputs	Outputs				
	M = 4	**M = 6**	**M = 8**	**M = 9**	**M = 10**
DI–0 (A1:P2)	DO–6 (A2:P1)	DO–4 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)	DO–0 (A2:P1)
DI–1 (A1:P2)	DO–7 (A2:P1)	DO–5 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)
DI–2 (A1:P2)	DO–8 (A2:P1)	DO–6 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)
DI–3 (A1:P2)	DO–9 (A2:P1)	DO–7 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)
DI–4 (A1:P2)	NA	DO–8 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)
DI–5 (A1:P2)	NA	DO–9 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)
DI–6 (A1:P2)	NA	NA	DO–8 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)
DI–7 (A1:P2)	NA	NA	DO–9 (A2:P1)	DO–8 (A2:P1)	DO–7 (A2:P1)
DI–8 (A1:P2)	NA	NA	NA	DO–9 (A2:P1)	DO–8 (A2:P1)
DI–9 (A1:P2)	NA	NA	NA	NA	DO–9 (A2:P1)

EVM users may evaluate this mode of operation using 4, 6, 8, 9 or 10 parallel data bits from the signal generator. The user must select matching PLL multiplier ratios (M), for both the serializer and deserializer boards.

4.3 Cascade Data Operation

The EVM cascade operation can transfer parallel data 12 to 20 bits wide. This operation utilizes the cascade input (CI) between devices A1:U2 and A1:U3, and cascade output (CO) between A2:U2 and A2:U3. The data is transmitted using a single LVDS pair (labeled CASCADE_DO and CASCADE_DI in the EVM kit). The link is illustrated in Figure 4–3. The user needs to select a matching PLL multiplier ratio (M) between 12 and 20 on both the serializer and deserializer boards. Assuming a 200Mbps serial LVDS signaling rate, input clock reference rates from 5 MHz to 10 MHz for M = 20, and 5 MHz to 16.7 MHz for M = 12 can be used.

Figure 4–3. Cascade Mode Operation for 12- to 20-Parallel Bits



NOTE: U4 and terminations for both boards are not shown

Notice that 12<=M<=20, where M = Multiplex/Multiplier ratio set by M1 through M5 using the S1 rocker switches. Input-to-output bit mapping for 12 to 20-bit cascade mode is shown in Table 4–2.

Table 4–2. Input-to-Output Bit Mapping for 12- to 20-Bit Cascade Mode

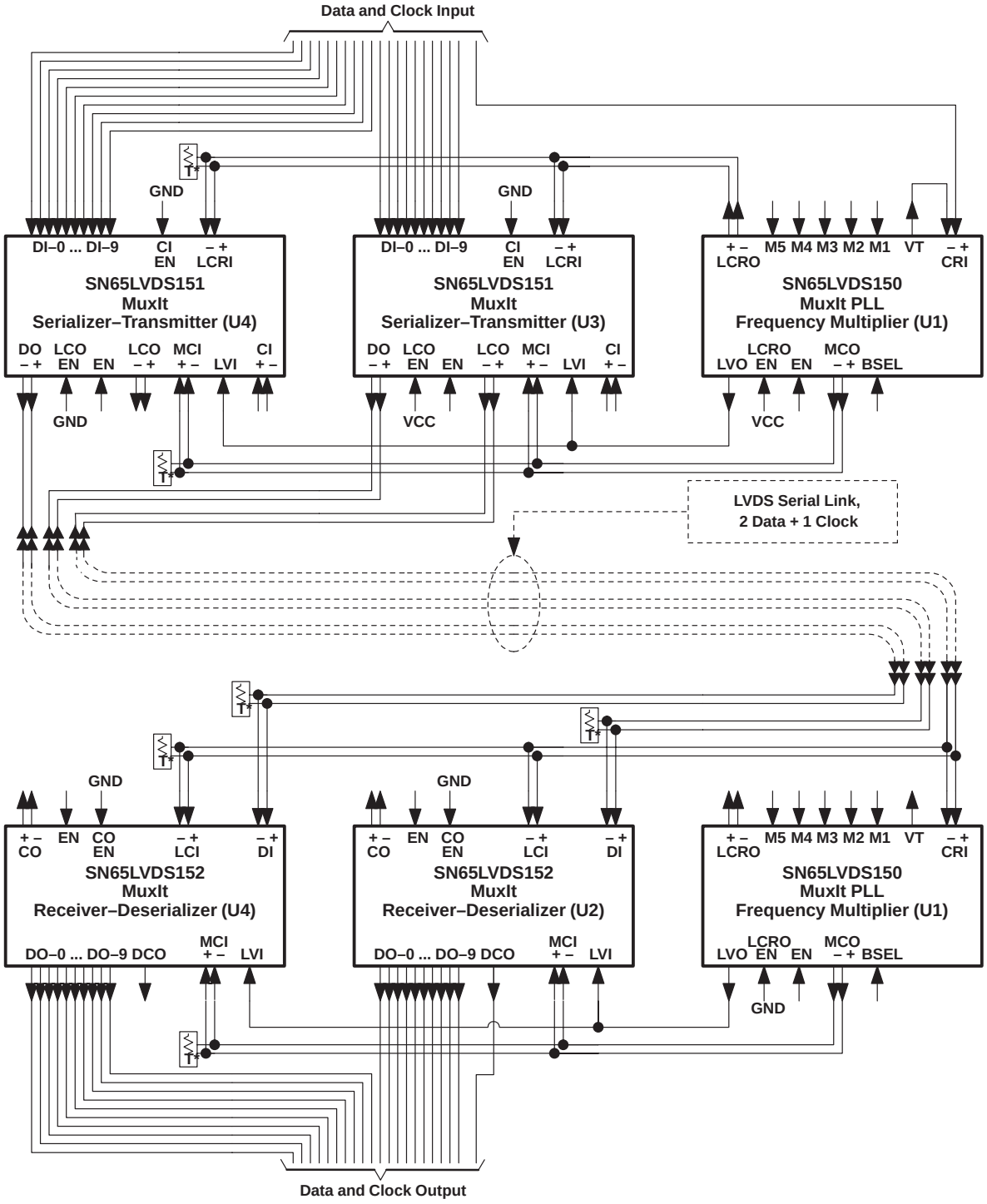
Inputs	Outputs								
	M = 12	**M = 13**	**M = 14**	**M = 15**	**M = 16**	**M = 17**	**M = 18**	**M = 19**	**M = 20**
DI–0 (A1:P2)	DO–8 (A2:P2)	DO–7 (A2:P2)	DO–6 (A2:P2)	DO–5 (A2:P2)	DO–4 (A2:P2)	DO–3 (A2:P2)	DO–2 (A2:P2)	DO–1 (A2:P2)	DO–0 (A2:P2)
DI–1 (A1:P2)	DO–9 (A2:P2)	DO–8 (A2:P2)	DO–7 (A2:P2)	DO–6 (A2:P2)	DO–5 (A2:P2)	DO–4 (A2:P2)	DO–3 (A2:P2)	DO–2 (A2:P2)	DO–1 (A2:P2)
DI–2 (A1:P2)	DO–0 (A2:P1)	DO–9 (A2:P2)	DO–8 (A2:P2)	DO–7 (A2:P2)	DO–6 (A2:P2)	DO–5 (A2:P2)	DO–4 (A2:P2)	DO–3 (A2:P2)	DO–2 (A2:P2)
DI–3 (A1:P2)	DO–1 (A2:P1)	DO–0 (A2:P1)	DO–9 (A2:P2)	DO–8 (A2:P2)	DO–7 (A2:P2)	DO–6 (A2:P2)	DO–5 (A2:P2)	DO–4 (A2:P2)	DO–3 (A2:P2)
DI–4 (A1:P2)	DO–2 (A2:P1)	DO–1 (A2:P1)	DO–0 (A2:P1)	DO–9 (A2:P2)	DO–8 (P2)	DO–7 (A2:P2)	DO–6 (A2:P2)	DO–5 (A2:P2)	DO–4 (A2:P2)
DI–5 (A1:P2)	DO–3 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)	DO–0 (A2:P1)	DO–9 (A2:P2)	DO–8 (A2:P2)	DO–7 (A2:P2)	DO–6 (A2:P2)	DO–5 (A2:P2)
DI–6 (A1:P2)	DO–4 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)	DO–0 (A2:P1)	DO–9 (A2:P2)	DO–8 (A2:P2)	DO–7 (A2:P2)	DO–6 (A2:P2)
DI–7 (A1:P2)	DO–5 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)	DO–0 (A2:P1)	DO–9 (A2:P2)	DO–8 (A2:P2)	DO–7 (A2:P2)
DI–8 (A1:P2)	DO–6 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)	DO–0 (A2:P1)	DO–9 (A2:P2)	DO–8 (A2:P2)
DI–9 (A1:P2)	DO–7 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)	DO–0 (A2:P1)	DO–9 (A2:P2)
DI–0 (A1:P1)	DO–8 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)	DO–0 (A2:P1)
DI–1 (A1:P1)	DO–9 (A2:P1)	DO–8 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)
DI–2 (A1:P1)	NA	DO–9 (A2:P1)	DO–8 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)
DI–3 (A1:P1)	NA	NA	DO–9 (A2:P1)	DO–8 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)
DI–4 (A1:P1)	NA	NA	NA	DO–9 (A2:P1)	DO–8 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)
DI–5 (A1:P1)	NA	NA	NA	NA	DO–9 (A2:P1)	DO–8 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)
DI–6 (A1:P1)	NA	NA	NA	NA	NA	DO–9 (A2:P1)	DO–8 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)
DI–7 (A1:P1)	NA	NA	NA	NA	NA	NA	DO–9 (A2:P1)	DO–8 (A2:P1)	DO–7 (A2:P1)
DI–8 (A1:P1)	NA	NA	NA	NA	NA	NA	NA	DO–9 (A2:P1)	DO–8 (A2:P1)
DI–9 (A1:P1)	NA	NA	NA	NA	NA	NA	NA	NA	DO–9 (A2:P1)

Although not supported by this EVM, up to 40 LVTTL parallel inputs can be serialized down to two pair of LVDS lines. This topology would require four SN65LVDS151 serializer-transmitters and four SN65LVDS152 deserializer-receivers. One pair of the LVDS lines is used to transmit a clock signal and a second LVDS pair transmits the data. It also means that 40 wires, connector pins, or back plane signal traces can be reduced from 40 down to 4.

4.4 Parallel Operation Using Two LVDS Data Pairs

As mentioned earlier, one of the key features of MuxIt is its flexibility in terms of the different operations that can be supported. This parallel operation illustrates how to send 20 bits of data over two LVDS data pairs as opposed to the single data pair in the cascade operation. The user can apply up to 20 bits of data on A1:P2 and A1:P3 (corresponding to the inputs A1:U3 and A1:U4). The output data (all 20 bits) will appear at the A2:P1 and A2:P3 connector (corresponding to the outputs from A2:U2 and A2:U4). The EVM parallel operation is illustrated in Figure 4–4.

Figure 4–4. 8- to 20-Bit Parallel Operation Using Two LVDS Data Lines



NOTE: U2 in the Serializer and U3 in the Deserializer are not shown

The user may notice that when implementing basic operation, the minimum number of parallel bits is four, which corresponds to the lowest PLL clock multiplier ratio. This minimum number is increased by the number of LVDS pairs used in parallel operation. The MuxIt EVM uses two serializer-transmitters and two LVDS pairs, which doubles the minimum number of data bits (four

to eight) and the effective throughput. For example, if 16-bit parallel input data needs to be sampled at 10 MHz, then the data is equally divided between A1:P2 and A1:P3. The clock reference is set to 10 MHz and the PLL multiplier to 8. The result will be each LVDS data pair carrying 8 bits at 80 Mbps. The amount of data transferred across the interface is now twice the signaling rate (2×80 Mbps = 160 Mbps). The user is encouraged to evaluate the throughput capabilities of MuxIt for different signaling rates. The input-to-output bit mapping for the full 20 bits is shown in Table 4–3.

Table 4–3. Input-to-Output Bit Mapping for 8- to 20-Parallel Bits Using Two LVDS Data Lines

Inputs	**Outputs**				
	M = 4	**M = 6**	**M = 8**	**M = 9**	**M = 10**
DI–0 (A1:P2)	DO–6 (A2:P1)	DO–4 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)	DO–0 (A2:P1)
DI–1 (A1:P2)	DO–7 (A2:P1)	DO–5 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)	DO–1 (A2:P1)
DI–2 (A1:P2)	DO–8 (A2:P1)	DO–6 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)	DO–2 (A2:P1)
DI–3 (A1:P2)	DO–9 (A2:P1)	DO–7 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)	DO–3 (A2:P1)
DI–4 (A1:P2)	NA	DO–8 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)	DO–4 (A2:P1)
DI–5 (A1:P2)	NA	DO–9 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)	DO–5 (A2:P1)
DI–6 (A1:P2)	NA	NA	DO–8 (A2:P1)	DO–7 (A2:P1)	DO–6 (A2:P1)
DI–7 (A1:P2)	NA	NA	DO–9 (A2:P1)	DO–8 (A2:P1)	DO–7 (A2:P1)
DI–8 (A1:P2)	NA	NA	NA	DO–9 (A2:P1)	DO–8 (A2:P1)
DI–9 (A1:P2)	NA	NA	NA	NA	DO–9 (A2:P1)
DI–0 (A1:P3)	DO–6 (A2:P3)	DO–4 (A2:P3)	DO–2 (A2:P3)	DO–1 (A2:P3)	DO–0 (A2:P3)
DI–1 (A1:P3)	DO–7 (A2:P3)	DO–5 (A2:P3)	DO–3 (A2:P3)	DO–2 (A2:P3)	DO–1 (A2:P3)
DI–2 (A1:P3)	DO–8 (A2:P3)	DO–6 (A2:P3)	DO–4 (A2:P3)	DO–3 (A2:P3)	DO–2 (A2:P3)
DI–3 (A1:P3)	DO–9 (A2:P3)	DO–7 (A2:P3)	DO–5 (A2:P3)	DO–4 (A2:P3)	DO–3 (A2:P3)
DI–4 (A1:P3)	NA	DO–8 (A2:P3)	DO–6 (A2:P3)	DO–5 (A2:P3)	DO–4 (A2:P3)
DI–5 (A1:P3)	NA	DO–9 (A2:P3)	DO–7 (A2:P3)	DO–6 (A2:P3)	DO–5 (A2:P3)
DI–6 (A1:P3)	NA	NA	DO–8 (A2:P3)	DO–7 (A2:P3)	DO–6 (A2:P3)
DI–7 (A1:P3)	NA	NA	DO–9 (A2:P3)	DO–8 (A2:P3)	DO–7 (A2:P3)
DI–8 (A1:P3)	NA	NA	NA	DO–9 (P3)	DO–8 (A2:P3)
DI–9 (A1:P3)	NA	NA	NA	NA	DO–9 (A2:P3)

Again, this topology can support 8 to 20-bit parallel inputs, which are equally divided between A1:P2 and A1:P3. The user needs to select the same PLL multiplier ratio (M), between 4 and 10 on both boards. A total of three LVDS lines are used; two for data and one for the clock timing reference.

This EVM is not designed for input widths greater than twenty bits. However, MuxIt can transmit forty parallel inputs in the parallel operation if desired. Like cascade operation, this topology would require four serializer-transmitters and four receiver-deserializers. One pair of the LVDS lines is used to transmit a clock signal and four LVDS pairs transmit the data. The transmission media is reduced from 40 lines to 5 LVDS pairs (4 data and 1 clock).

Chapter 5

System Design Issues

This chapter discusses basic design issues and board layout guidelines used in designing the MuxIt EVM boards. These guidelines should be followed to ensure the user is successful in designing their MuxIt interface. The user should also refer to the Application Note SLLA014, *Low Voltage Differential Signaling (LVDS) Design Notes*, for general board layout guidelines.

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5.2 Terminations and Multidrop Configurations 5-6

5.1 PC Board Layout Considerations

The difference in propagation delay of signal interfaces is an important parameter, and the signal interface between the PLL and the serializer or deserializer devices needs to be matched in length and medium. Propagation delays are inevitable, but it is important to maintain a timing relationship between the multiplied clock (MCO, MCI) and the link clock reference (LCRO, LCRI) signals at the source end. Likewise, the timing between MCI and MCO, and link clock (LCI, LCO) at the destination end must be maintained. Without maintaining timing relationships data can be lost. Maintaining a timing relationship at the source end of the EVM means that the propagation delay of the signal path from LCRO on A1:U1 to LCRI on A1:U2 should match the propagation delay of the signal path from the MCO output on A1:U1 to the MCI input on A1:U2. These two propagation delays are identified as $t_{pd(LCR1)}$ and $t_{pd(A1:MC1)}$ respectively, and are illustrated in Figure 5–1. The desired relationship is:

$$t_{pd(LCR1)} = t_{pd(A1:MC1)}$$

A similar propagation delay match should be made at the destination end of the LVDS link to prevent a loss of data. The propagation delay of the link clock signal (LCI) to the LCI input on A2:U2 should be equal to the sum of the propagation delays from the link clock signal to the CRI input on A2:U1 and the propagation delay from the MCO output on A2:U1 to the MCI input on A2:U2. In this case the link clock signal propagation delays are being referenced to the input into the deserializer board before the signals split between A2:U1 and A2:U2, as illustrated in Figure 5–2. The desired relationship is:

$$t_{pd(LCI1)} = t_{pd(A2:MC1)} + t_{pd(CRI)}$$

When multiple devices are being used, the propagation delays should be matched for each input to a device, and the propagation delays for each device should be kept to a minimum. These delays include LCRI and MCI signals at the source; and link clock and MCI signals at the destination. These propagation delays are illustrated in Figures 5–1 and 5–2.

The relationships for the serializer are:

$$t_{pd(LCR1)} = t_{pd(A1:MC1)}$$
$$t_{pd(LCR2)} = t_{pd(A1:MC2)}$$
$$t_{pd(LCR3)} = t_{pd(A1:MC3)}$$

The relationships for the deserializer are:

$$t_{pd(LCI1)} = t_{pd(A2:MC1)} + t_{pd(CRI)}$$
$$t_{pd(LCI2)} = t_{pd(A2:MC2)} + t_{pd(CRI)}$$
$$t_{pd(LCI3)} = t_{pd(A2:MC3)} + t_{pd(CRI)}$$

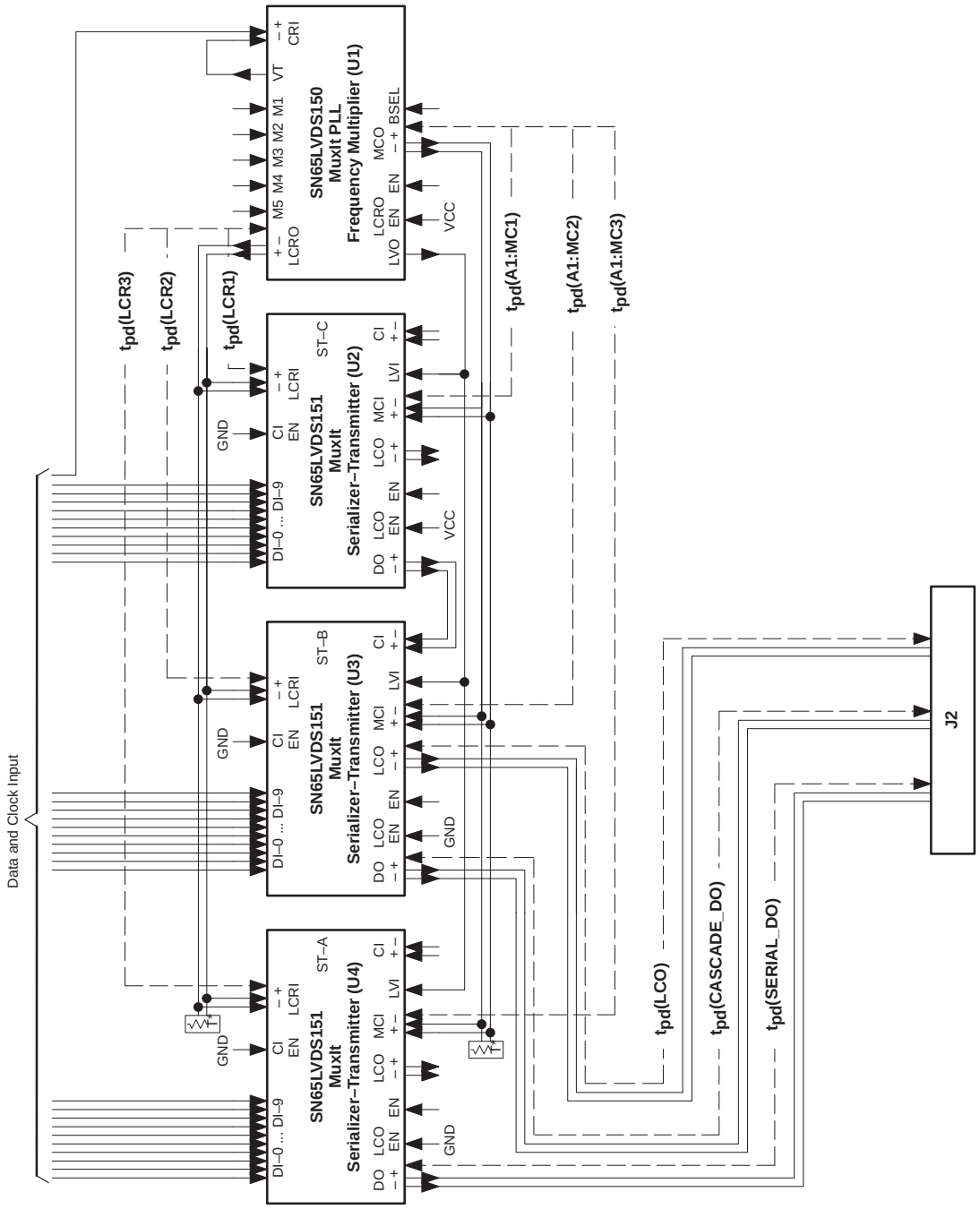


Figure 5–1. Illustrating Signal Delay Matching of the Serializer Board

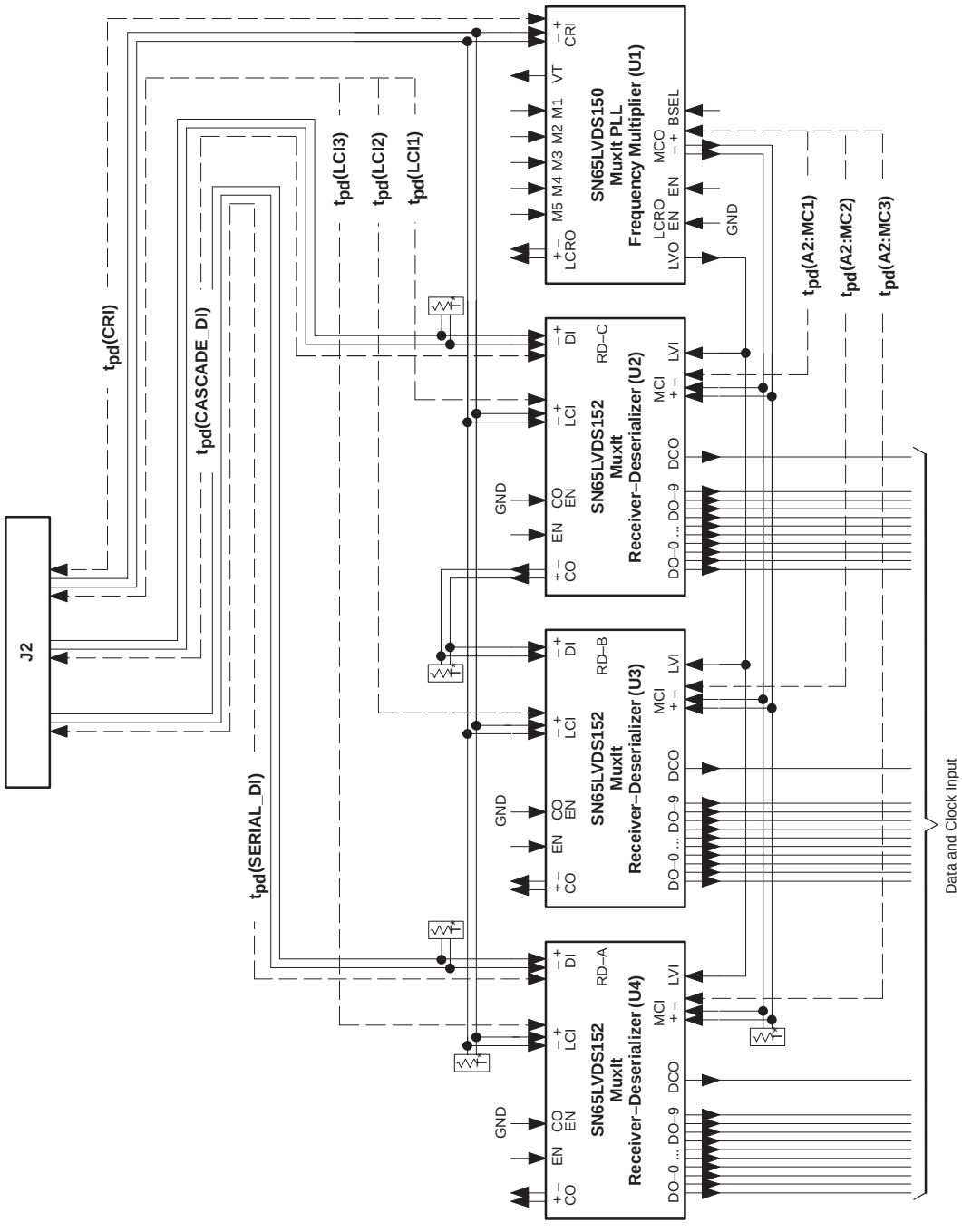


Figure 5–2. Illustrating Signal Delay Matching of the Deserializer Board

Like the clock signals, the propagation delay of data signal interfaces also have to be related. The remaining critical propagation delays for Figure 5–1 are given by:

$$t_{pd(LCO)} = t_{pd(CASCADE\_DO)}$$
$$t_{pd(CASCADE\_DO)} + t_{pd(A1:MC2)} = t_{pd(SERIAL\_DO)} + t_{pd(A1:MC3)}$$

and for Figure 5–2 are given by:

$$t_{pd(CASCADE\_DI)} = t_{pd(LCI1)}$$
$$t_{pd(SERIAL\_DI)} = t_{pd(LCI3)}$$

In addition to trace length matches, the user must also be aware of stubs present on multidrop lines and keep these stub lengths to a minimum. Each line to a multiple drop input from the LVDS link is called a stub and contributes to reflections on the link. Stubs are present in the MuxIt EVM multidrop lines. These lines include the LCRO/LCRI and MCO/MCI lines on the serializer board and CRI/LCI and MCO/MCI lines on the deserializer boards. Both boards provide examples of how to minimize stub lengths. The serializer board uses fly-by routing on the signal layer that distributes these signals, and the vias needed to bring the signals to the top layer and the devices act as the stubs. The deserializer also uses fly-by routing for most of the signal distribution. The exceptions are traces from the A2:U1 LCI, the A2:U4 CRI, and A2:U4 MCI. The traces of A2:U4 are relatively long to the terminations, as compared to similar terminations on the serializer board. All stub lengths are within the acceptable limit of 2 to 3 cm given in application note SLLA014A. In general all signal terminations should be kept close to the input of a device, even in point-to-point signals. The A2:U1 LCI signal is split at A2:TP2 and the resulting stub is the trace running from A2:TP2 to the A2:U1 input. Figures 5–3 and 5–4 show the fly-by routing and the stubs present on the MCO and LCI lines of the serializer and deserializer boards.

Figure 5–3. Serializer Board MCO Trace Routing

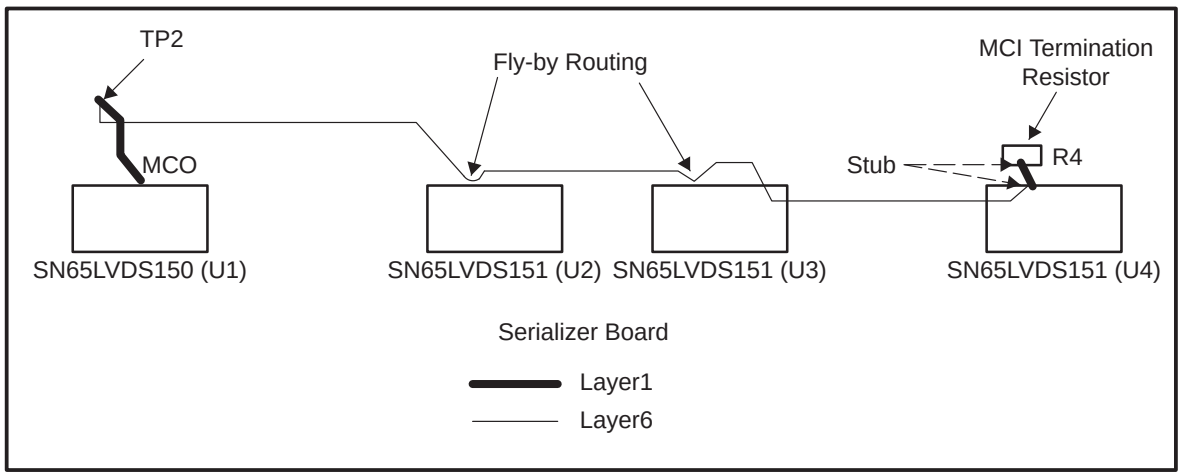
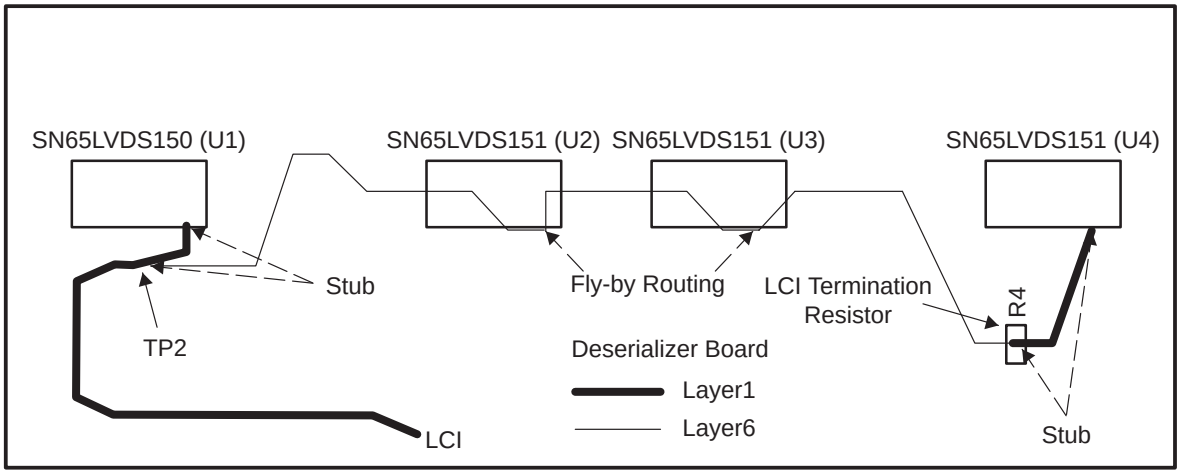


Figure 5–4. Deserializer LCI Trace Routing

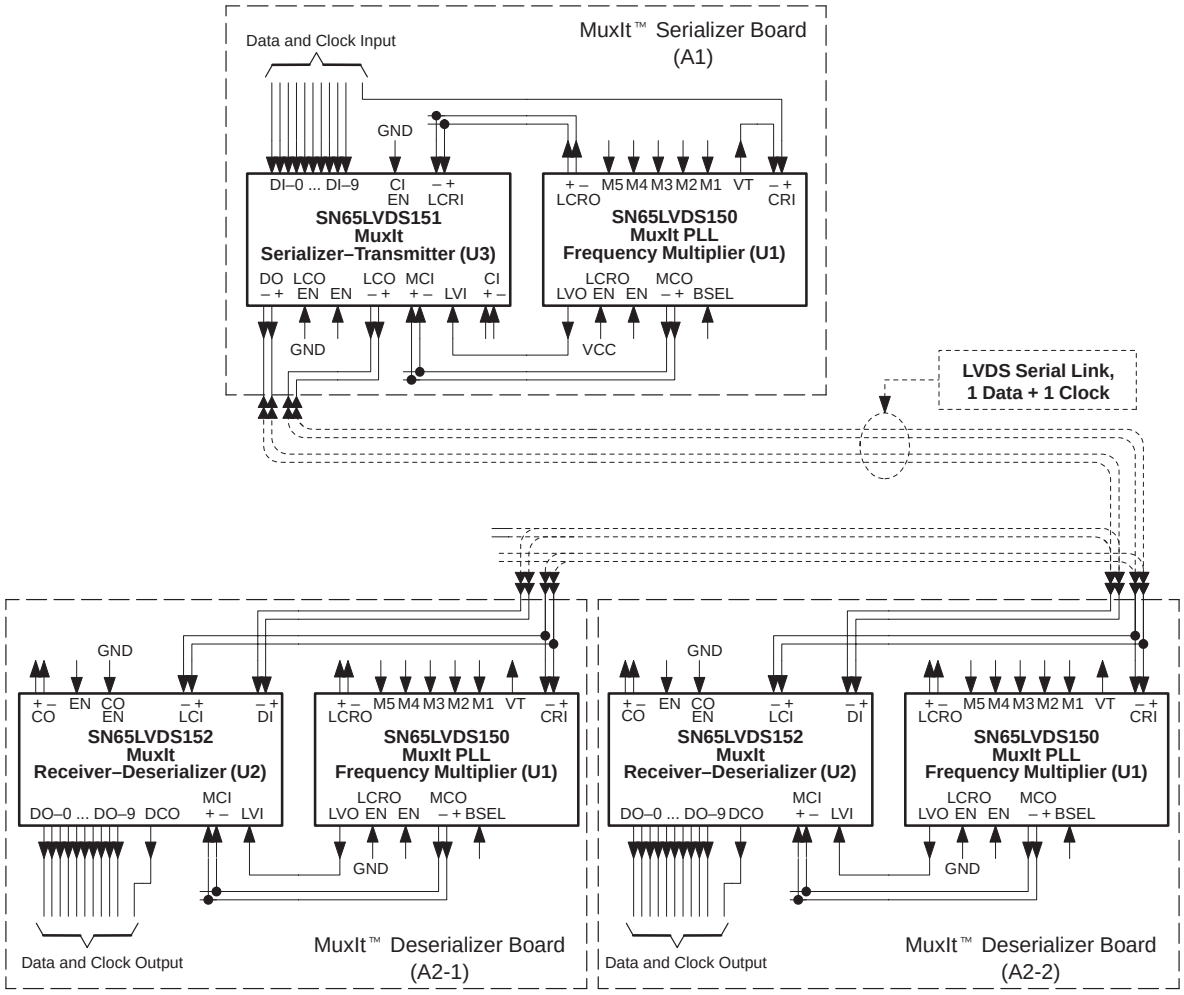


5.2 Terminations and Multidrop Configurations

Designers should notice that an internal termination resistor is provided on the CI input of the SN65LVDS151 serializer-transmitter. All other LVDS inputs are not internally terminated. The reason for this is to allow multiple receivers to be connected in a multidrop configuration. This is illustrated in Figure 5–5.

If a user has more than one MuxIt EVM, then multidrop operation can be evaluated. System designers can use multiple drops of an LVDS link as long as there is only one termination, located at the end of the transmission line. As described earlier, the multiple drops from the LVDS signals are stubs, and these stub lengths need to be kept as short as possible to minimize reflections on the LVDS lines. Using the multiple EVMs in multidrop operation would create stubs that are equivalent to the trace length from the input connector (A2:J2) to the device input. Such stub lengths may impact the evaluation of MuxIt in a multidrop configuration. Also note that one or more of the terminations on the EVMs must be removed so that only one termination exists at the end of each transmission line. In the example depicted in Figure 5–5, the removal of terminations for LCI/CRI and CASCADE_DI (resistors R5 and R1) on A2–2 is recommended.

Figure 5–5. Multidrop Configuration of MuxIt EVMs



Appendix A

PC Board Bill of Material and Schematics

This appendix contains the PC board bill of materials, silkscreen art and board layers, and schematics for the MuxIt EVM.

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A.1	**PC Board Bill of Materials**	**A-2**
A.2	**Board Layers and Silkscreen Art**	**A-4**
A.3	**Schematics**	**A-8**

A.1 PC Board Bill of Materials

Table A–1.Parts Lists for MuxIt EVM Serializer Board

QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATOR	KITTED PART NUMBER
1	BD06	Switch, 6 PST, dip	S1	GRAYHILL P/N 76SB06
1	CES–112–02–T–S–RA	1×12 .1 CTR FEM R/A	J2	
2	CRCW080551R1F	51.1 Ω, 0.1 W, 1%	R1, R2	NEWARK P/N 48F4419
2	CRCW08051000F	100 Ω 0.1 W, 2%	R3, R4	NEWARK P/N 66F9119
1	C3216X7R1C105K	Cap, 1 µF, 16 V, ±10%, X7R	C3	NMC1206Z5U105M16TRPLP3K
1	DUT_TSSOPW_28	SN65LVDS150PW PLL	U1	
3	DUT_TSSOP_DA_32P	SN65LVDS151DA	U2–U4	
7	JUMPER, 3P, 100CC	Jumper, 3P, 100 CC	JMP2 – JMP8	
7	NFSC104J16TRC3	Cap, 0.1 µF, 16 V, ±5%	C4–C10	
14	NMC0603Y5V104Z25TRP	Cap, 0.1 µF, 25 V, 80/–20%, Y5V	C11, C13, C15, C17, C19, C21, C23, C25, C27, C29, C31, C33, C35, C37	
2	NTCT686K10TRC	Cap, 68 µF, 10 V, ±10%	C1, C2	
3	TSW–110–07–T–T	Header, 3×10, 0.1 CTR	P1–P3	SAMTEC
5	103185–2	Male, 2 PIN, 0.100 CC	P13, TP6, JMP1, JMP11, JMP12	
1	15CT200	Compression terminal	J1	
2	901–144–8RFX	SMA RF/Coax connector	J3, J4	AMPHENOL
14	0805YG105ZAT2A	Cap, 1.0 µF, 16V, ±20%	C12, C14, C16, C18, C20, C22, C24, C26, C28, C30, C32, C34, C36, C38	NSPC102J50TRA1
1	5002K–ND	Test point, white	TP1	TP1 = KEYSTONE 5002K–ND (white)
1	5000K–ND	Test point, red	TP2	TP2 = KEYSTONE 5002K–ND (red)
1	5001K–ND	Test point, black	TP3	TP3 = KEYSTONE 5002K–ND (black)
4	SJ5003	Rubber mounting feet	NA	BUMPON (DIV. OF 3M)
42	65474–010	Jumper short, mini	NA	BERG Electronics
1	SLLP099 (6422795)	Printed wiring board	NA	CERPROBE
2	91102–A005	Lock washer, #4	NA	McMASTER–CARR (To Mount S1)
2	90272–A107	#4–40 × 5/16” Screw	NA	McMASTER–CARR (TO MOUNT S1)
2	90760–A005	Nut, #4–40, small pattern	NA	McMASTER–CARR (To Mount S1)

Table A–2. Parts Lists for MuxIt EVM Deserializer Board

QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATOR	KITTED PART NUMBER
1	76SB06	Switch, 6 PST, dip	S1	GRAYHILL
1	CES–112–02–T–S–RA	1×12 .1 CTR FEM R/A	J2	
33	CRCW060351R1F	51.1 Ω, 0.1 W, 1%, 603 PCK	R40–R72	Not installed (Part Not In Kit)
6	CRCW08051000F	100 Ω , 0.1 W, 2%	R1–R6	NEWARK P/N 66F9119
2	C3216X7R1C105K	Cap, 1 µF, 16 V, ±10%, X7R	C2, C3	NMC1206Z5U105M16TRPLP3K
1	DUT_TSSOPW_28	SN65LVDS150PW PLL	U1	
3	DUT_TSSOP_DA_32P	SN65LVDS152DA	U2–U4	
6	JUMPER, 3P, 100CC	Jumper, 3P, 100 CC	JMP4 – JMP9	
7	NFSC104J16TRC3	Cap, 0.1 µF, 16 V, ±5%	C4–C10	
14	NMC0603Y5V104Z16TRP	Cap, 0.1 µF, 16 V, 80/–20%, Y5V	C11, C13, C15, C17, C19, C21, C23, C25, C27, C29, C31, C33, C35, C37	
1	NTCT686K10TRC	Cap, 68 µF, 16 V, ±10%	C1	
33	P29.4HTR–ND	29.4 Ω 0.1w, 1% 0603 PCK	R7–R39	Output Series Resistor
3	TSW–111–08–T–D	Header, 3x10, 0.1 CTR	P1–P3	SAMTEC
10	4–103329–0x2	Male, 2 pin, 0.100 CC	TP2, TP4–6, TP8–10, JMP–2, JMP3	1×2 Header, AMP P/N = 103185–2 00
1	15CT200	Compression terminal	J1	
14	0805ZG105ZAT2A	Cap, 1.0 ∝F, 10 V, ±20%	C12, C14, C16, C18, C20, C22, C24, C26, C28, C30, C32, C34, C36, C38	NSPC102J50TRA1
1	5002K–ND	Test point, white	TP1	TP1 = KEYSTONE 5002K-ND (white)
1	5001K–ND	Test point, black	TP3	TP2 = KEYSTONE 5002K-ND (black)
4	SJ5003	Rubber mounting feet	NA	BUMPON (DIV. OF 3M)
8	65474–010	Jumper short, mini	NA	BERG Electronics
1	SLLP100 (6422796)	Printed wiring board	NA	CERPROBE
2	91102–A005	Lock washer, #4	NA	McMASTER–CARR (To Mount S1)

A.2 Board Layers and Silkscreen Art

Figure A–1. Serializer Layer 1

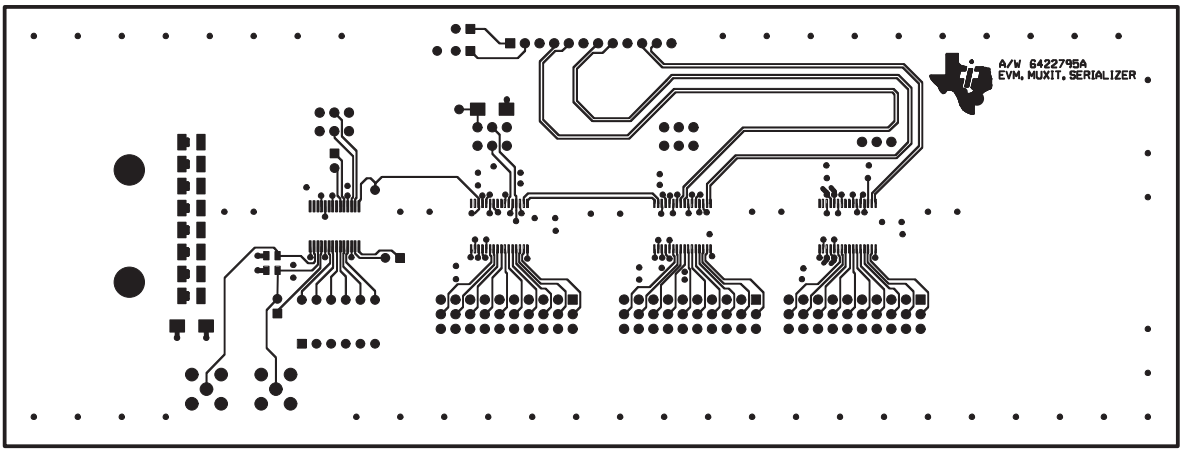


Figure A–2. Serializer Layer 6

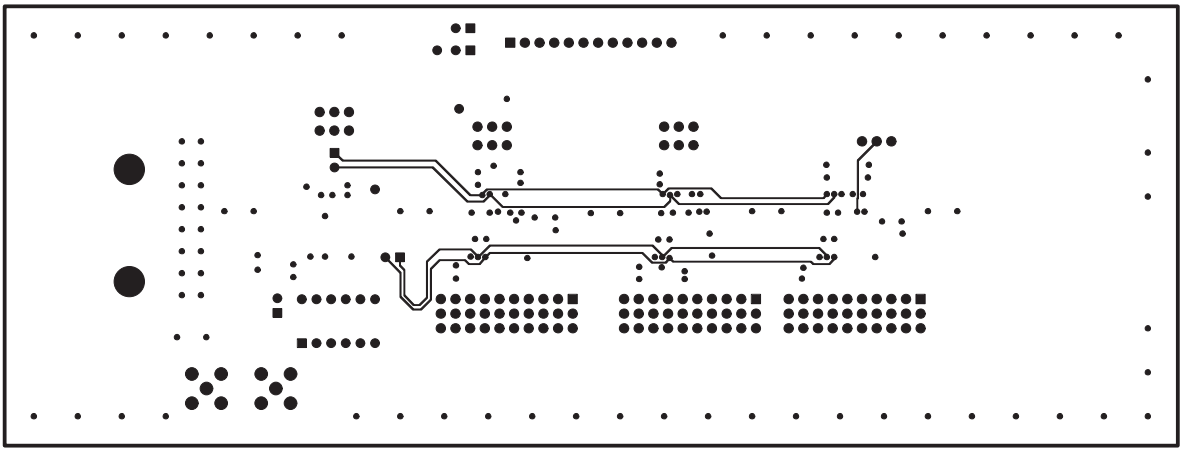


Figure A–3. Serializer Layer 8

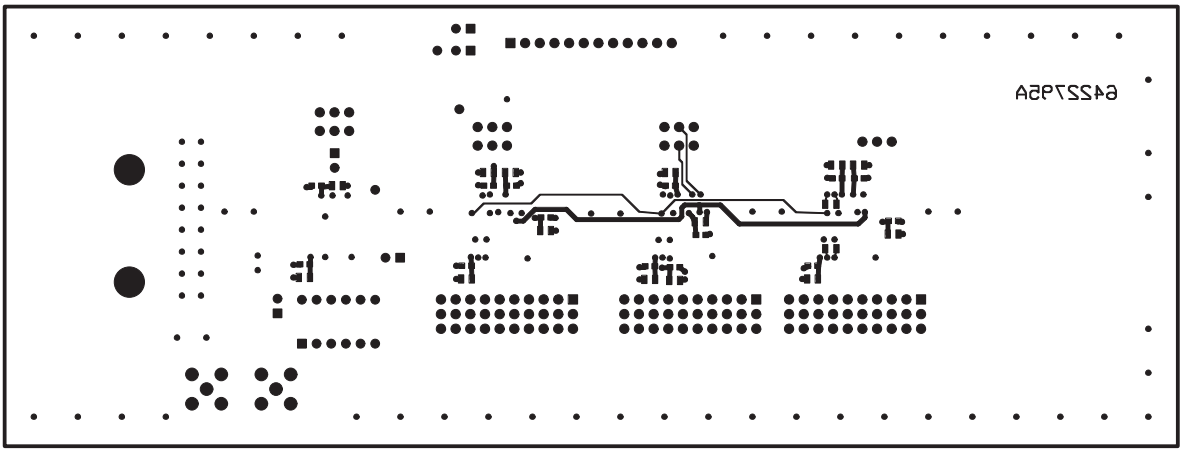


Figure A–4. Serializer Silkscreen Bottom

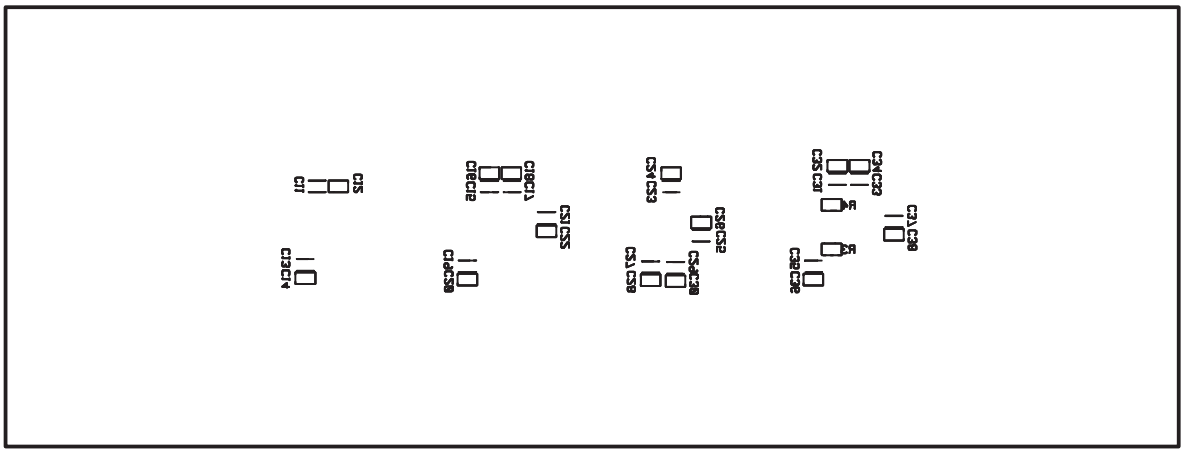


Figure A–5. Serializer Silkscreen Top

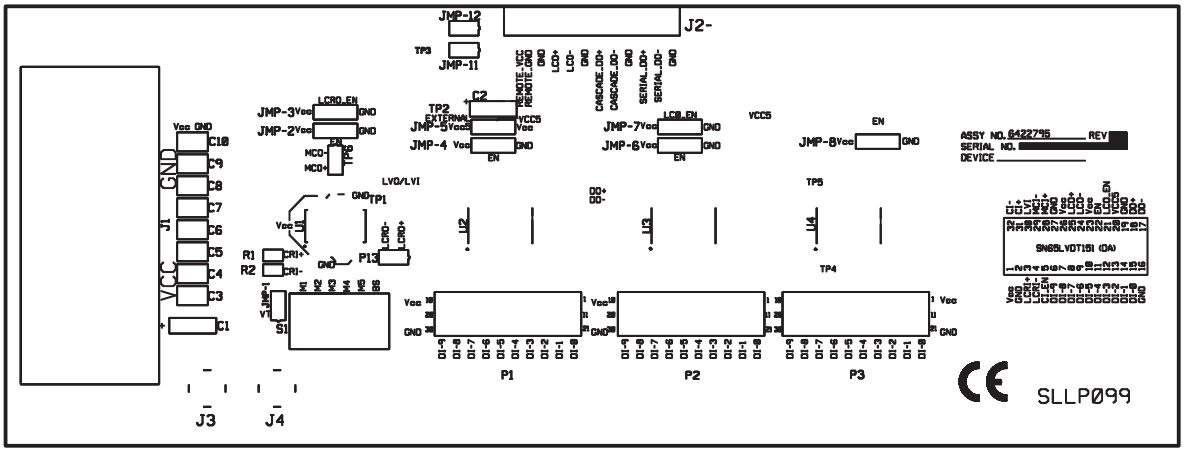


Figure A–6. Deserializer Layer 1

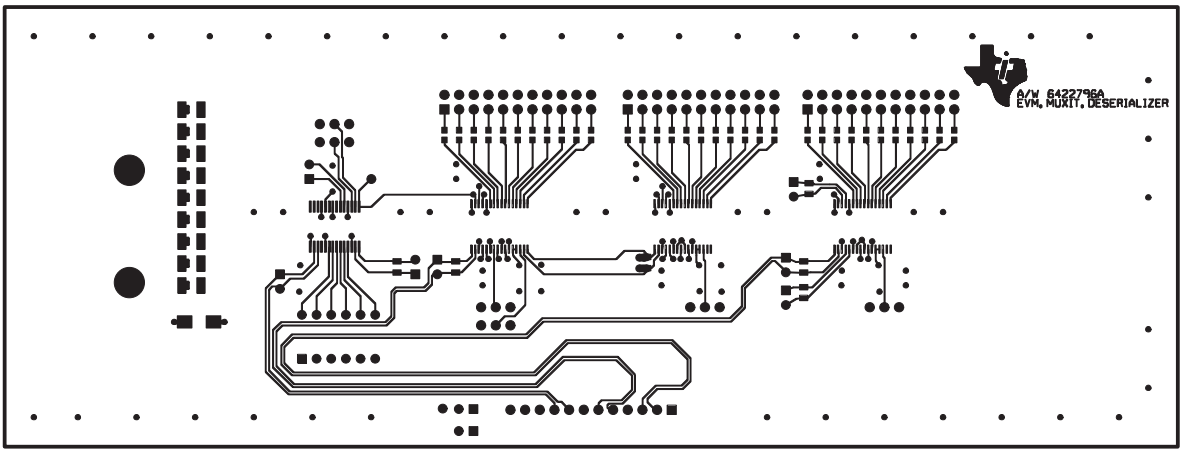


Figure A–7. Deserializer Layer 2

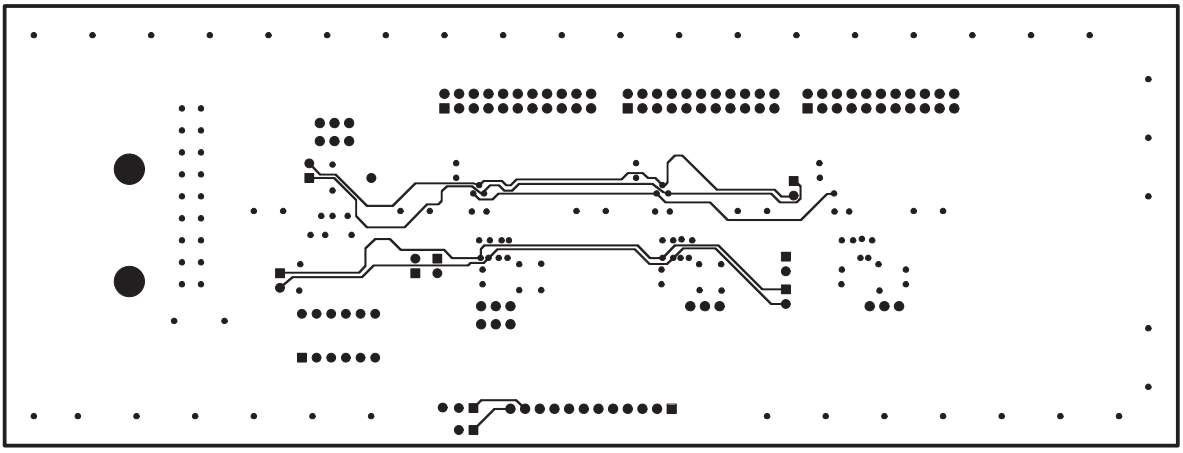


Figure A–8. Deserializer Layer 8

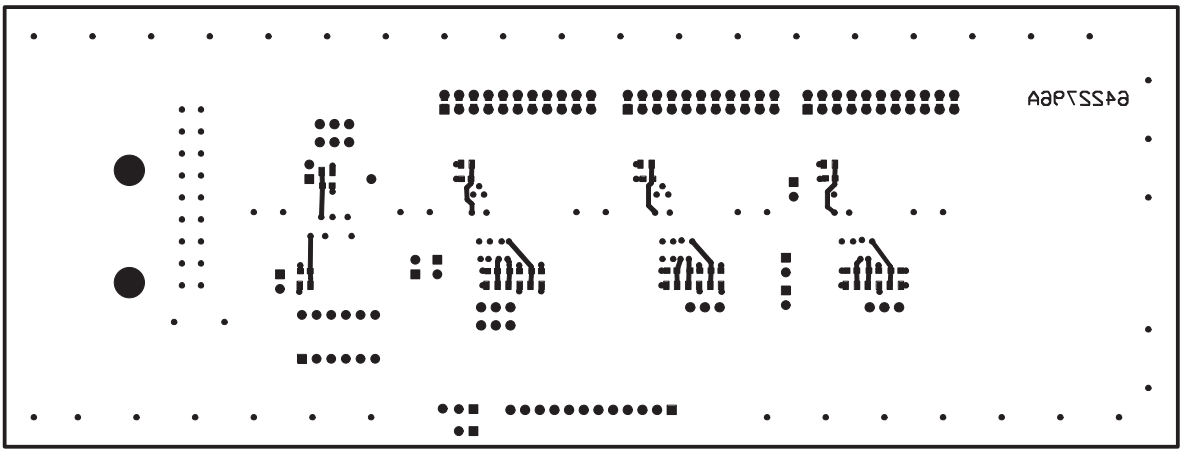


Figure A–9. Deserializer Silkscreen Bottom

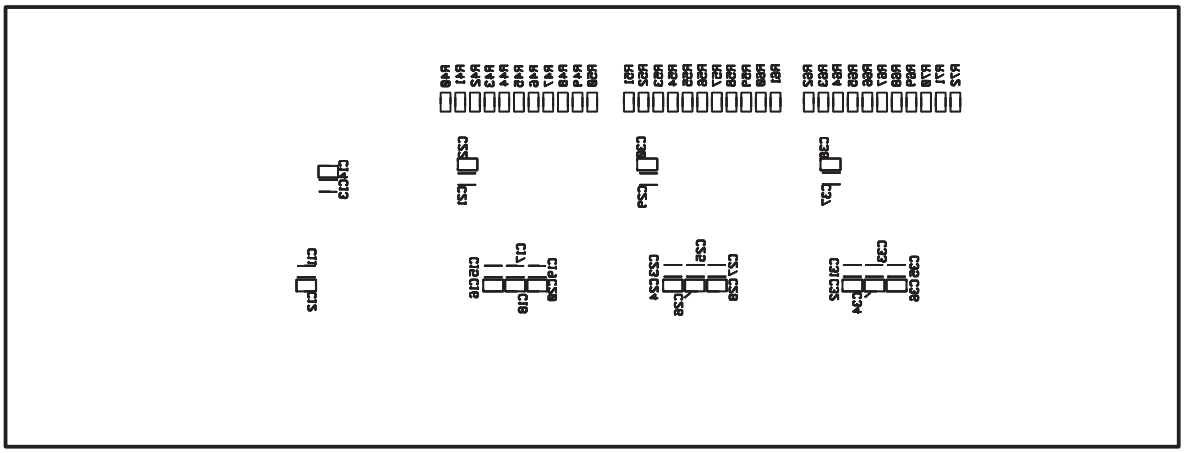
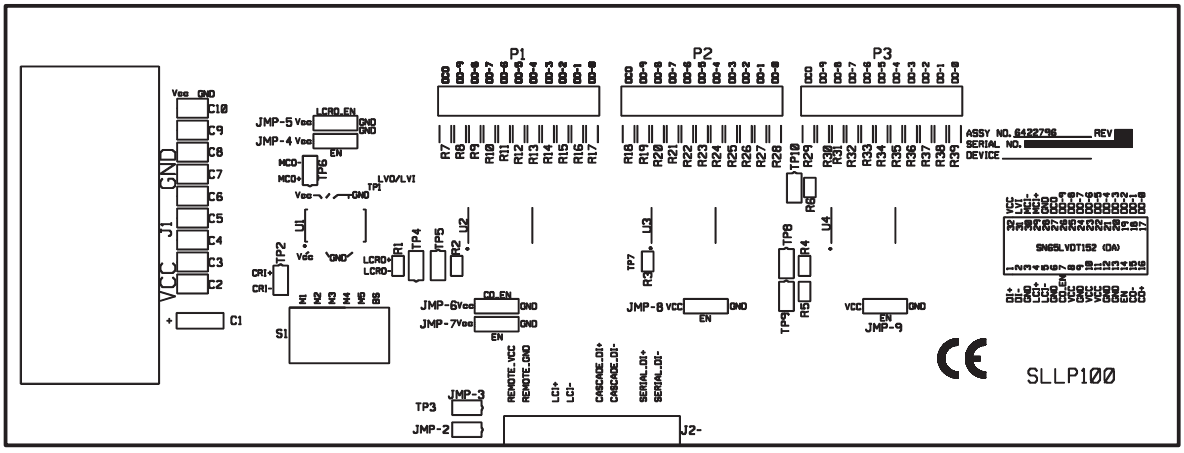
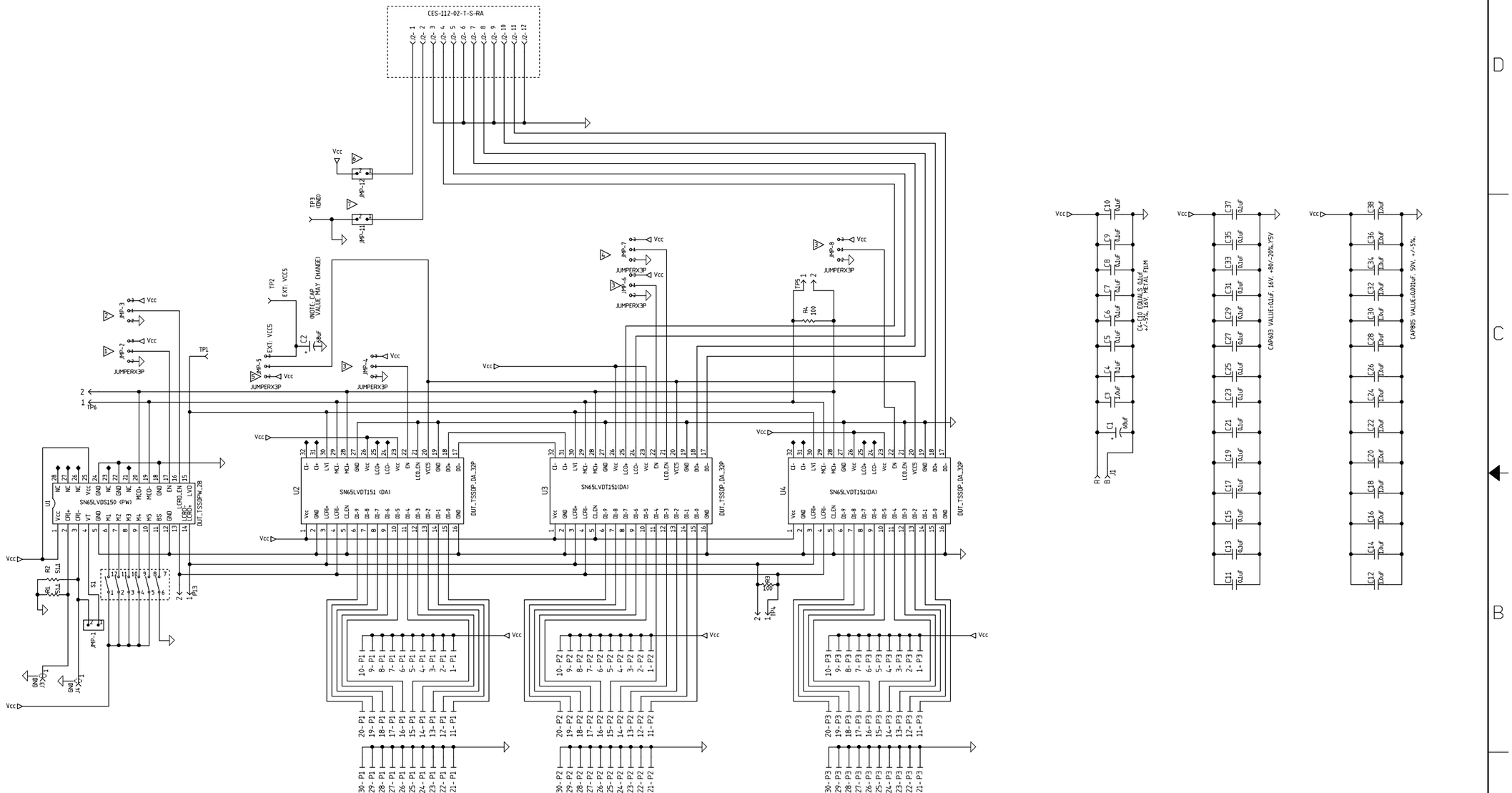


Figure A–10. Deserializer Silkscreen Top



A.3 Schematics

SYM	REVISIONS
A	ECR 2013971, 06/22/00 .MPK



1. INSTALL JUMPER FROM CENTER PIN TO VCC, TO ENABLE THE PLL FREQUENCY MULTIPLIER.
2. INSTALL JUMPER FROM CENTER PIN TO VCC, TO ENABLE LINK CLOCK REFERENCE OUTPUT FROM PLL.
3. INSTALL JUMPER FROM CENTER PIN TO VCC, TO ENABLE THE SERIALIZER/TRANSMITTER.
4. INSTALL JUMPER FROM CENTER PIN TO VCC, TO ENABLE LINK CLOCK OUTPUT FROM SERIALIZER.
5. INSTALL JUMPER FROM CENTER PIN TO VCC, WHEN INPUT SIGNALS ARE LVTTL. INSTALL JUMPER FROM CENTER PIN TO EXTVCC5 WHEN INPUTS ARE 5V TTL.
6. JUMPER 2 MAYBE INSTALLED TO CONNECT SERIALIZER VCC TO DESERIALIZER WHEN DESIRED.
7. JUMPER 3 MAYBE INSTALLED TO CONNECT SERIALIZER GND TO DESERIALIZER GND WHEN DESIRED.

DRAFTSMAN: E. LINDEMAN	DATE 07/11/00	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
DESIGNER: VENDOR	DATE 07/10/00	TITLE: SCHEMATIC, EVM, MUXIT, SERIALIZER	
CHECKER: E. COLE	DATE 07/10/00		
ENGINEER: E. COLE	DATE 07/10/00		
APPROVED: E. COLE	DATE 07/10/00		
RELEASED: MIKE KORSON	DATE 07/10/00	SCALE N / D SIZE / 6422795 / A REV / SHEET 01/01	

SYM	REVISIONS
A	ECR 2013972, 06/22/00 .MPK

1. JUMPER 2 MAYBE INSTALLED TO CONNECT SERIALIZER VCC TO DESERIALIZER WHEN DESIRED.
2. JUMPER 3 MAYBE INSTALLED TO CONNECT SERIALIZER GND TO DESERIALIZER GND WHEN DESIRED.
3. INSTALL JUMPER FROM CENTER PIN TO VCC, TO ENABLE PLL.
4. INSTALL JUMPER FROM CENTER PIN TO VCC, TO ENABLE LINK CLOCK REFERENCE OUTPUT FROM PLL.
5. INSTALL JUMPER FROM CENTER PIN TO VCC, TO ENABLE CASCADE OUTPUT.
6. INSTALL JUMPER FROM CENTER PIN TO VCC, TO ENABLE DESERIALIZER/RECEIVER.

DRAFTSMAN: E. LINDEMAN	DATE 07/12/00	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
DESIGNER: VENDOR	DATE 07/10/00	TITLE: SCHEMATIC, EVM, MUXIT, DESERIALIZER	
CHECKER: E. COLE	DATE 07/10/00		
ENGINEER: E. COLE	DATE 07/10/00		
APPROVED: E. COLE	DATE 07/10/00		
RELEASED: MIKE KORSON	DATE 07/10/00	SCALE N / SIZE D / 6422796 / REV A / SHEET 01/01	