96-Channel Data Driver
With High Voltage Push-Pull Outputs

Features

► HVCMOS® technology
► Operating output voltage of 90V
► Data clock speed 30MHz @ V_{DD} = 5V
► Six data shift registers
► Data directional loading control
► Outputs: enable, polarity, all high, all low
► CMOS compatible inputs

Applications

► Ink Jet print head driver
► AC plasma data driver

General Description

The HV582 is a low-voltage serial to high-voltage (HV) parallel converter with HV push-pull outputs. This device has been designed for use as a driver for printer applications. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capability such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

The device has 6 parallel 16-bit shift registers, permitting data rates of up to 180MHz. Data are shifted through the shift registers on the logic low to high transition of the clock. The DIR pin allows for clockwise or counter-clockwise data shifting. Data output buffers are provided for cascading the 6 shift register into one 96 bit shift register, or cascading additional HV582 devices. Transfer of data from the shift registers to the 96 latches, and to the HV outputs, occurs when the LE (latch enable) input is high.

The HV outputs are further controlled without affecting the data in shift registers and latches. All HV outputs can be forced to a high state ($\overline{OH}$ input), to a low state ($\overline{OL}$ input), to a HiZ state (OE input), or to alter their polarity (POL input).
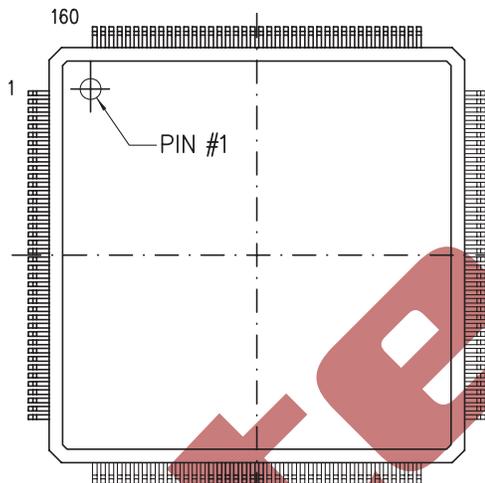
Typical Application Diagram
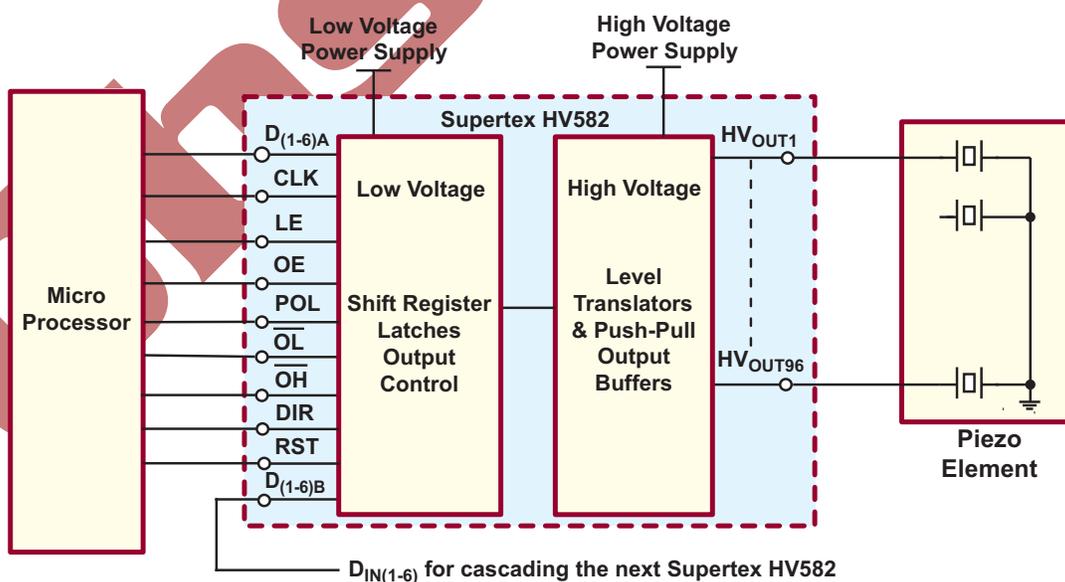
Ordering Information

Device	Package Option
	160-Lead LQFP
HV582	HV582FG-G

-G indicates package is RoHS compliant ('Green')

Package Configuration

160

1

PIN #1

Absolute Maximum Ratings

Parameter	Value
Supply Voltage, V_{DD}	-0.5V to 6V
Supply Voltage, V_{PP}	V_{DD} to 100V
Logic input voltages	-0.5V to V_{DD}+0.5V
Tj, junction temperature	-40°C to +125°C
Storage temperature	-65°C +150°C

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	4.5	5.0	5.5	V
V_{PP}	High voltage supply	10	-	90	V
V_{IH}	High-level input voltage	V_{DD} −0.9	-	V_{DD}	V
V_{IL}	Low-level input voltage	0	-	0.9	V
T_A	Operating free-air temperature	-40	-	+85	°C

Power-up Sequence

Power-up sequence should be the following:

1	Connect ground.
2	Apply V_{DD}.
3	Set all inputs (Data, CLK, LE, etc.) to a known state.
4	Apply V_{PP}.

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics

*(Over operating supply voltages unless otherwise specified)*

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{PPQ}	V_{PP} quiescent supply current	-	-	100	µA	---
I_{DDQ}	V_{DD} quiescent supply current	-	-	100	µA	---
I_{DD}	V_{DD} supply current	-	-	25	mA	F_{CLK} = 30MHz, LE = low
HV_{OH}	High level output voltage	80	85	-	V	I_{OUT} = +75mA, V_{PP} = 90V
HV_{OHD}	Output p-channel body diode	-	-	93	V	I_{OUT} = -75mA, V_{PP} = 90V
HV_{OL}	Low level output voltage	-	5.0	10	V	I_{OUT} = -75mA
HV_{OLD}	Output n-channel body diode	-3.0	-	-	V	I_{OUT} = +75mA
I_{IH}	Logic input high current	-	-	1.0	µA	V_{IH} = V_{DD}
		10	30	50	µA	V_{IH} = V_{DD}, For DIR, and POL only
I_{IL}	Logic input low current	-1.0	-	-	µA	V_{IL} = -0.3V
V_{OH}	Logic output high	3.5	-	-	V	I_{OUT} = 4.0mA
V_{OL}	Logic output low	-	-	1.0	V	I_{OUT} = -4.0mA

AC Electrical Characteristics

(Over operating supply voltages unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Data clock frequency	-	-	30	MHz	---
t_{wCLK}	Clock pulse width, high and low	16.6	-	-	ns	---
t_{wLE}	LE pulse width, high and low	16.6	-	-	ns	---
t_{su1}	Setup time, $D_{nA/B}$ to CLK	5	-	-	ns	---
t_{su2}	Setup time, CLK to LE	15	-	-	ns	---
t_{su3}	Setup time, LE to $\overline{OL}$, $\overline{OH}$	25	-	-	ns	---
t_{h1}	Hold time, CLK to $D_{nA/B}$	15	-	-	ns	---
t_{h2}	Hold time, LE to CLK	15	-	-	ns	---
t_{pdHL}	CLK to $D_{nA/B}$	-	-	25	ns	C = 170pF
t_{pdLH}	CLK to $D_{nA/B}$	-	-	25	ns	C = 170pF
t_{pHL}	LE, $\overline{OH}$, $\overline{OL}$ to HV_{OUTS}	-	-	300	ns	C = 170pF
t_{pLH}	LE, $\overline{OH}$, $\overline{OL}$ to HV_{OUTS}	-	-	300	ns	C = 170pF
t_{pHZL}	OE to HV_{OUTS}	-	-	150	ns	C = 170pF
t_{pLZH}	OE to HV_{OUTS}	-	-	150	ns	C = 170pF
t_{pHZ}	OE to HV_{OUTS}	-	-	300	ns	---
t_{pLZ}	OE to HV_{OUTS}	-	-	300	ns	---
t_r	HV_{OUTS}	-	-	200	ns	C = 170pF
t_f	HV_{OUTS}	-	-	200	ns	C = 170pF

Switching Waveforms
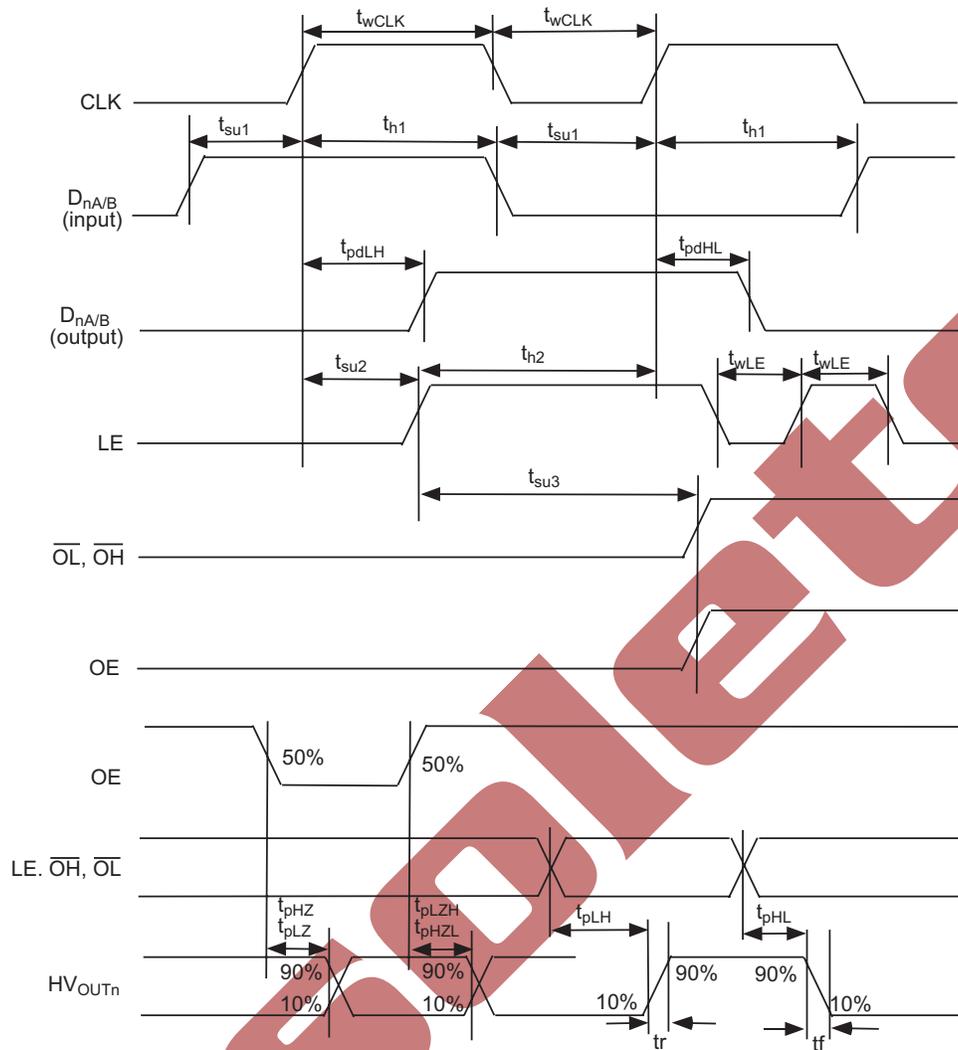
Input and Output Equivalent Circuits

Logic Inputs

Logic Data Output

High Voltage Outputs
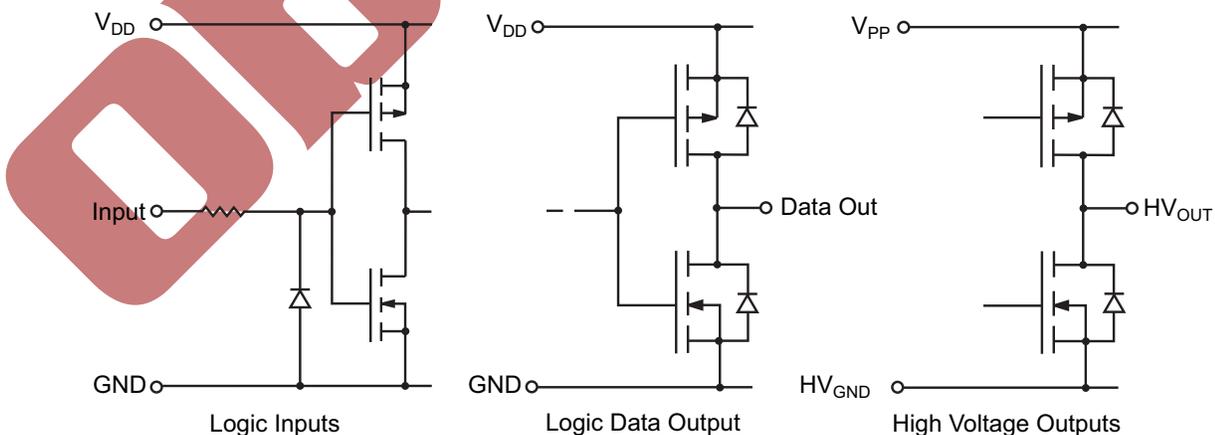
Functional Block Diagram
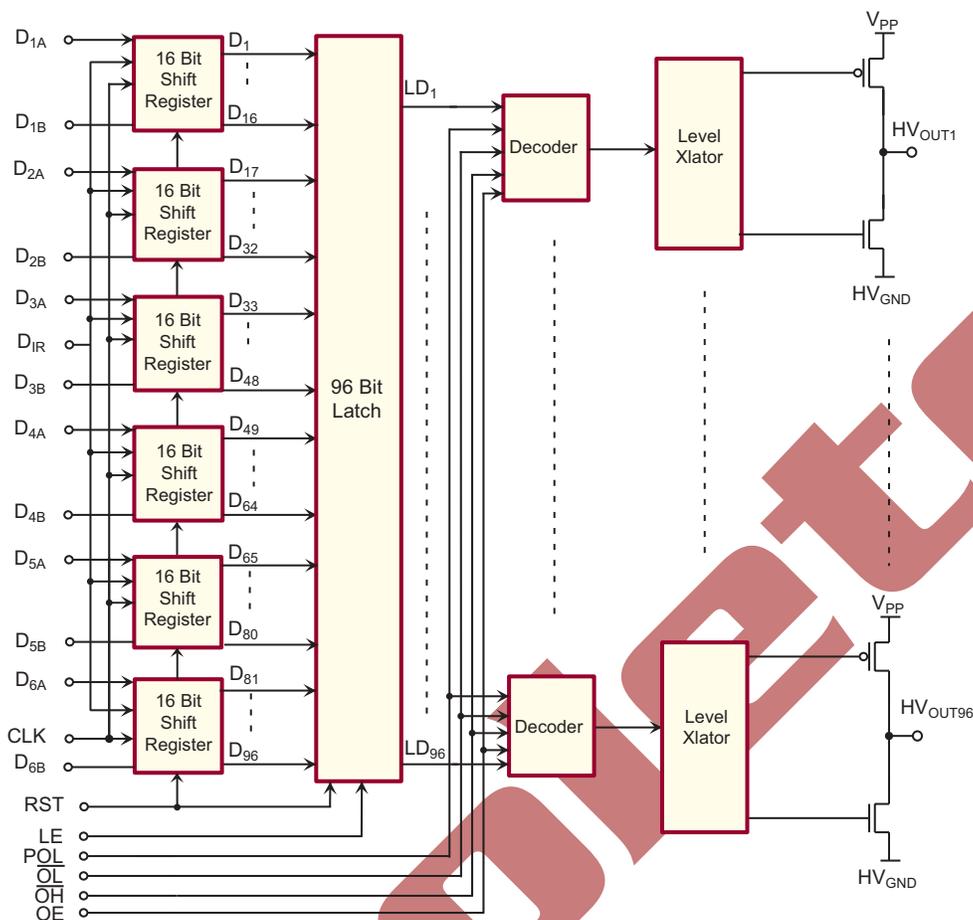
Function Table

| Function | Inputs | | | | | | | | Outputs | | |
	RST	Data	CLK	LE	OE	POL	$\overline{OL}$	$\overline{OH}$	Shift Reg 1 2…96	HV Outputs 1 2..96	Data Out
All low	L	X	X	X	H	X	L	X	* *…*	L L…L	*
All high	L	X	X	X	H	X	H	L	* *…*	H H…H	*
Outputs Hi-Z	L	X	X	X	L	X	X	X	* *…*	Z Z…Z	*
Invert mode	L	X	X	L	H	H	H	H	* *…*	* *…* (b)	*
Load S/R	L	H or L	⌐	L	H	L	H	H	H or L *…*	* *…*	*
Store Data in latches	L	X	X	L	H	L	H	H	* *…*	* *…*	*
	L	X	X	L	H	H	H	H	* *…*	* *…* (b)	*
Transparent mode	L	L	⌐	H	H	L	H	H	L *…*	L *…*	*
	L	H	⌐	H	H	L	H	H	H *…*	H *…*	*
Reset	H	X	X	X	H	L	H	H	L *…*	L *…*	L

DIR is direction control: H shifts in $Q_N \blacktriangleright Q_{N-1}$ direction, L shifts in $Q_N \blacktriangleright Q_{N+1}$ direction.

Notes: H = high level, L = low level, X = irrelevant, ⌐ = low-to-high transition, (b) indicates inversion
*   * = dependent on previous stage's state before the last CLK or last LE high.*
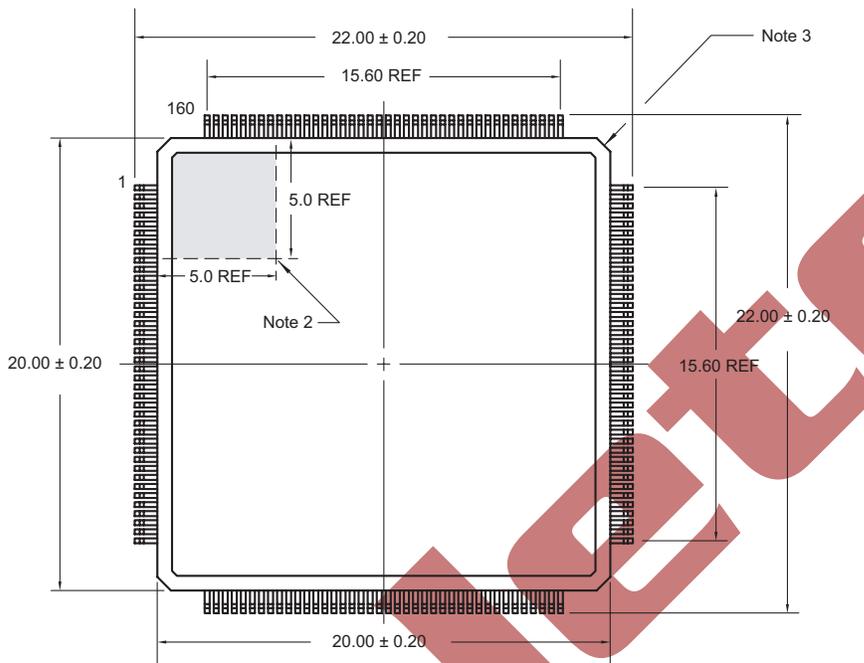
Pin Description

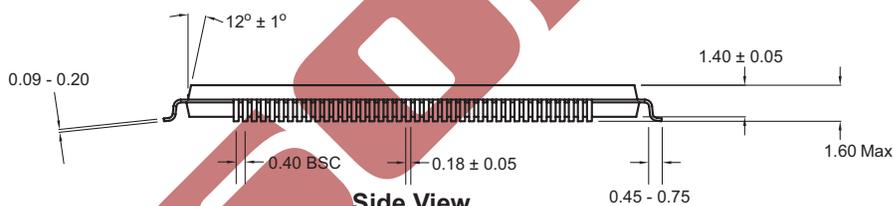| Pin Number	Name	Function	Description
65	CLK	Shift register clock	Input data are shifted into the data shift register on the positive edge of the clock.
64	LE	Latch enable input	When LE is high, data is transferred from data shift register to the HV_{OUT} output latch. When LE is low, data is latched into data latches and new data can be clocked into the shift register.
63	RST	Power on reset	1 = Resets all shift registers and latches to low
61	DIR	Shift register direction input	When DIR is set high, the HV_{OUT} loading sequence is HV_{OUT96} to HV_{OUT1}. When DIR is set low, the HV_{OUT} loading sequence is HV_{OUT1} to HV_{OUT96}.
56	POL	Polarity input	Inverts the polarity of the HV_{OUTS}.
57	OE	High impedance control	When OE is high, the HV_{OUTS} are enabled and form a push-pull configuration. When OE is low, all HV_{OUTS} are in a high impedance state.
58	$\overline{OL}$	All outputs low	When $\overline{OL}$ is low, all HV_{OUTS} are forced to a low state, regardless of data in each channel. When $\overline{OL}$ is high, HV_{OUTS} reflect data in each channel.
59	$\overline{OH}$	All outputs high	When $\overline{OH}$ is low, all HV_{OUTS} are forced to a high state, regardless of data in each channel. When $\overline{OH}$ is high, HV_{OUTS} reflects data in each channel.
66-71	D_{1A}, D_{2A}, D_{3A}, D_{4A}, D_{5A}, D_{6A}	Data IO input/output designation	When DIR is low, these six IOs are configured as inputs to the data shift registers. When DIR is high, they are configured as outputs of the data shift registers.
50-55	D_{1B}, D_{2B}, D_{3B}, D_{4B}, D_{5B}, D_{6B}	Data IO output/input designation	When DIR is high, these six IOs are configured as inputs to the data shift registers. When DIR is low, they are configured as outputs of the data shift registers.
1-41, 75-76, 80-127, 154-160	$HV_{OUT1-96}$	High voltage outputs	---
62, 74	GND	Logic ground	---
47, 60	V_{DD}	Logic power	---
45-46, 75-76, 136-137, 140-141, 144-145	HV_{GND}	High voltage ground	---
42-44, 77-79, 128-129, 131-132, 149-150, 152-153	V_{PP}	High voltage power	---

Package Pin Configuration

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	HV_{OUT56}	41	HV_{OUT96}	81	HV_{OUT2}	121	HV_{OUT42}
2	HV_{OUT57}	42	V_{PP}	82	HV_{OUT3}	122	HV_{OUT43}
3	HV_{OUT58}	43	V_{PP}	83	HV_{OUT4}	123	HV_{OUT44}
4	HV_{OUT59}	44	V_{PP}	84	HV_{OUT5}	124	HV_{OUT45}
5	HV_{OUT60}	45	HV_{GND}	85	HV_{OUT6}	125	HV_{OUT46}
6	HV_{OUT61}	46	HV_{GND}	86	HV_{OUT7}	126	HV_{OUT47}
7	HV_{OUT62}	47	V_{DD}	87	HV_{OUT8}	127	HV_{OUT48}
8	HV_{OUT63}	48	NC	88	HV_{OUT9}	128	V_{PP}
9	HV_{OUT64}	49	NC	89	HV_{OUT10}	129	V_{PP}
10	HV_{OUT65}	50	D_{6B}	90	HV_{OUT11}	130	NC
11	HV_{OUT66}	51	D_{5B}	91	HV_{OUT12}	131	V_{PP}
12	HV_{OUT67}	52	D_{4B}	92	HV_{OUT13}	132	V_{PP}
13	HV_{OUT68}	53	D_{3B}	93	HV_{OUT14}	133	NC
14	HV_{OUT69}	54	D_{2B}	94	HV_{OUT15}	134	NC
15	HV_{OUT70}	55	D_{1B}	95	HV_{OUT16}	135	NC
16	HV_{OUT71}	56	POL	96	HV_{OUT17}	136	HV_{GND}
17	HV_{OUT72}	57	OE	97	HV_{OUT18}	137	HV_{GND}
18	HV_{OUT73}	58	$\overline{OL}$	98	HV_{OUT19}	138	NC
19	HV_{OUT74}	59	$\overline{OH}$	99	HV_{OUT20}	139	NC
20	HV_{OUT75}	60	V_{DD}	100	HV_{OUT21}	140	HV_{GND}
21	HV_{OUT76}	61	DIR	101	HV_{OUT22}	141	HV_{GND}
22	HV_{OUT77}	62	GND	102	HV_{OUT23}	142	NC
23	HV_{OUT78}	63	RST	103	HV_{OUT24}	143	NC
24	HV_{OUT79}	64	LE	104	HV_{OUT25}	144	HV_{GND}
25	HV_{OUT80}	65	CLK	105	HV_{OUT26}	145	HV_{GND}
26	HV_{OUT81}	66	D_{6A}	106	HV_{OUT27}	146	NC
27	HV_{OUT82}	67	D_{5A}	107	HV_{OUT28}	147	NC
28	HV_{OUT83}	68	D_{4A}	108	HV_{OUT29}	148	NC
29	HV_{OUT84}	69	D_{3A}	109	HV_{OUT30}	149	V_{PP}
30	HV_{OUT85}	70	D_{2A}	110	HV_{OUT31}	150	V_{PP}
31	HV_{OUT86}	71	D_{1A}	111	HV_{OUT32}	151	NC
32	HV_{OUT87}	72	NC	112	HV_{OUT33}	152	V_{PP}
33	HV_{OUT88}	73	NC	113	HV_{OUT34}	153	V_{PP}
34	HV_{OUT89}	74	GND	114	HV_{OUT35}	154	HV_{OUT49}
35	HV_{OUT90}	75	HV_{GND}	115	HV_{OUT36}	155	HV_{OUT50}
36	HV_{OUT91}	76	HV_{GND}	116	HV_{OUT37}	156	HV_{OUT51}
37	HV_{OUT92}	77	V_{PP}	117	HV_{OUT38}	157	HV_{OUT52}
38	HV_{OUT93}	78	V_{PP}	118	HV_{OUT39}	158	HV_{OUT53}
39	HV_{OUT94}	79	V_{PP}	119	HV_{OUT40}	159	HV_{OUT54}
40	HV_{OUT95}	80	HV_{OUT1}	120	HV_{OUT41}	160	HV_{OUT55}

160-Lead LQFP (FG) Package Outline

22.00 ± 0.20

15.60 REF

Note 3

160

1

5.0 REF

5.0 REF

Note 2

20.00 ± 0.20

22.00 ± 0.20

15.60 REF

20.00 ± 0.20

Top View

12° ± 1°

0.09 - 0.20

1.40 ± 0.05

1.60 Max

0.40 BSC

0.18 ± 0.05

0.45 - 0.75

Side View

Notes:

1. All dimensions in millimeters. Angles in degrees.
2. Details of pin 1 identifier are optional, but must be located within the zone indicated.
3. Corner shape may differ from drawing.

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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