

## SINGLE-ENDED OUTPUT SILICON OSCILLATOR

### Features

- Quartz-free, MEMS-free, and PLL-free all-silicon oscillator
- Any output frequencies from 0.9 to 200 MHz
- Short lead times
- Excellent temperature stability ( $\pm 20$  ppm)
- Highly reliable startup and operation
- High immunity to shock and vibration
- Low jitter:  $< 1.5$  ps rms
- 0 to 85 °C operation includes 10-year aging in hot environments
- Footprint compatible with industry-standard 3.2 x 5.0 mm XOs
- CMOS and SSTL versions available
- Driver stopped, tri-state, or powerdown operation
- RoHS compliant
- 1.8, 2.5, or 3.3 V options
- Low power
- More than 10x better fit rate than competing crystal solutions



### Specifications

| Parameters            | Condition                                           | Min  | Typ      | Max       | Units |
|-----------------------|-----------------------------------------------------|------|----------|-----------|-------|
| Frequency Range       |                                                     | 0.9  | —        | 200       | MHz   |
| Frequency Stability   | Temperature stability, 0 to +70 °C                  | —    | $\pm 10$ | —         | ppm   |
|                       | Temperature stability, 0 to +85 °C                  | —    | $\pm 20$ | —         | ppm   |
|                       | Total stability, 0 to +70 °C operation <sup>1</sup> | —    | —        | $\pm 150$ | ppm   |
|                       | Total stability, 0 to +85 °C operation <sup>2</sup> | —    | —        | $\pm 250$ | ppm   |
| Operating Temperature | Commercial                                          | 0    | —        | 70        | °C    |
|                       | Extended commercial                                 | 0    | —        | 85        | °C    |
| Storage Temperature   |                                                     | -55  | —        | +125      | °C    |
| Supply Voltage        | 1.8 V option                                        | 1.71 | —        | 1.98      | V     |
|                       | 2.5 V option                                        | 2.25 | —        | 2.75      | V     |
|                       | 3.3 V option                                        | 2.97 | —        | 3.63      | V     |

#### Notes:

1. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, first-year aging at 25 °C, shock, vibration, and one solder reflow.
2. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, ten-year aging at 85 °C, shock, vibration, and one solder reflow.
3. See "AN409: Output Termination Options for the Si500S and Si500D Silicon Oscillators" for further details regarding output clock termination recommendations.
4.  $V_{TT} = .5 \times V_{DD}$ .
5.  $V_{TT} = .45 \times V_{DD}$ .

| Parameters                             | Condition                                                                                             | Min                          | Typ  | Max                          | Units  |
|----------------------------------------|-------------------------------------------------------------------------------------------------------|------------------------------|------|------------------------------|--------|
| Supply Current                         | 1.8 V option, 40 pF, 40 MHz, CMOS                                                                     | —                            | 13.9 | 16                           | mA     |
|                                        | 1.8 V option, 10 pF, 200 MHz, CMOS                                                                    | —                            | 16.7 | 19                           | mA     |
|                                        | 2.5 V option, 40 pF, 40 MHz, CMOS                                                                     | —                            | 15.8 | 18                           | mA     |
|                                        | 2.5 V option, 10 pF, 200 MHz, CMOS                                                                    | —                            | 19.3 | 22                           | mA     |
|                                        | 3.3 V option, 40 pF, 40 MHz, CMOS                                                                     | —                            | 17.7 | 20                           | mA     |
|                                        | 3.3 V option, 10 pF, 200 MHz, CMOS                                                                    | —                            | 21.5 | 24                           | mA     |
|                                        | SSTL-3.3, 200 MHz                                                                                     | —                            | 18.1 | 20.2                         | mA     |
|                                        | SSTL-2.5, 200 MHz                                                                                     | —                            | 18.0 | 19.7                         | mA     |
|                                        | SSTL-1.8, 200 MHz                                                                                     | —                            | 16.8 | 18.7                         | mA     |
|                                        | Output Stopped, CMOS                                                                                  | —                            | 11.8 | 13.1                         | mA     |
|                                        | Tri-State                                                                                             | —                            | 9.7  | 10.7                         | mA     |
|                                        | Powerdown                                                                                             | —                            | 1.0  | 1.9                          | mA     |
| Output Symmetry                        | $0.5 \times V_{DD}$                                                                                   | $46 - 13 \text{ ns}/T_{CLK}$ | —    | $54 + 13 \text{ ns}/T_{CLK}$ | %      |
| Rise and Fall Times <sup>3</sup>       | CMOS, $C_L = 15 \text{ pF}$ measured from 20 to 80% of $V_{DD}$                                       | —                            | 1.4  | 2.0                          | ns     |
|                                        | SSTL                                                                                                  | —                            | —    | 0.6                          | ns     |
| CMOS Output Voltage                    | $V_{OH}$ , sourcing 9 mA                                                                              | $V_{DD} - 0.5$               | —    | —                            | V      |
|                                        | $V_{OL}$ , sinking 9 mA                                                                               | —                            | —    | 0.5                          | V      |
| SSTL-1.8 Output Voltage <sup>4</sup>   | $V_{OH}$                                                                                              | $V_{TT} + 0.375$             | —    | —                            | V      |
|                                        | $V_{OL}$                                                                                              | —                            | —    | $V_{TT} - 0.375$             |        |
| SSTL-2.5 Output Voltage <sup>4</sup>   | $V_{OH}$                                                                                              | $V_{TT} + 0.48$              | —    | —                            | V      |
|                                        | $V_{OL}$                                                                                              | —                            | —    | $V_{TT} - 0.48$              |        |
| SSTL-3.3 Output Voltage <sup>5</sup>   | $V_{OH}$                                                                                              | $V_{TT} + 0.48$              | —    | —                            | V      |
|                                        | $V_{OL}$                                                                                              | —                            | —    | $V_{TT} - 0.48$              |        |
| Powerup Time                           | From time $V_{DD}$ crosses min spec supply                                                            | —                            | —    | 2                            | ms     |
| OE Deassertion to Clk Stop             |                                                                                                       | —                            | —    | $250 + 3 \times T_{CLK}$     | ns     |
| Return from Output Driver Stopped Mode |                                                                                                       | —                            | —    | $250 + 3 \times T_{CLK}$     | ns     |
| Return from Tri-State Time             |                                                                                                       | —                            | —    | $12 + 3 \times T_{CLK}$      | μs     |
| Return from Powerdown Time             |                                                                                                       | —                            | —    | 2                            | ms     |
| Period Jitter (1-sigma)                | SSTL <sup>3</sup>                                                                                     | —                            | 1    | 2                            | ps RMS |
| Integrated Phase Jitter                | 1 MHz – $0.4 \times F_{OUT}$ , SSTL or CMOS and $C_L \leq 7 \text{ pF}$ , $F_{OUT} > 2.5 \text{ MHz}$ | —                            | 0.7  | 1.5                          | ps RMS |

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2. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, ten-year aging at 85 °C, shock, vibration, and one solder reflow.
3. See "AN409: Output Termination Options for the Si500S and Si500D Silicon Oscillators" for further details regarding output clock termination recommendations.
4.  $V_{TT} = .5 \times V_{DD}$ .
5.  $V_{TT} = .45 \times V_{DD}$ .

## Package Specifications

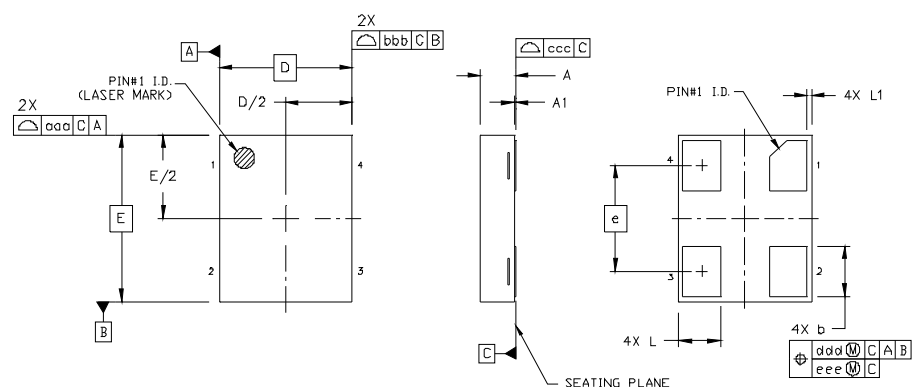


Table 1. Package Diagram Dimensions (mm)

| Dimension | Min      | Nom  | Max  |
|-----------|----------|------|------|
| A         | 0.80     | 0.85 | 0.90 |
| A1        | 0.00     | 0.03 | 0.05 |
| b         | 1.15     | 1.20 | 1.25 |
| D         | 3.20 BSC |      |      |
| e         | 2.54 BSC |      |      |
| E         | 4.00 BSC |      |      |
| L         | 0.95     | 1.00 | 1.05 |

| Dimension | Min  | Nom  | Max  |
|-----------|------|------|------|
| L1        | 0.00 | 0.05 | 0.10 |
| aaa       |      |      | 0.10 |
| bbb       |      |      | 0.10 |
| ccc       |      |      | 0.08 |
| ddd       |      |      | 0.10 |
| eee       |      |      | 0.05 |

Table 2. Pad Connections

|   |        |
|---|--------|
| 1 | OE     |
| 2 | GND    |
| 3 | Output |
| 4 | VDD    |

Table 3. Tri-State/Powerdown/Driver Stopped Function on OE (3rd Option Code)

|         | A         | B         | C          | D          | E              | F              |
|---------|-----------|-----------|------------|------------|----------------|----------------|
| Open    | Active    | Active    | Active     | Active     | Active         | Active         |
| 1 Level | Active    | Tri-State | Active     | Power-down | Active         | Driver Stopped |
| 0 Level | Tri-State | Active    | Power-down | Active     | Driver Stopped | Active         |

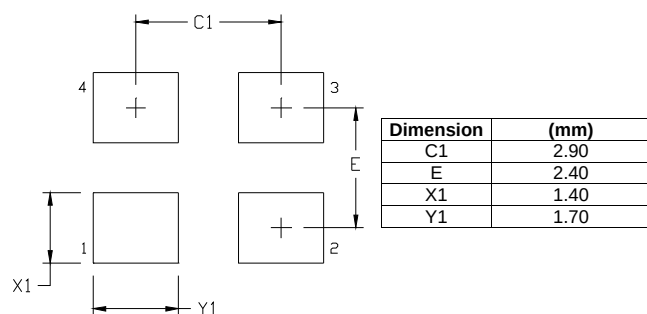
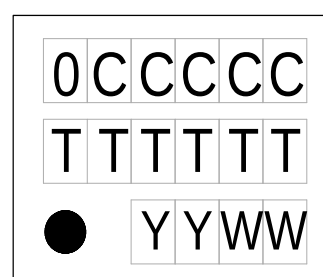


Figure 1. Recommended Land Pattern



0 = Si500  
 CCCCC = mark code  
 TTTTTT = assembly manufacturing code  
 YY = year  
 WW = work week

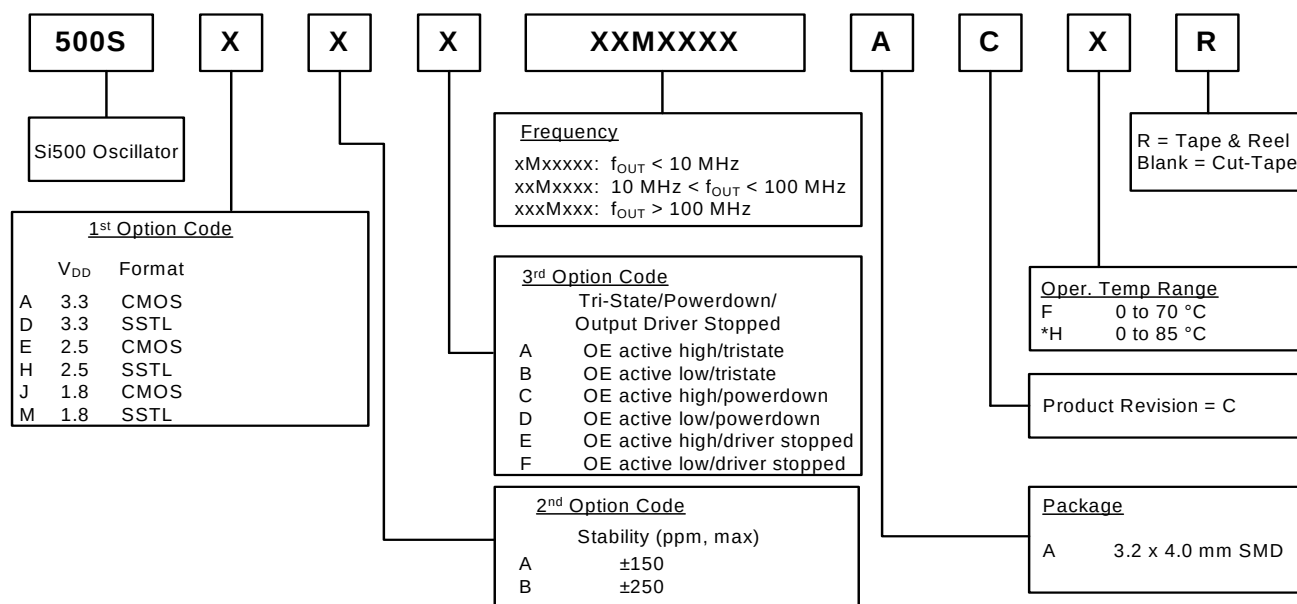
Figure 2. Top Mark

## Environmental Compliance

| Parameter                    | Conditions/Test Method            |
|------------------------------|-----------------------------------|
| Mechanical Shock             | MIL-STD-883, Method 2002.4        |
| Mechanical Vibration         | MIL-STD-883, Method 2007.3 A      |
| Resistance to Soldering Heat | MIL-STD-202, 260 C° for 8 seconds |
| Solderability                | MIL-STD-883, Method 2003.8        |
| Damp Heat                    | IEC 68-2-3                        |
| Moisture Sensitivity Level   | J-STD-020, MSL 3                  |

## Ordering Information

The Si500S supports a variety of options including frequency, output format, supply voltage, and tri-state/powerdown/output driver stopped mode. Specific device configurations are programmed into the Si500S at time of shipment. Configurations are specified using the figure below. Silicon Labs provides a web-based part number utility that can be used to simplify part number configuration. Refer to [www.silabs.com/SiliconXOPartnumber](http://www.silabs.com/SiliconXOPartnumber) to access this tool. The Si500S silicon oscillator is supplied in a ROHS-compliant, 4-pad, 3.2 x 4.0 mm package. Tape and reel packaging is available as an ordering option.



\*Note: Only ±250 ppm is supported.

## DOCUMENT CHANGE LIST

### Revision 0.3 to Revision 0.4

- Revision B to Revision C updated in Ordering Information
- 0 to 85 °C Operating Temperature Range option added
- Multiple CMOS output format codes removed

### Revision 0.4 to Revision 1.0

- Clarified SSTL specifications.
- Revised CMOS supply current max values .

### Revision 1.0 to Revision 1.1

- Updated Ordering information for  $\pm 250$  ppm from 0 to +85 °C.
- Updated jitter from 1.5 ps to 1.5 ps rms.
- Updated operating temperature to include extended commercial at 0 to +85 °C.

## ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

[www.silabs.com/CBPro](http://www.silabs.com/CBPro)



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Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
USA

<http://www.silabs.com>