

# S71GL-N Based MCPs

**Stacked Multi-Chip Product (MCP)**

**Flash Memory and RAM**

**64/32 Megabit (4/2M x 16-bit) CMOS 3.0 Volt-Only**

**Page Mode Flash Memory and**

**32/16 Megabit (2M/1M x 16-bit) Pseudo Static RAM**

***Data Sheet*** (*Advance Information*)

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# S71GL-N Based MCPs

## Stacked Multi-Chip Product (MCP)

### Flash Memory and RAM

64/32 Megabit (4/2M x 16-bit) CMOS 3.0 Volt-Only

Page Mode Flash Memory and

32/16 Megabit (2M/1M x 16-bit) Pseudo Static RAM



*Data Sheet (Advance Information)*

## Distinctive Characteristics

### MCP Features

■ **Power Supply Voltage of 2.7V to 3.3V**

■ **High Performance**

- 90 ns access time (90 ns Flash, 70 ns pSRAM/SRAM)
- 25 ns page read times

### ■ Packages

- 7 x 9 x 1.2 mm 56 ball FBGA

### ■ Operating Temperature

- –25°C to +85°C

## General Description

The S71GL-N product series consists of S29GL-N Flash memory with pSRAM combinations defined as:

|               |       | Flash Memory Density |             |
|---------------|-------|----------------------|-------------|
|               |       | 32 Mb                | 64 Mb       |
| pSRAM Density | 16 Mb | S71GL032NA0          |             |
|               | 32 Mb |                      | S71GL064NB0 |

For detailed specifications, please refer to the individual data sheets.

| Document                           | Publication Identification Number (PID) |
|------------------------------------|-----------------------------------------|
| S29GL-N                            | S29GL-N_00                              |
| SPH016D970R1R (16 Mb pSRAM Type 9) | SPH016D970R1R                           |
| SPH032D970R1R (32 Mb pSRAM Type 9) | SPH032D970R1R                           |

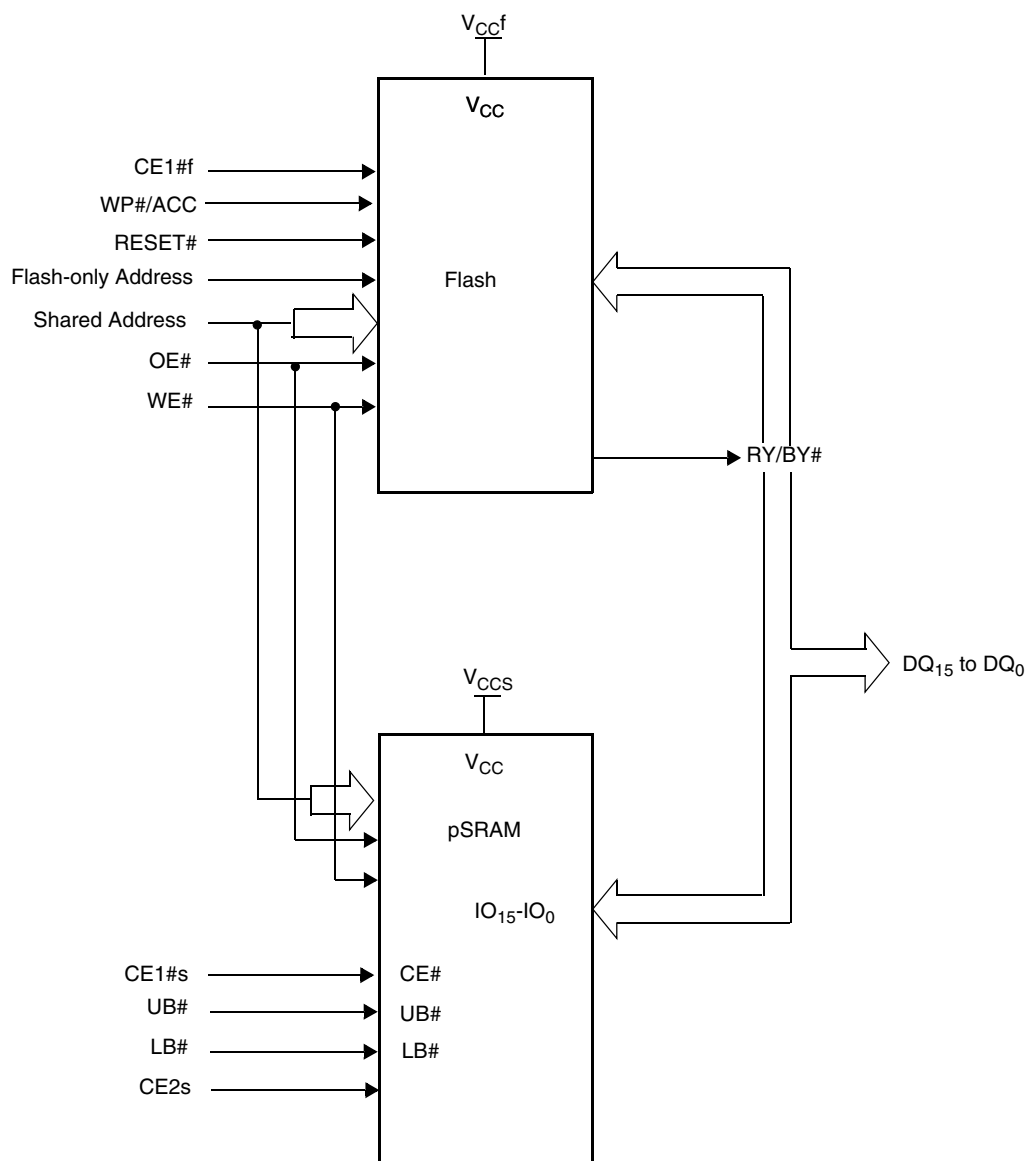
## 1. Product Selector Guide

| Device-Model# (Note) | (p)SRAM density | (p)SRAM type | Package |
|----------------------|-----------------|--------------|---------|
| S71GL032NA0-0K       | 16 Mb           | pSRAM 9      | TLC056  |
| S71GL032NA0-0P       |                 |              |         |
| S71GL064NB0-0K       | 32 Mb           | pSRAM 9      | TLC056  |
| S71GL064NB0-0P       |                 |              |         |

**Note:**

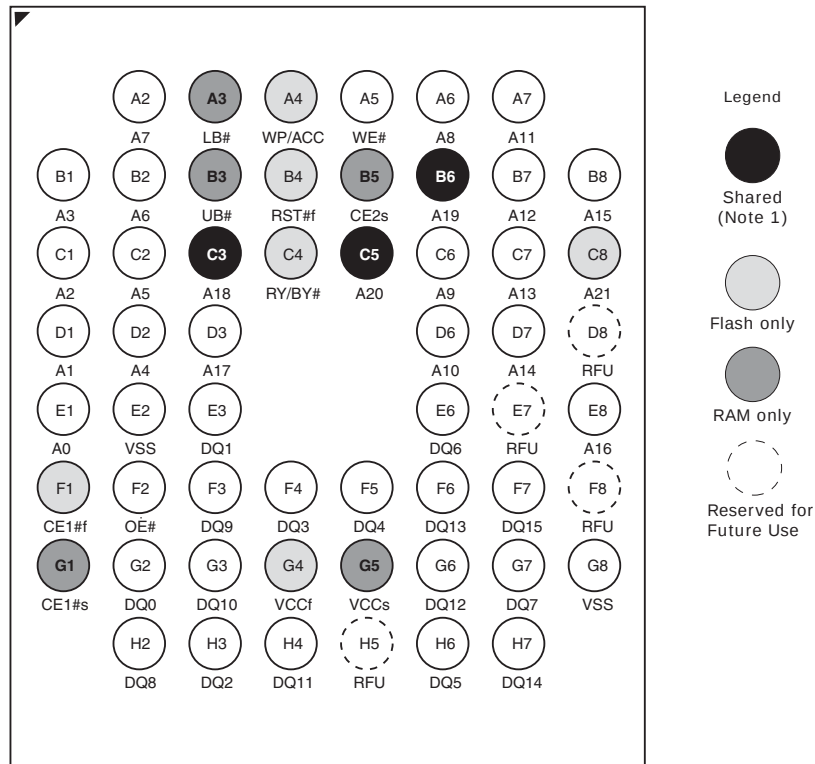
Please see the valid combinations table for the model# description.

## 2. MCP Block Diagram



### 3. Connection Diagram

**56-ball Fine-Pitch Ball Grid Array**  
(Top View, Balls Facing Down)



**Note:**

1. May be shared depending on density.

| MCP         | Flash-only Addresses | Shared Addresses |
|-------------|----------------------|------------------|
| S71GL032NA0 | A20                  | A19-A0           |
| S71GL064NB0 | A21                  | A20-A0           |

#### 3.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

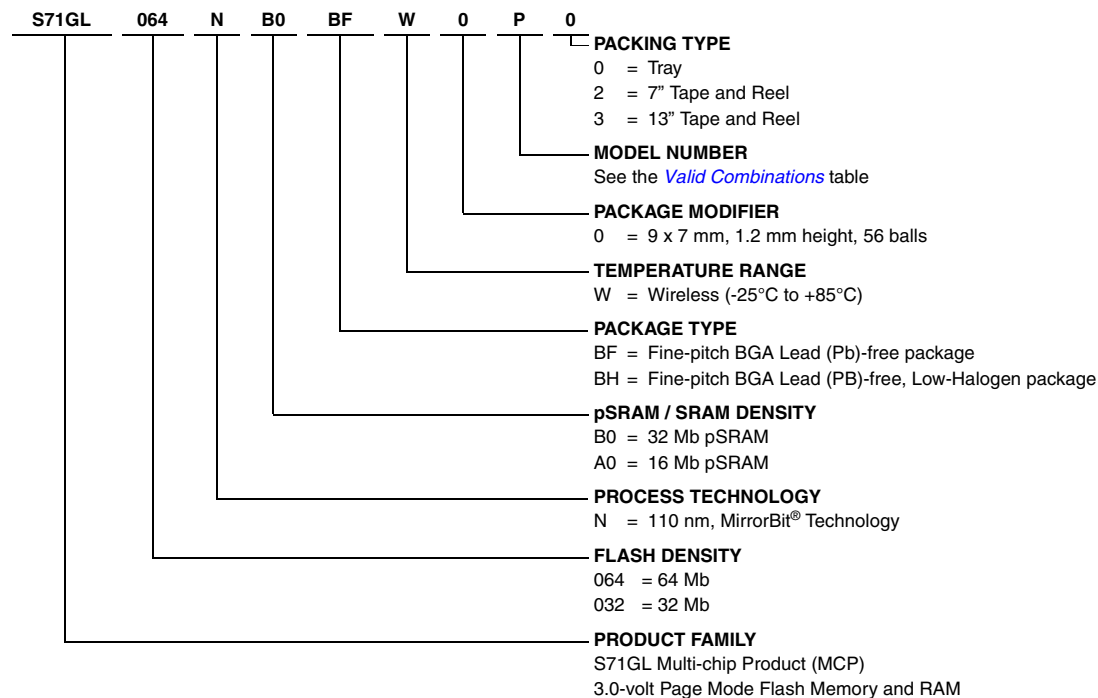
Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

## 4. Pin Description

| Pin              | Description                                                                                                                                                                                                                                       |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A21–A0           | 22 Address Inputs (Common and Flash only) (A20-A0 for the S71GL032N)                                                                                                                                                                              |
| DQ15–DQ0         | 16 Data Inputs/Outputs (Common)                                                                                                                                                                                                                   |
| CE1#f            | Chip Enable (Flash)                                                                                                                                                                                                                               |
| CE1#s            | Chip Enable 1 (pSRAM/SRAM)                                                                                                                                                                                                                        |
| CE2s             | Chip Enable 2 (pSRAM/SRAM)                                                                                                                                                                                                                        |
| OE#              | Output Enable (Common)                                                                                                                                                                                                                            |
| WE#              | Write Enable (Common)                                                                                                                                                                                                                             |
| RY/BY#           | Ready/Busy Output (Flash 1)                                                                                                                                                                                                                       |
| UB#              | Upper Byte Control (pSRAM/SRAM)                                                                                                                                                                                                                   |
| LB#              | Lower Byte Control (pSRAM/SRAM)                                                                                                                                                                                                                   |
| RESET#           | Hardware Reset Pin, Active Low (Flash)                                                                                                                                                                                                            |
| WP#/ACC          | Hardware Write Protect/Acceleration Pin (Flash)                                                                                                                                                                                                   |
| V <sub>CCf</sub> | Flash 3.0 volt-only single power supply (see <a href="#">Product Selector Guide</a> for speed options and voltage supply tolerances)                                                                                                              |
| V <sub>CCS</sub> | pSRAM/SRAM Power Supply                                                                                                                                                                                                                           |
| V <sub>SS</sub>  | Device Ground (Common)                                                                                                                                                                                                                            |
| NC               | Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). |

## 5. Ordering Information

The order number is formed by a valid combinations of the following:



### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

**Table 5.1** Valid Combinations

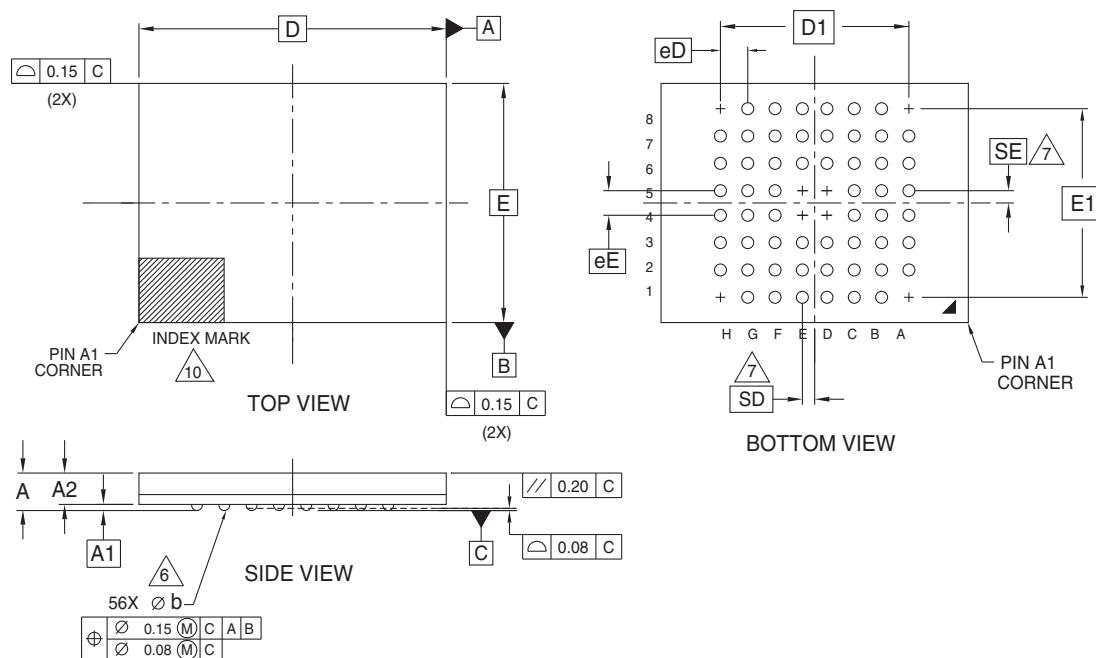
| S71GL064N Valid Combinations |                       |                               |              | Speed Options (ns)/Boot Sector Option | (p)SRAM Type/ Access Time (ns) | Package Marking |
|------------------------------|-----------------------|-------------------------------|--------------|---------------------------------------|--------------------------------|-----------------|
| Base Ordering Part Number    | Package & Temperature | Package Modifier/Model Number | Packing Type |                                       |                                |                 |
| S71GL032NA0                  | BHW                   | 0K                            | 0, 2, 3 (1)  | 90 / Bottom Boot Sector               | pSRAM 9 / 70                   | TLC056          |
|                              |                       | 0P                            |              | 90 / Top Boot Sector                  |                                |                 |
| S71GL064NB0                  | BFW, BHW              | 0K                            |              | 90 / Bottom Boot Sector               |                                |                 |
| S71GL064NB0                  |                       | 0P                            |              | 90 / Top Boot Sector                  |                                |                 |

**Note:**

1. Type 0 is standard. Specify other options as required.

## 6. Physical Dimensions

### 6.1 TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7 mm Package



|                         |                              |      |      |                          |
|-------------------------|------------------------------|------|------|--------------------------|
| PACKAGE                 | TLC 056                      |      |      |                          |
| JEDEC                   | N/A                          |      |      |                          |
| D x E                   | 9.00 mm x 7.00 mm<br>PACKAGE |      |      |                          |
| SYMBOL                  | MIN                          | NOM  | MAX  | NOTE                     |
| A                       | ---                          | ---  | 1.20 | PROFILE                  |
| A1                      | 0.20                         | ---  | ---  | BALL HEIGHT              |
| A2                      | 0.81                         | ---  | 0.97 | BODY THICKNESS           |
| D                       | 9.00 BSC.                    |      |      | BODY SIZE                |
| E                       | 7.00 BSC.                    |      |      | BODY SIZE                |
| D1                      | 5.60 BSC.                    |      |      | MATRIX FOOTPRINT         |
| E1                      | 5.60 BSC.                    |      |      | MATRIX FOOTPRINT         |
| MD                      | 8                            |      |      | MATRIX SIZE D DIRECTION  |
| ME                      | 8                            |      |      | MATRIX SIZE E DIRECTION  |
| n                       | 56                           |      |      | BALL COUNT               |
| φb                      | 0.35                         | 0.40 | 0.45 | BALL DIAMETER            |
| eE                      | 0.80 BSC.                    |      |      | BALL PITCH               |
| eD                      | 0.80 BSC                     |      |      | BALL PITCH               |
| SD / SE                 | 0.40 BSC.                    |      |      | SOLDER BALL PLACEMENT    |
| A1,A8,D4,D5,E4,E5,H1,H8 |                              |      |      | DEPOPULATED SOLDER BALLS |

#### NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
- WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- N/A
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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## 7. Revision History

| Section                               | Description                                                                                                                  |
|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| <b>Revision 01 (May 14, 2007)</b>     |                                                                                                                              |
|                                       | Initial release                                                                                                              |
| <b>Revision 02 (June 19, 2007)</b>    |                                                                                                                              |
| Global                                | Editorial changes to valid combinations table                                                                                |
| <b>Revision 03 (March 25, 2008)</b>   |                                                                                                                              |
| Ordering Information                  | Added Low-Halogen option to package type                                                                                     |
| <b>Revision 04 (October 31, 2008)</b> |                                                                                                                              |
| General Description                   | Added pSRAM Type 8, 90 nm                                                                                                    |
| Product Selector Guide                | Added pSRAM Type 8, 90 nm<br>Changed S71GL064Nxx-xx package to TSC056                                                        |
| Ordering Information                  | Changed S71GL064Nxx-xx package to TSC056                                                                                     |
| Physical Dimensions                   | Added TSC056                                                                                                                 |
| <b>Revision 05 (January 20, 2009)</b> |                                                                                                                              |
| Global                                | Added OPNs S71GL032NA0BHW0B/0F and S71GL064NA0BHW0B/0F                                                                       |
| General Description                   | Added pSRAM Type 10                                                                                                          |
| <b>Revision 06 (January 13, 2010)</b> |                                                                                                                              |
| General Description                   | Updated Table with current pSRAM offerings                                                                                   |
| Global                                | Removed pSRAM Type 7 MCPs<br>Added 32 Mb and 64 Mb pSRAM Type 9 MCPs                                                         |
| <b>Revision 07 (May 8, 2012)</b>      |                                                                                                                              |
| Global                                | Removed 4 Mb and 8 Mb pSRAM<br>Updated Document and Publication Identification Number descriptions                           |
| <b>Revision 08 (May 6, 2013)</b>      |                                                                                                                              |
| Global                                | Changed V <sub>CC</sub> Range to 2.7-3.3V<br>Removed pSRAM Type 8 and Type 10<br>Corrected Package to TLC056 for S71GL064Nxx |

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