



EMIF02-MIC03C2

2 line EMI filter and ESD protection

Main product characteristics

Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers and printers and MCU Boards

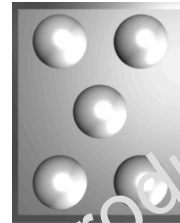
Description

The EMIF02-MIC03C2 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The Flip-Chip packaging means the package size is equal to the die size.

This filter includes ESD protection circuitry, which prevents damage to the application when it is subjected to ESD surges up to 15 kV.

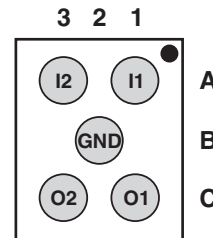
Benefits

- EMI symmetrical (I/O) low-pass filter
- High efficiency EMI filter (-35 dB @ 900 MHz)
- Very low PCB space consumption: 1.07 mm x 1.47 mm
- Very thin package: 0.695 mm
- Coating resin on back side and lead free package
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging.



Carrier Flip-Chip package
(about 20 times real size)

Pin configuration (Bump side)



Complies with following standards:

IEC 61000-4-2

level 4 input pins 15 kV (air discharge)
 8 kV (contact discharge)

level 1 output pins 2 kV (air discharge)
 2 kV (contact discharge)

MIL STD 883G - Method 3015-7 Class 3

1 Characteristics

Figure 1. Basic cell configuration

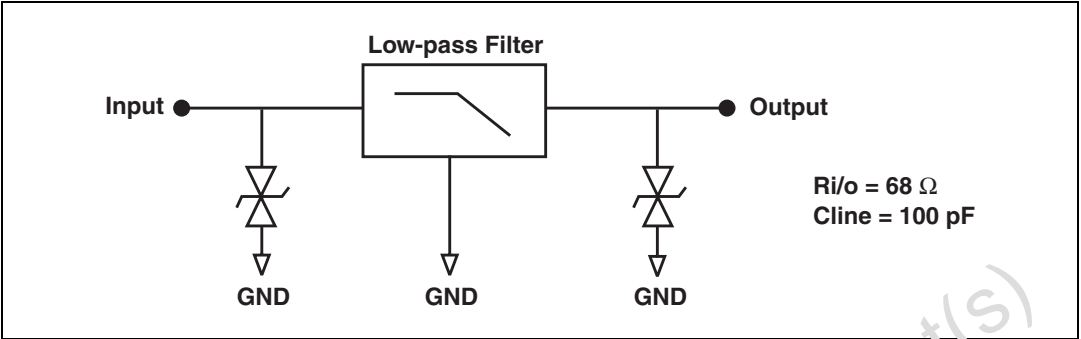


Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Table 2. Electrical characteristics ($T_{amb} = 25^\circ \text{C}$)

Symbol	Parameters	
V_{BR}	Breakdown voltage	
I_{RM}	Leakage current @ V_{RM}	
V_{RM}	Stand-off voltage	
V_{CL}	Clamping voltage	
r_d	Dynamic impedance	
I_{PP}	Peak pulse current	
$R_{I/O}$	Series resistance between input and output	
C_{line}	Input capacitance per line	

Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	$I_R = 1 \text{ mA}$	6	8		V
I_{RM}	$V_{RM} = 3 \text{ V per line}$			500	nA
$R_{I/O}$	Tolerance		68		Ω
C_{line}	$V_R = 0 \text{ V}$		100		pF

Figure 2. S21 (dB) attenuation measurement **Figure 3. Analog crosstalk measurement**

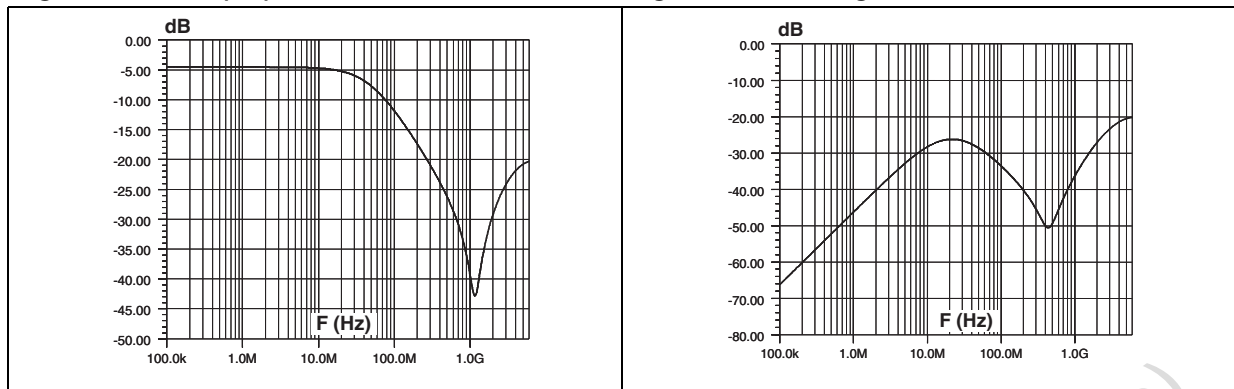


Figure 4. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input V_{in} and one output V_{out}

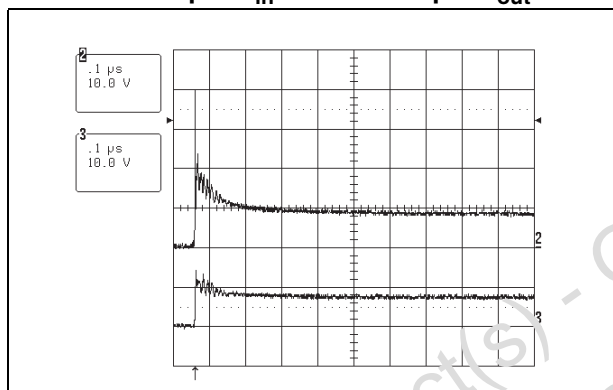


Figure 5. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input V_{in} and one output V_{out}

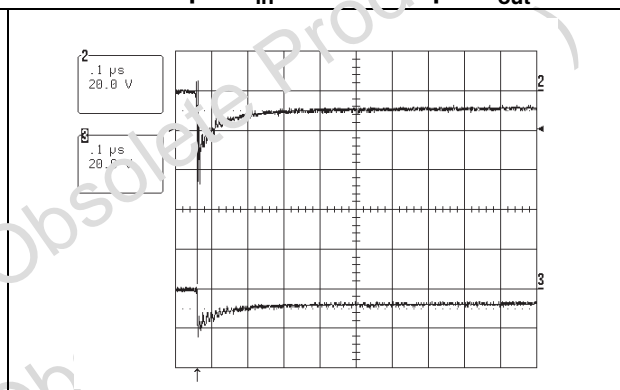


Figure 6. Line capacitance versus applied voltage

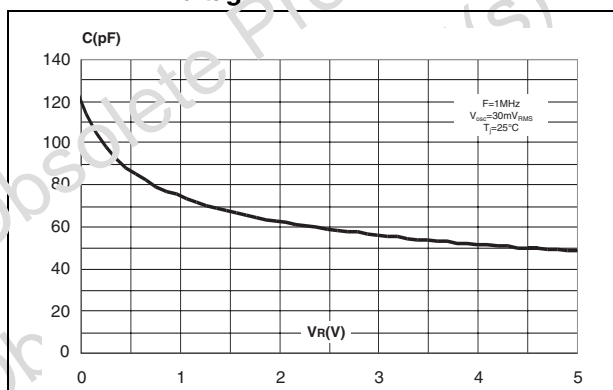


Figure 7. Aplac model

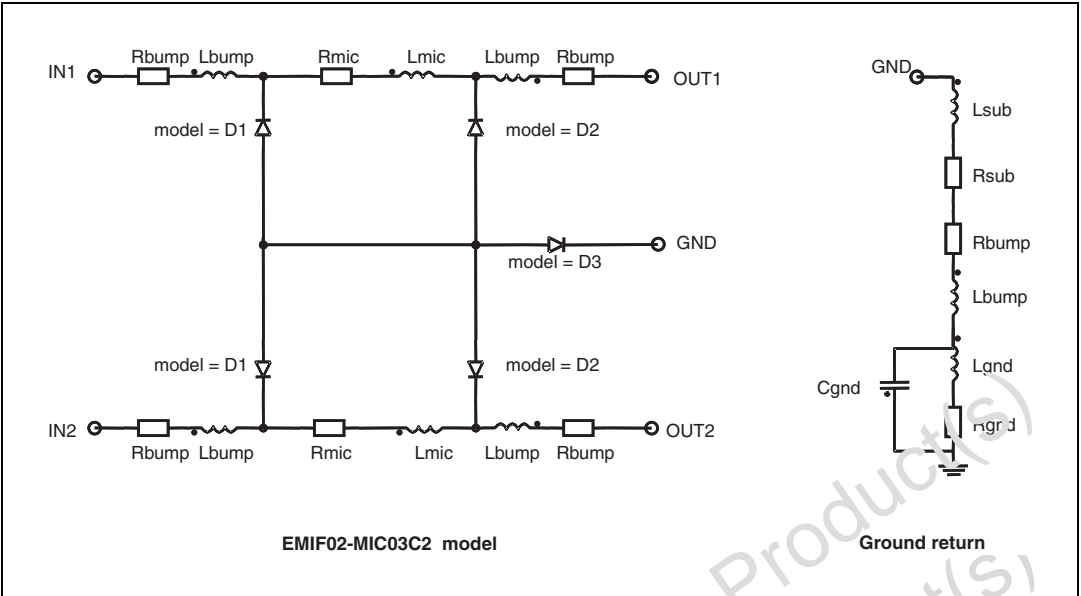
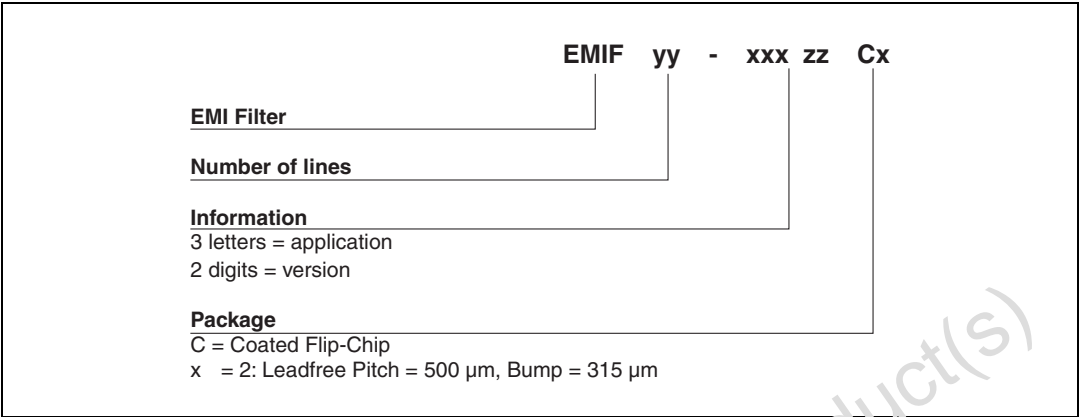


Figure 8. Aplac parameters

Model D1	Model D3	Model D2	
CJO=Cdiode1	CJO=Cdiode3	CJO=Cdiode2	aplacvar Rmic 68
BV=7	BV=7	BV=7	aplacvar Lmic 10p
IBV=1u	IBV=1u	IBV=1u	aplacvar Cdiode1 100pF
IKF=1000	IKF=1000	IKF=1000	aplacvar Cdiode2 3.6pF
IS=10f	IS=10f	IS=10f	aplacvar Cdiode3 1.17nF
ISR=100p	ISR=100p	ISR=100p	aplacvar Lbump 50pH
N=1	N=1	N=1	aplacvar Rbump 20m
M=0.3333	M=0.3333	M=0.3333	aplacvar Rsub 0.5m
RS=0.7	RS=0.12	RS=0.3	aplacvar Rgnd 10m
VJ=0.6	VJ=0.6	VJ=0.6	aplacvar Lgnd 50pH
TT=50n	TT=50n	TT=50n	aplacvar Cgnd 0.15pF
			aplacvar Lsub 10pH

2 Ordering information scheme



3 Package information

Figure 9. Flip-Chip Dimensions

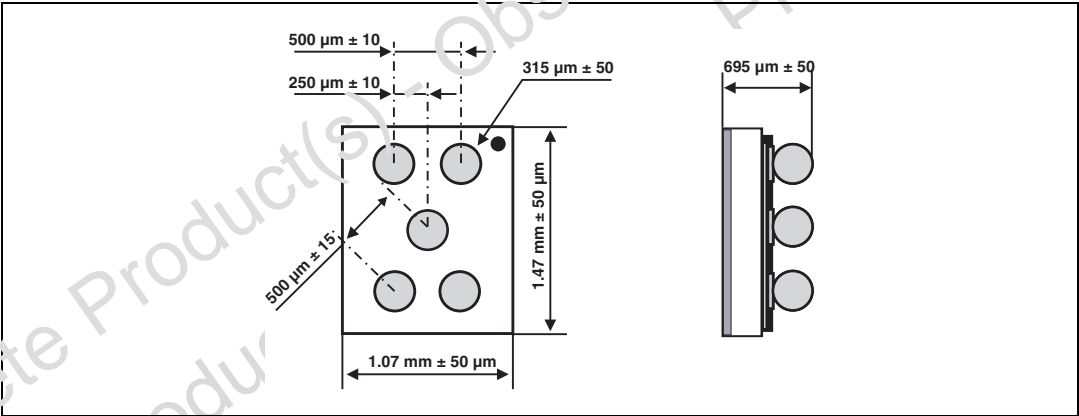


Figure 10. Marking

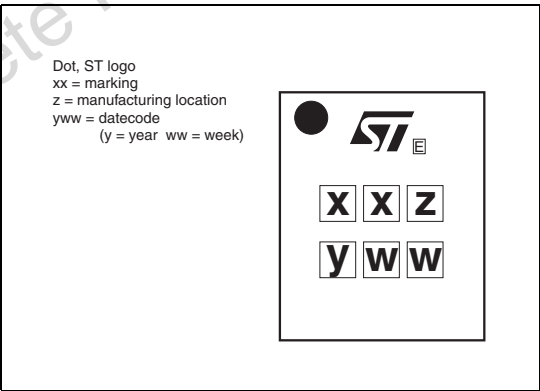
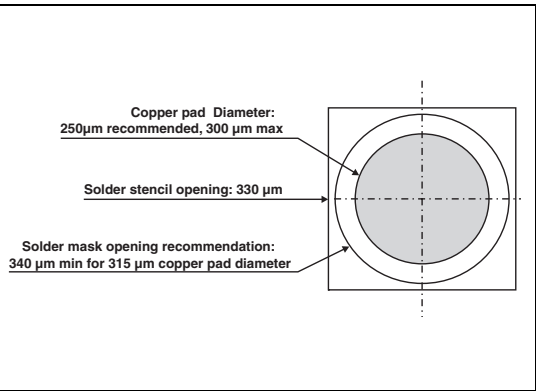


Figure 11. Footprint recommendation



Technical drawing of a 3.5mm floppy diskette showing dimensions and pin locations. The drawing includes a side view on the left and a top view on the right.

Dimensions:

- Overall width: 8 ± 0.3 mm
- Overall height: 3.5 ± 0.1 mm
- Pin pitch (center-to-center): 4 ± 0.1 mm
- Pin diameter: $\varnothing 1.5 \pm 0.1$ mm
- Distance from left edge to first pin: 0.73 ± 0.05 mm
- Distance from top edge to pin center line: 1.75 ± 0.1 mm

Pin Locations:

- Four pins are located along the top edge.
- Three pins are located along the bottom edge.
- The pins are arranged in a staggered pattern.

Labels:

- ST**: Standard Track
- xxz**: Track number
- yww**: Head number

Other Labels:

- Dot identifying Pin A1 location**: Points to the first pin on the top edge.
- User direction of unrolling**: Indicated by an arrow pointing to the right.

Dimensions in mm:

All dimensions in mm

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-MIC03C2	FW	Flip-Chip	2.3 mg	5000	7" Tape and reel

5 Revision history

Date	Revision	Changes
28-Nov-2006	1	Initial release.

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