



TS4985

2 X 1.2W Stereo Audio Power Amplifier with Dedicated Standby Pins

- Operating from $V_{CC}=2.2V$ to $5.5V$
- 1.2W output power per channel @ $V_{CC}=5V$, THD+N=1%, $R_L=8\Omega$
- 10nA standby current
- 62dB PSRR @ 217Hz with grounded inputs
- High SNR: 106dB(A) typ.
- Near zero pop & click
- Lead-free 15 bumps, flip-chip package

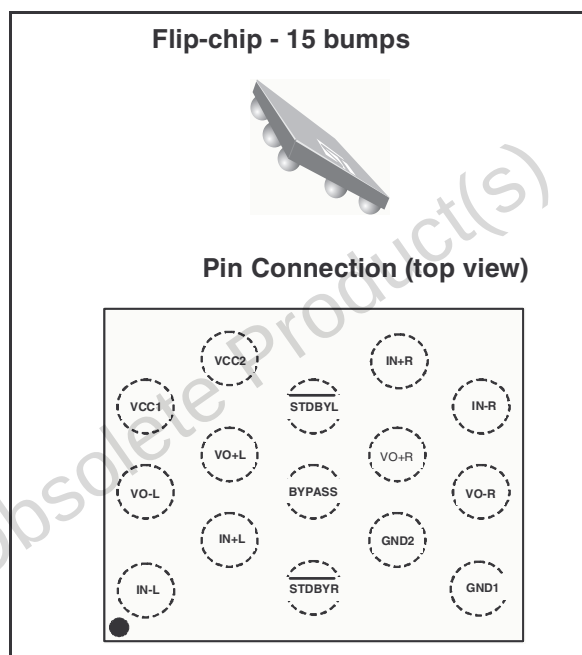
Description

The TS4985 has been designed for top-class stereo audio applications. Thanks to its compact and power-dissipation efficient flip-chip package, it suits various applications.

With a BTL configuration, this audio power amplifier is capable of delivering 1.2W per channel of continuous RMS output power into an 8Ω load @ 5V.

Each output channel (left and right), has an external controlled standby mode pin (STDBYL & STDBYR) to reduce the supply current to less than 10nA per channel. The device also features an internal thermal shutdown protection.

The gain of each channel can be configured by external gain setting resistors.



Applications

- Cellular mobile phones
- Notebook & PDA computers
- LCD monitors & TVs
- Portable audio devices

Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TS4985EIJT	-40, +85°C	Lead free flip-chip	Tape & Reel	A85
TS4985EKIJT		Lead free flip-chip + back coating		

1 Typical Application Schematic

Figure 1 shows a typical application schematic for the TS4985.

Figure 1. Application schematic

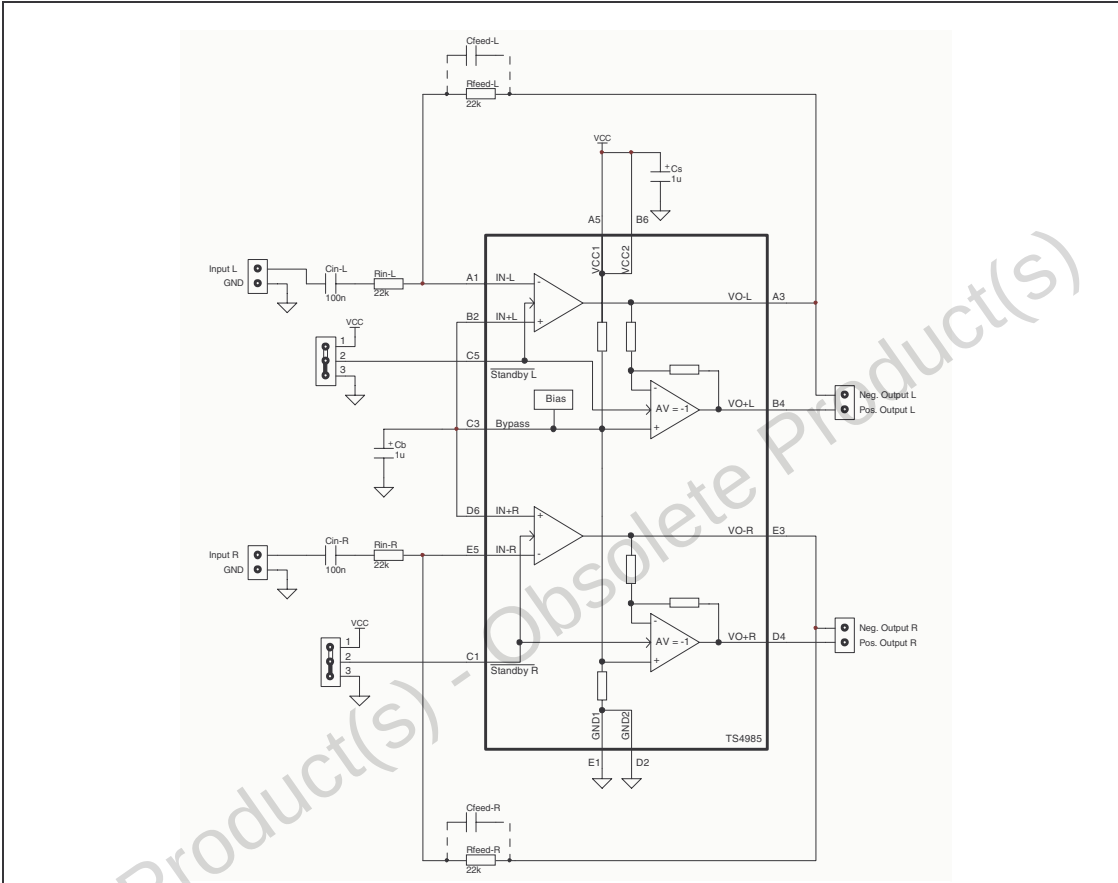


Table 1. External component descriptions

Components	Functional Description
$R_{IN\ L,R}$	Inverting input resistors which sets the closed loop gain in conjunction with R_{FEED} . These resistors also form a high pass filter with C_{IN} ($f_c = 1 / (2 \times \pi \times R_{IN} \times C_{IN})$)
$C_{IN\ L,R}$	Input coupling capacitors which blocks the DC voltage at the amplifier input terminal
$R_{FEED\ L,R}$	Feedback resistors which sets the closed loop gain in conjunction with R_{IN}
C_S	Supply Bypass capacitor which provides power supply filtering
C_B	Bypass pin capacitor which provides half supply filtering
$A_{V\ L, R}$	Closed loop gain in BTL configuration = $2 \times (R_{FEED} / R_{IN})$ on each channel

2 Absolute Maximum Ratings

Table 2. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage ⁽¹⁾	6	V
V _i	Input Voltage ⁽²⁾	G _{ND} to V _{CC}	V
T _{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T _{stg}	Storage Temperature	-65 to +150	°C
T _j	Maximum Junction Temperature	150	°C
R _{thja}	Flip-chip Thermal Resistance Junction to Ambient	180	°C/W
P _d	Power Dissipation	Internally Limited	
ESD	Human Body Model ⁽³⁾	2	kV
ESD	Machine Model	200	V
	Latch-up Immunity	200	mA

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V
3. All voltage values are measured from each pin with respect to supplies.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	2.2 to 5.5	V
V _{ICM}	Common Mode Input Voltage Range	1.2V to V _{CC}	V
VSTB	Standby Voltage Input: Device ON Device OFF	$1.35 \leq V_{STB} \leq V_{CC}$ $GND \leq V_{STB} \leq 0.4$	V
RL	Load Resistor	≥ 4	Ω
ROUTGND	Resistor Output to GND (V _{STB} = GND)	≥ 1	MΩ
TSD	Thermal Shutdown Temperature	150	°C
RTHJA	Flip-chip Thermal Resistance Junction to Ambient ⁽¹⁾	110	°C/W

1. When mounted on a 4-layer PCB.

3 Electrical Characteristics

Table 4. $V_{CC} = +5V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		7.4	12	mA
$I_{STANDBY}$	Standby Current ⁽¹⁾ No input signal, $V_{stdby} = G_{ND}$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		1	10	mV
P_o	Output Power THD = 1% Max, $F = 1kHz$, $R_L = 8\Omega$	0.9	1.2		W
THD + N	Total Harmonic Distortion + Noise $P_o = 1W_{rms}$, $A_v = 2$, $20Hz \leq F \leq 20kHz$, $R_L = 8\Omega$		0.2		%
PSRR	Power Supply Rejection Ratio ⁽²⁾ $R_L = 8\Omega$, $A_v = 2$, $V_{ripple} = 200mV_{pp}$, Input Grounded $F = 217Hz$ $F = 1kHz$	55 55	62 64		dB
Crosstalk	Channel Separation, $R_L = 8\Omega$ $F = 1kHz$ $F = 20Hz$ to $20kHz$		-107 -82		dB
T_{WU}	Wake-Up Time ($C_b = 1\mu F$)		90	130	ms
T_{STDB}	Standby Time ($C_b = 1\mu F$)		10		μs
V_{STDBH}	Standby Voltage Level High			1.3	V
V_{STDBL}	Standby Voltage Level Low			0.4	V
Φ_M	Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$		65		Degrees
GM	Gain Margin $R_L = 8\Omega$, $C_L = 500pF$		15		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		1.5		MHz

1. Standby mode is activated when V_{stdby} is tied to Gnd .

2. All PSRR data limits are guaranteed by production sampling tests.
Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. V_{ripple} is the sinusoidal signal superimposed upon V_{cc}

Table 5. $V_{CC} = +3.3V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6.6	12	mA
$I_{STANDBY}$	Standby Current ⁽¹⁾ No input signal, $V_{stdby} = G_{ND}$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		1	10	mV
P_O	Output Power THD = 1% Max, $F = 1kHz$, $R_L = 8\Omega$	375	500		mW
THD + N	Total Harmonic Distortion + Noise $P_O = 400mW_{rms}$, $A_v = 2$, $20Hz \leq F \leq 20kHz$, $R_L = 8\Omega$		0.1		%
PSRR	Power Supply Rejection Ratio ⁽²⁾ $R_L = 8\Omega$, $A_v = 2$, $V_{ripple} = 200mV_{pp}$, Input Grounded $F = 217Hz$ $F = 1kHz$	55 55	61 63		dB
Crosstalk	Channel Separation, $R_L = 8\Omega$ $F = 1kHz$ $F = 20Hz$ to $20kHz$		-107 -82		dB
T_{WU}	Wake-Up Time ($C_b = 1\mu F$)		110	140	ms
T_{STDB}	Standby Time ($C_b = 1\mu F$)		10		μs
V_{STDBH}	Standby Voltage Level High			1.2	V
V_{STDBL}	Standby Voltage Level Low			0.4	V
Φ_M	Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$		65		Degrees
GM	Gain Margin $R_L = 8\Omega$, $C_L = 500pF$		15		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		1.5		MHz
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1. Standby mode is activated when V_{stdby} is tied to Gnd .
2. All PSRR data limits are guaranteed by production sampling tests.
Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. V_{ripple} is the sinusoidal signal superimposed upon V_{CC}

Table 6. $V_{CC} = +2.6V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6.2	12	mA
$I_{STANDBY}$	Standby Current ⁽¹⁾ No input signal, $V_{stdby} = G_{ND}$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		1	10	mV
P_o	Output Power THD = 1% Max, $F = 1kHz$, $R_L = 8\Omega$	220	300		mW
THD + N	Total Harmonic Distortion + Noise $P_o = 200mW_{rms}$, $A_v = 2$, $20Hz \leq F \leq 20kHz$, $R_L = 8\Omega$		0.1		%
PSRR	Power Supply Rejection Ratio ⁽²⁾ $R_L = 8\Omega$, $A_v = 2$, $V_{ripple} = 200mV_{pp}$, Input Grounded $F = 217Hz$ $F = 1kHz$	55 55	60 62		dB
Crosstalk	Channel Separation, $R_L = 8\Omega$ $F = 1kHz$ $F = 20Hz$ to $20kHz$		-107 -82		dB
T_{WU}	Wake-Up Time ($C_b = 1\mu F$)		125	150	ms
T_{STDB}	Standby Time ($C_b = 1\mu F$)		10		μs
V_{STDBH}	Standby Voltage Level High			1.2	V
V_{STDBL}	Standby Voltage Level Low			0.4	V
Φ_M	Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$		65		Degrees
GM	Gain Margin $R_L = 8\Omega$, $C_L = 500pF$		15		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		1.5		MHz

1. Standby mode is activated when V_{stdby} is tied to Gnd .

2. All PSRR data limits are guaranteed by production sampling tests.
Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is the sinusoidal signal superimposed upon V_{cc}

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Figure 2. Open loop frequency response

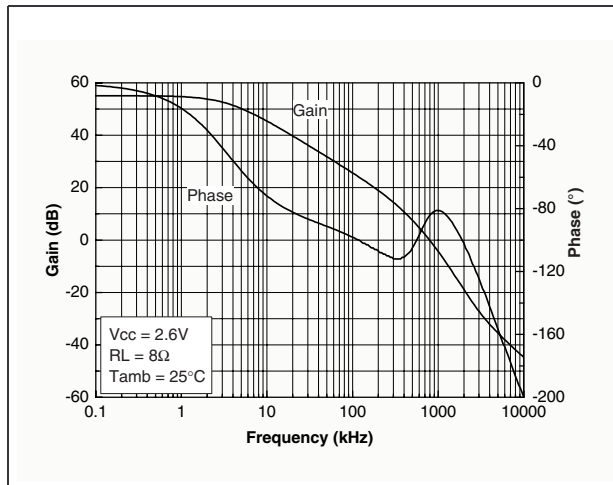


Figure 3. Open loop frequency response

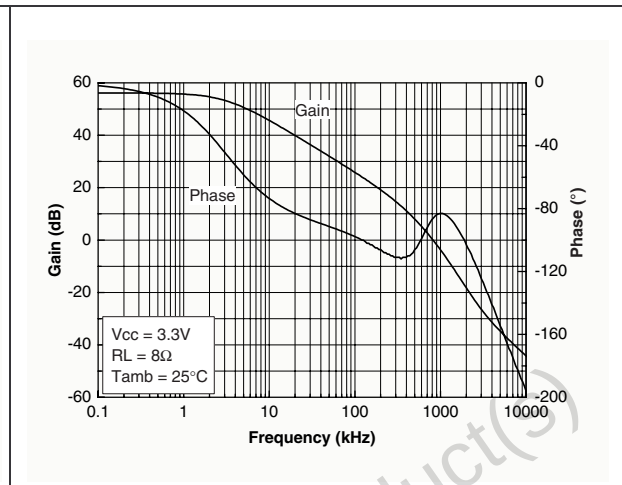


Figure 4. Open loop frequency response

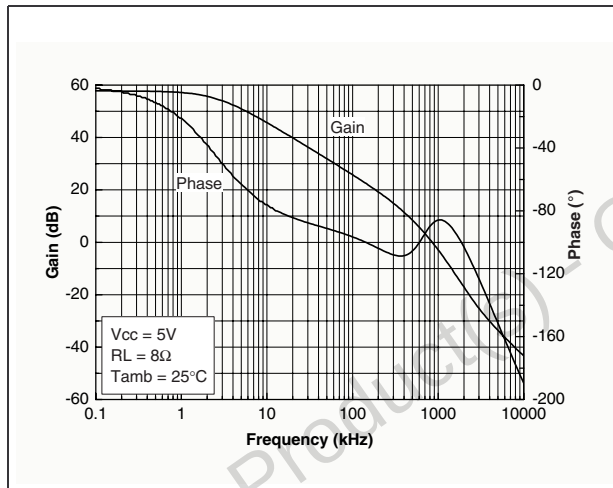


Figure 5. Open loop frequency response

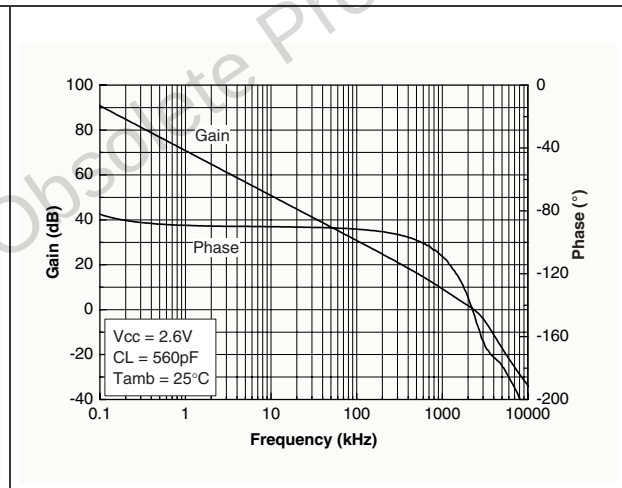


Figure 6. Open loop frequency response

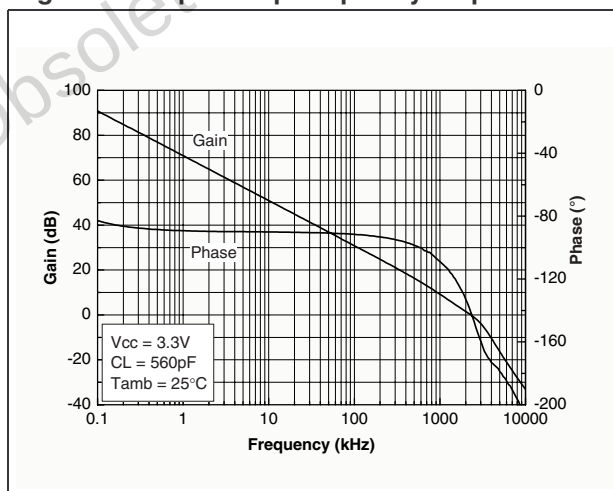


Figure 7. Open loop frequency response

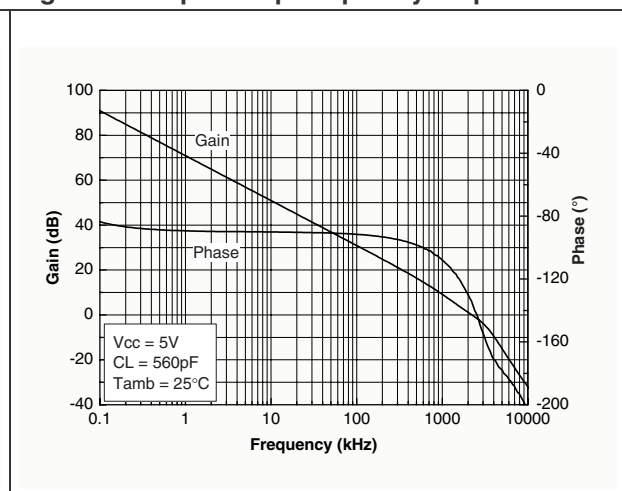


Figure 8. Power supply rejection ratio (PSRR) vs. frequency **Figure 9. Power supply rejection ratio (PSRR) vs. frequency**

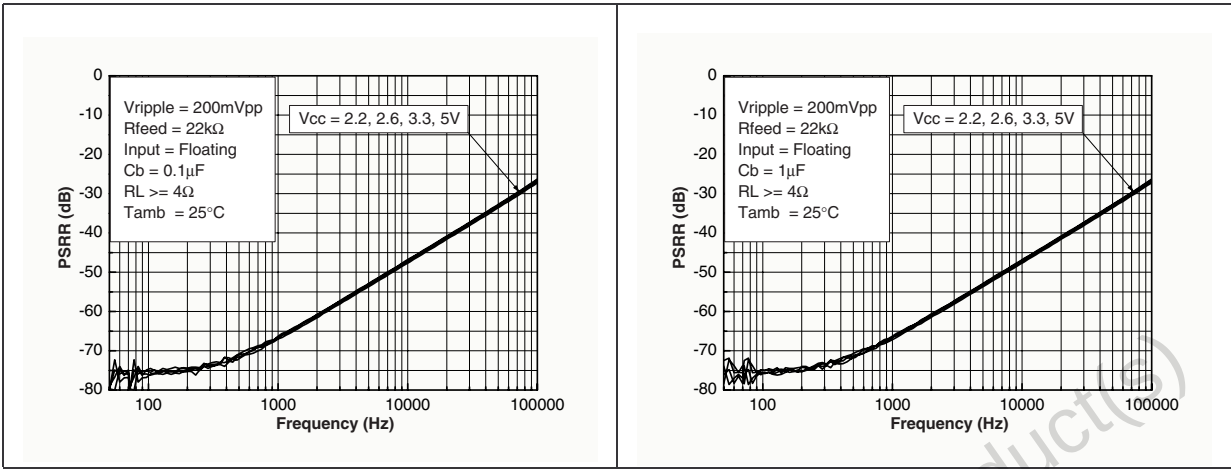


Figure 10. Power supply rejection ratio (PSRR) vs. frequency **Figure 11. Power supply rejection ratio (PSRR) vs. frequency**

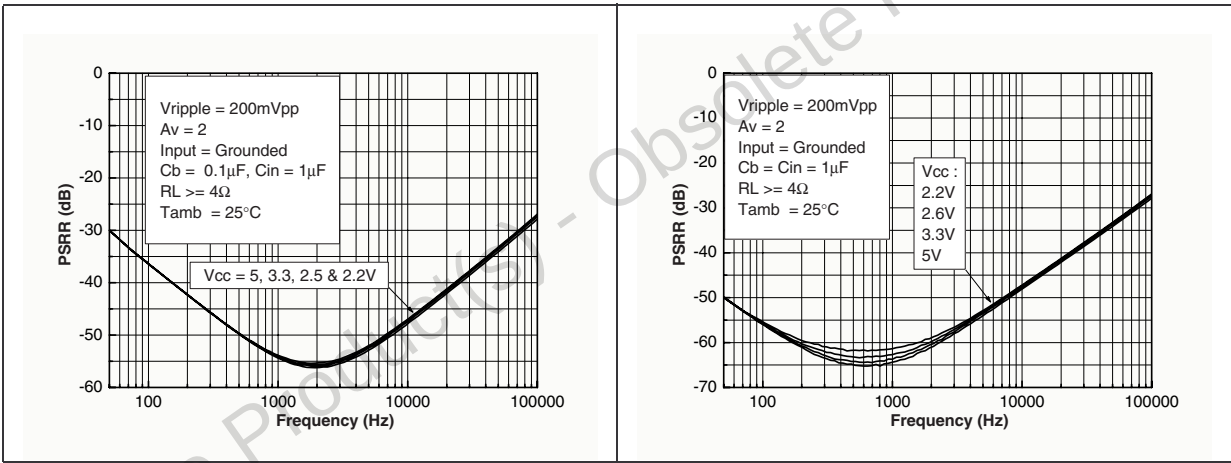


Figure 12. Power supply rejection ratio (PSRR) vs. frequency **Figure 13. Power supply rejection ratio (PSRR) vs. frequency**

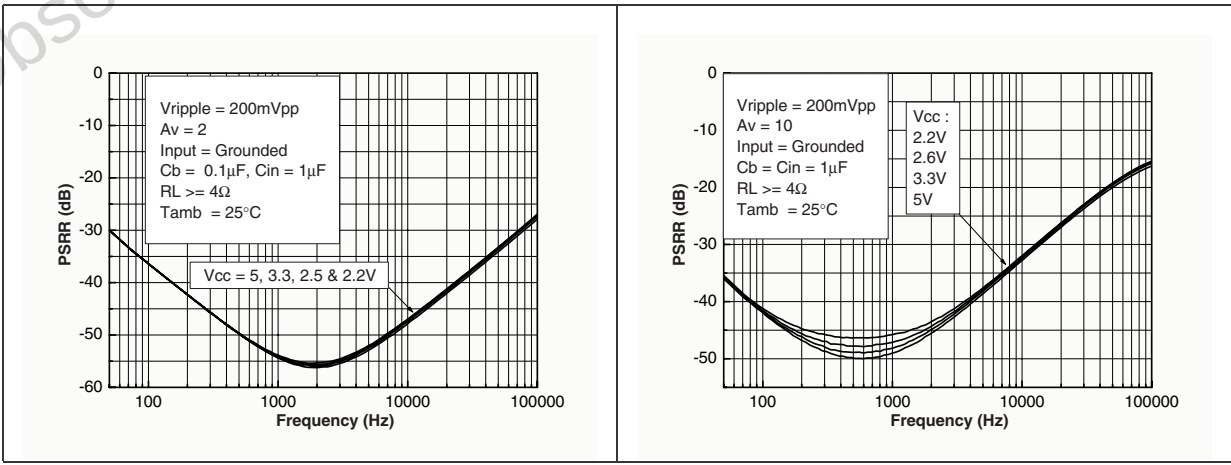


Figure 14. Power supply rejection ratio (PSRR) vs. DC output voltage

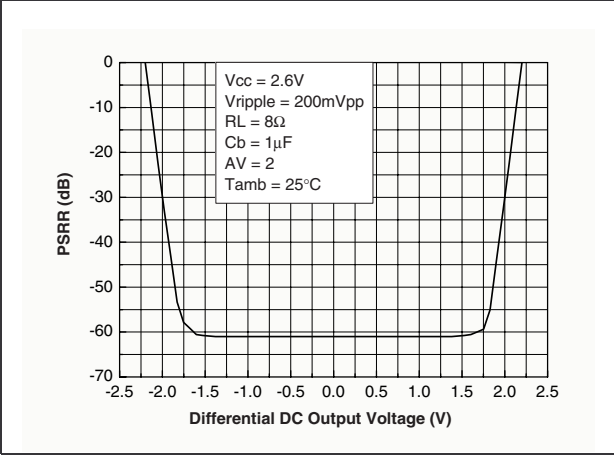


Figure 15. Power supply rejection ratio (PSRR) vs. DC output voltage

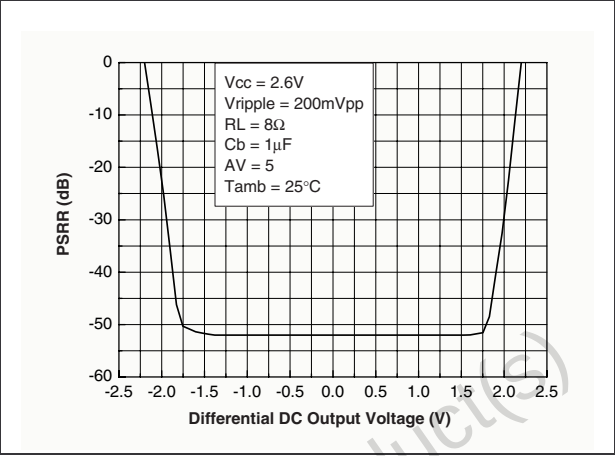


Figure 16. Power supply rejection ratio (PSRR) vs. DC output voltage

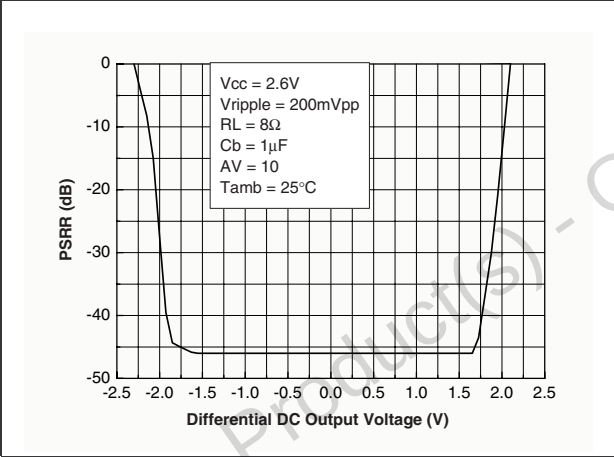


Figure 17. Power supply rejection ratio (PSRR) vs. DC output voltage

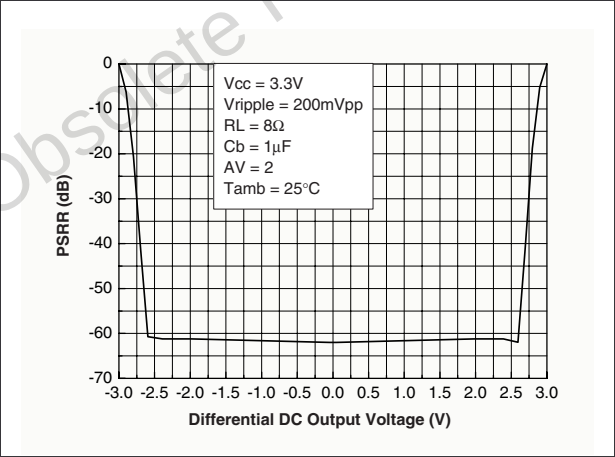


Figure 18. Power supply rejection ratio (PSRR) vs. DC output voltage

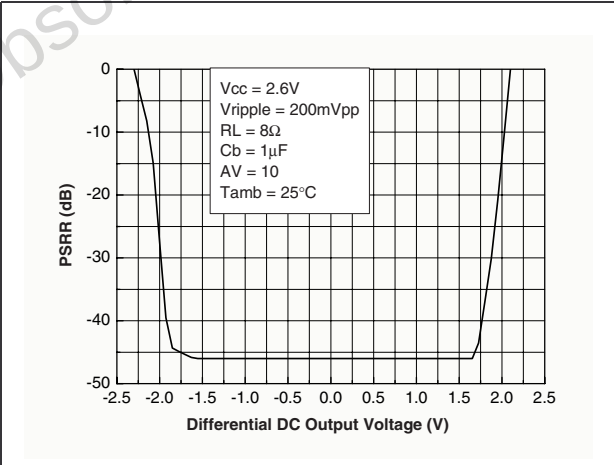


Figure 19. Power supply rejection ratio (PSRR) vs. DC output voltage

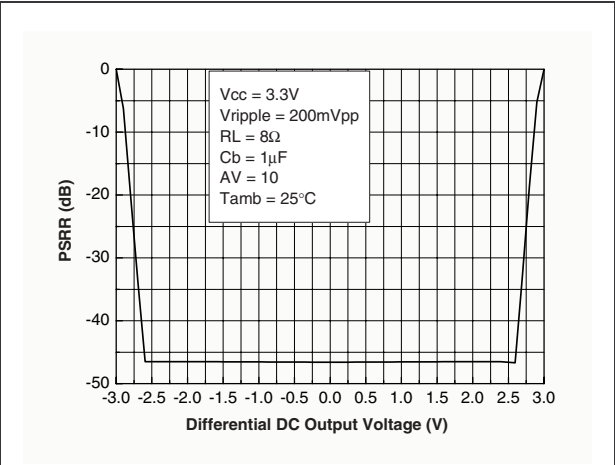


Figure 20. Power supply rejection ratio (PSRR) vs. DC output voltage **Figure 21. Power supply rejection ratio (PSRR) vs. DC output voltage**

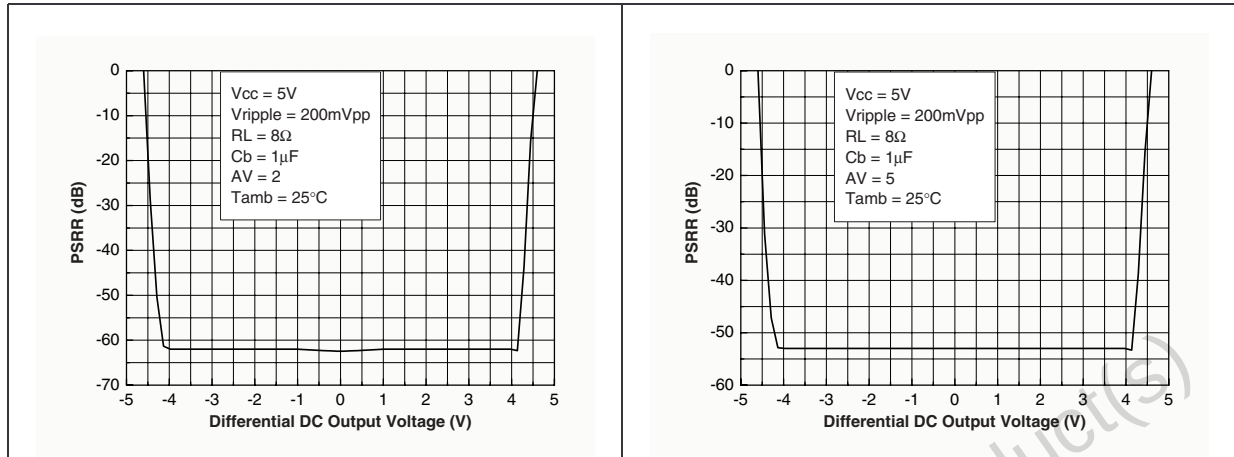


Figure 22. Power supply rejection ratio (PSRR) vs. DC output voltage **Figure 23. Power supply rejection ratio (PSRR) at $f=217Hz$ vs. bypass capacitor**

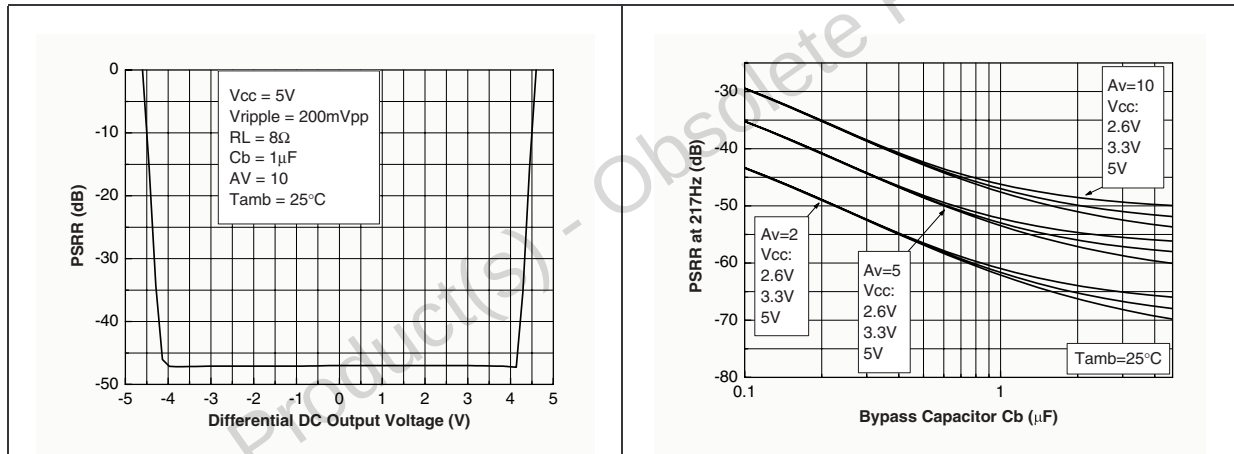


Figure 24. Output power vs. power supply voltage

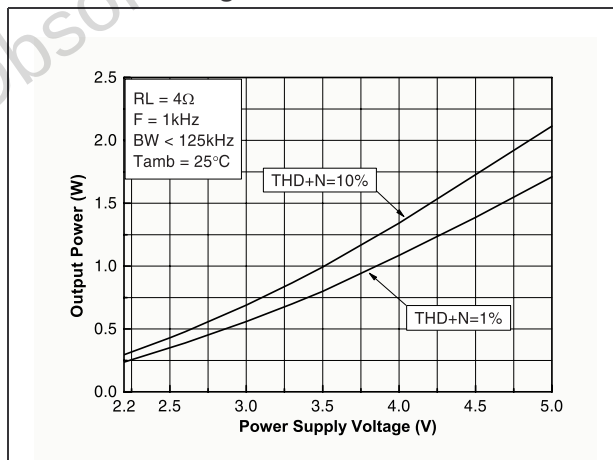


Figure 25. Output power vs. power supply voltage

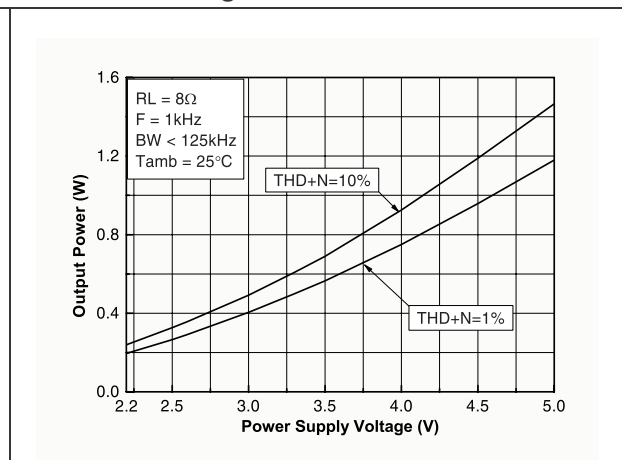


Figure 26. Output power vs. power supply voltage

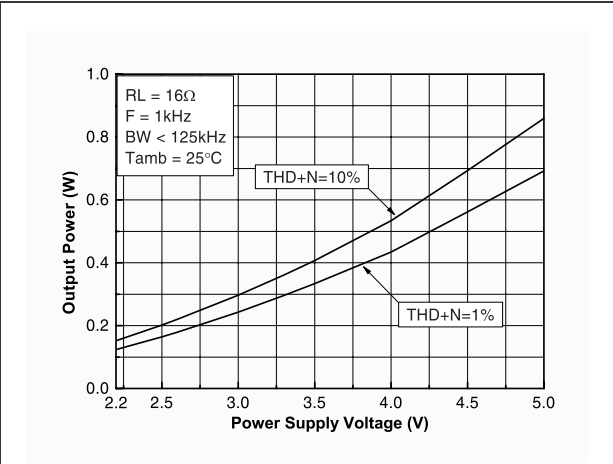


Figure 27. Output power vs. load resistor

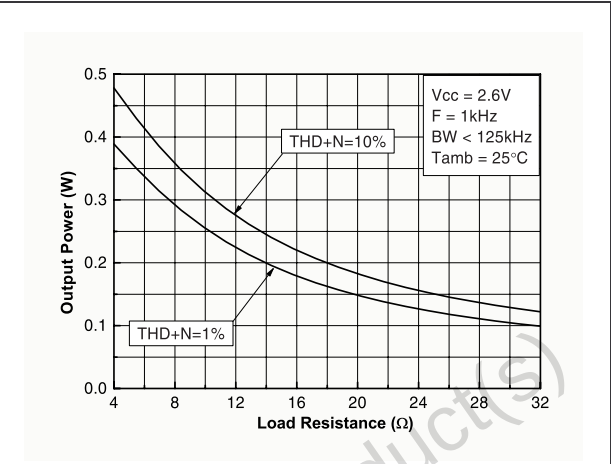


Figure 28. Output power vs. load resistor

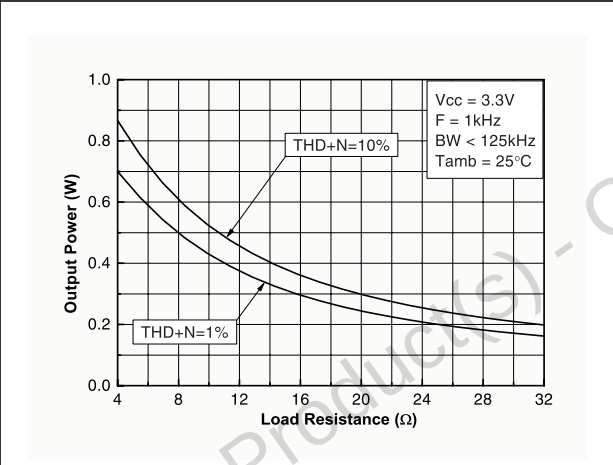


Figure 29. Output power vs. load resistor

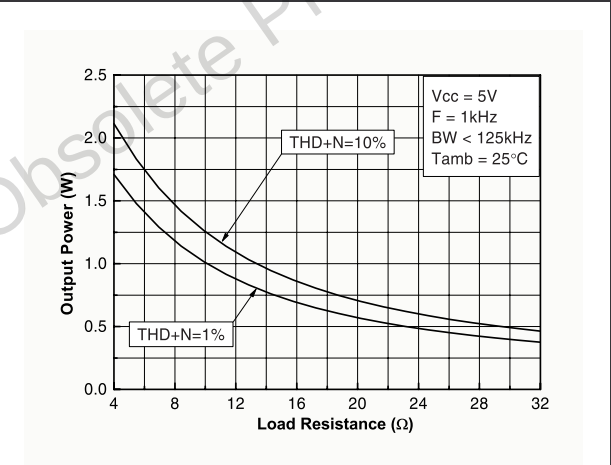


Figure 30. Power dissipation vs. output power per channel

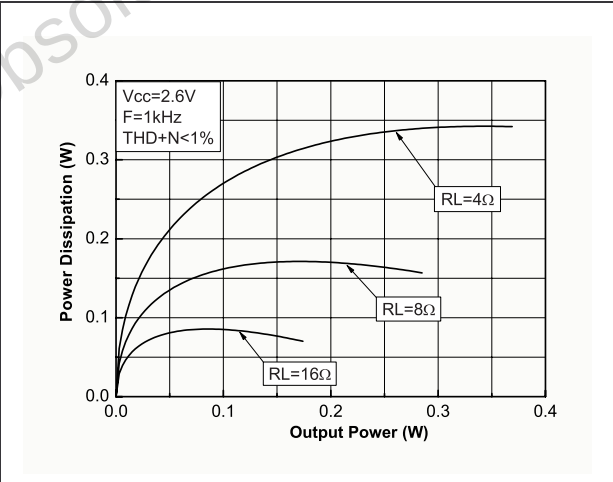


Figure 31. Power dissipation vs. output power per channel

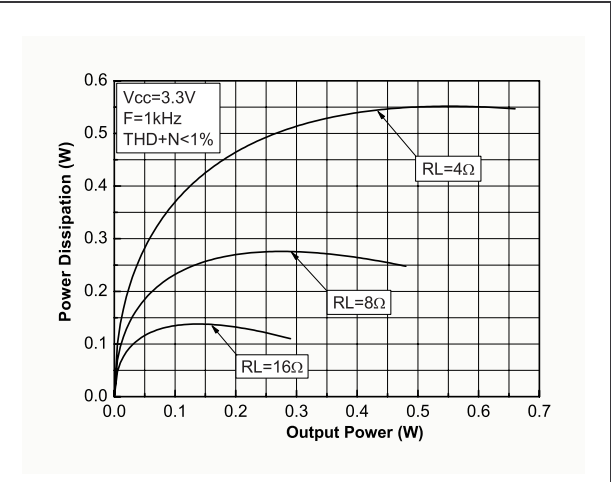


Figure 32. Power dissipation vs. output power per channel

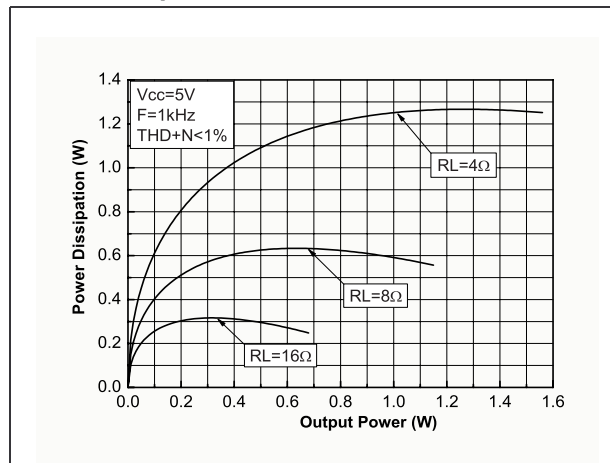


Figure 33. Clipping voltage vs. power supply voltage and load resistor

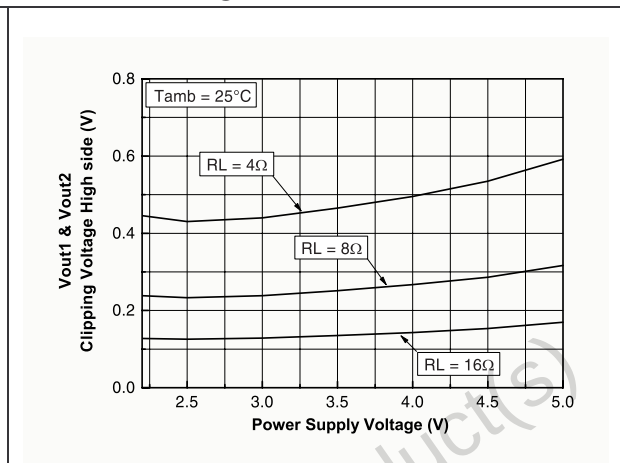


Figure 34. Clipping voltage vs. power supply voltage and load resistor

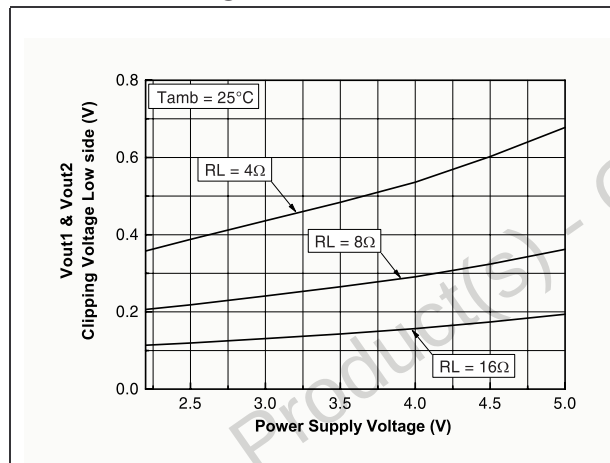


Figure 35. Current consumption vs. power supply voltage

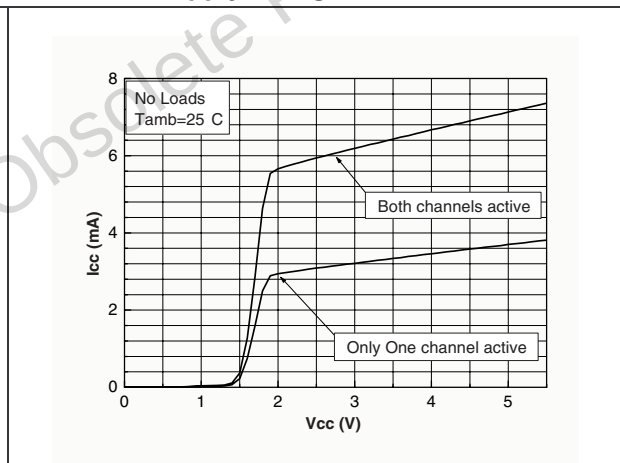


Figure 36. Current consumption vs. power supply voltage

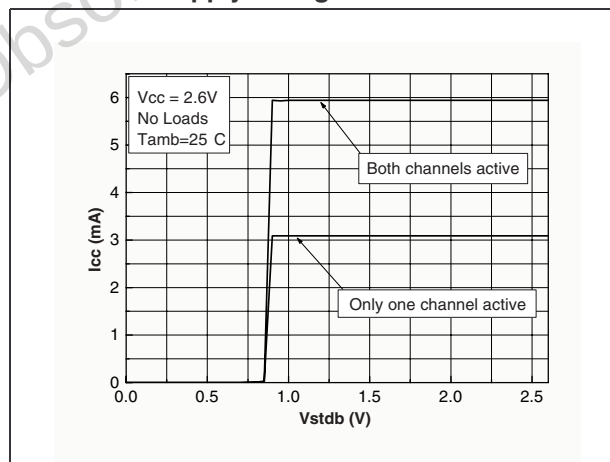


Figure 37. Current consumption vs. standby voltage

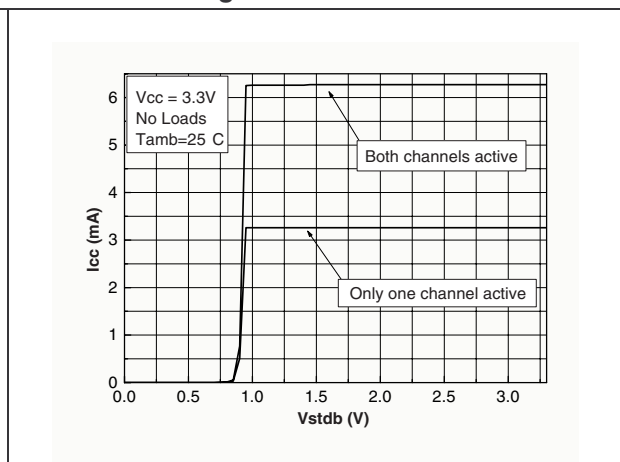


Figure 38. Current consumption vs. standby voltage

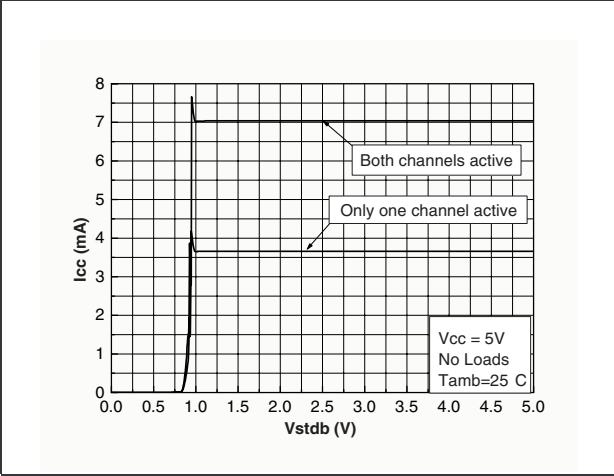


Figure 39. Output noise voltage device ON

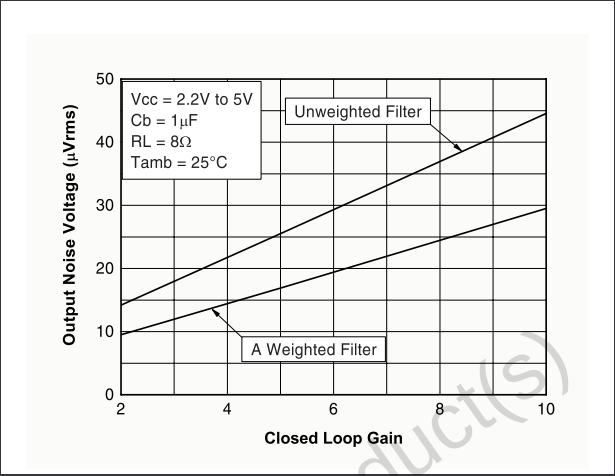


Figure 40. Output noise voltage device in Standby

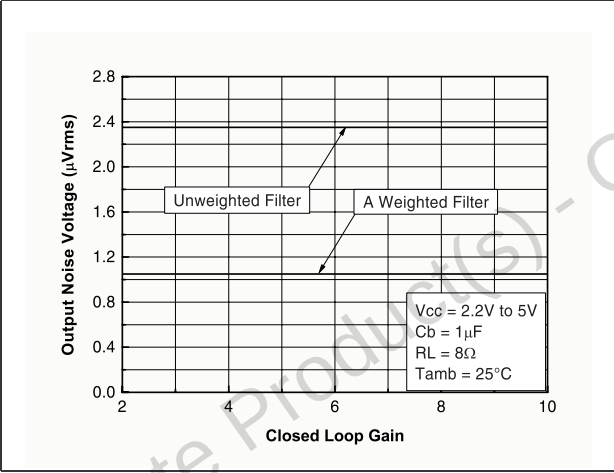


Figure 41. THD + N vs. output power

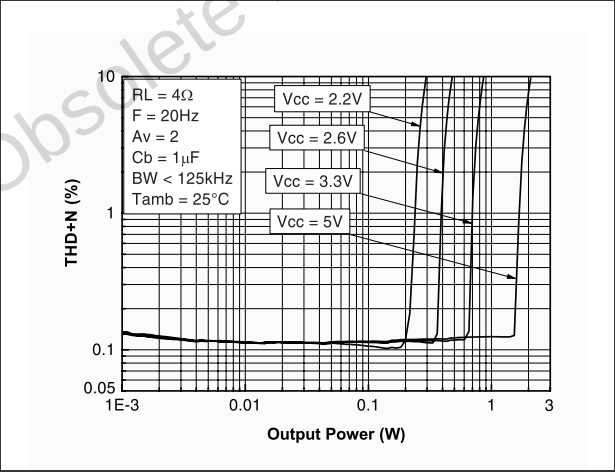


Figure 42. THD + N vs. output power

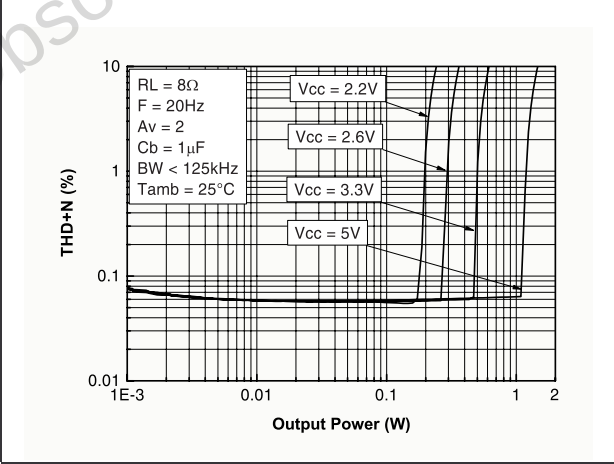


Figure 43. THD + N vs. output power

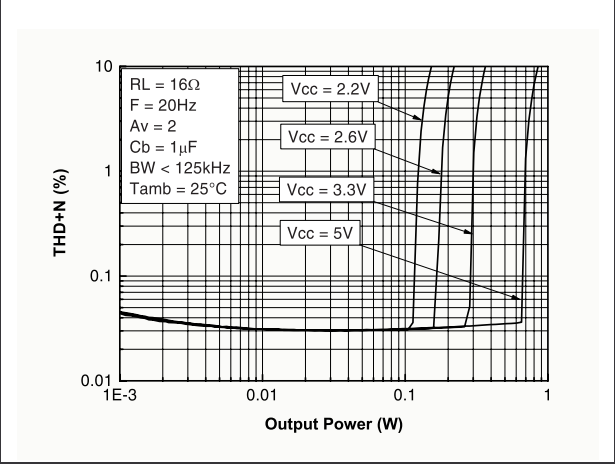


Figure 44. THD + N vs. output power

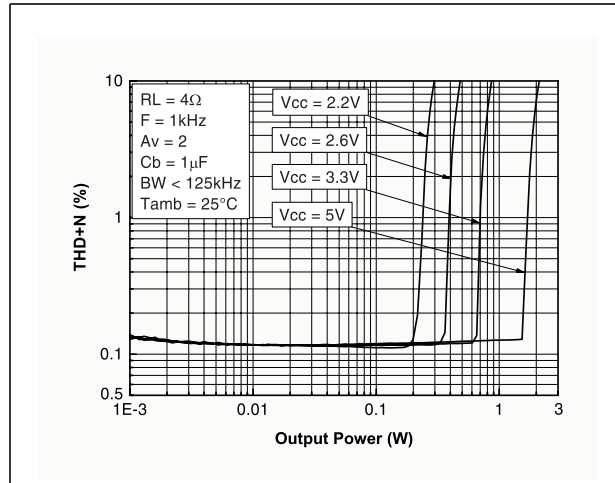


Figure 45. THD + N vs. output power

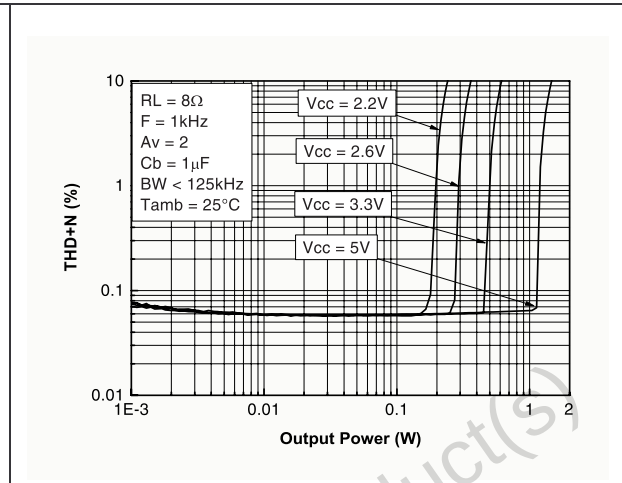


Figure 46. THD + N vs. output power

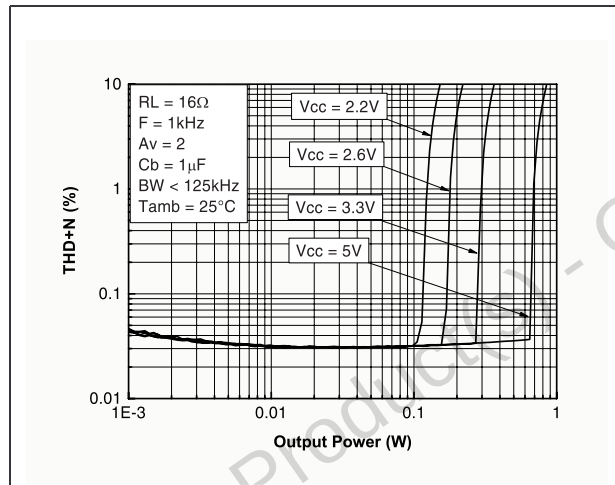


Figure 47. THD + N vs. output power

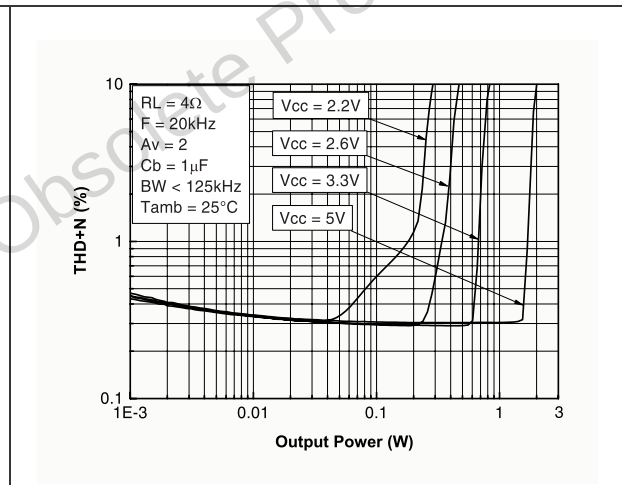


Figure 48. THD + N vs. output power

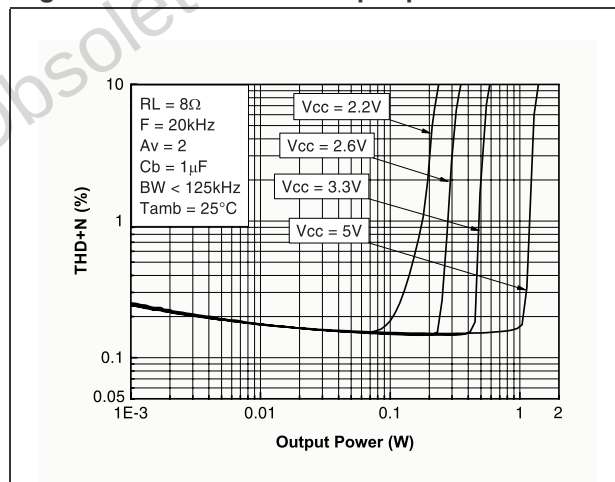


Figure 49. THD + N vs. output power

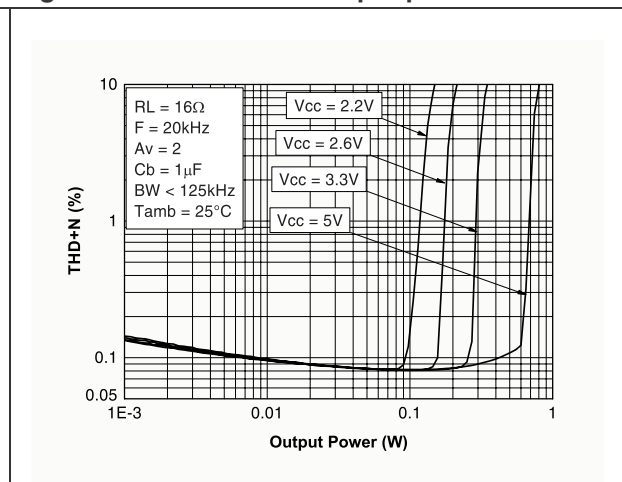


Figure 50. THD + N vs. frequency

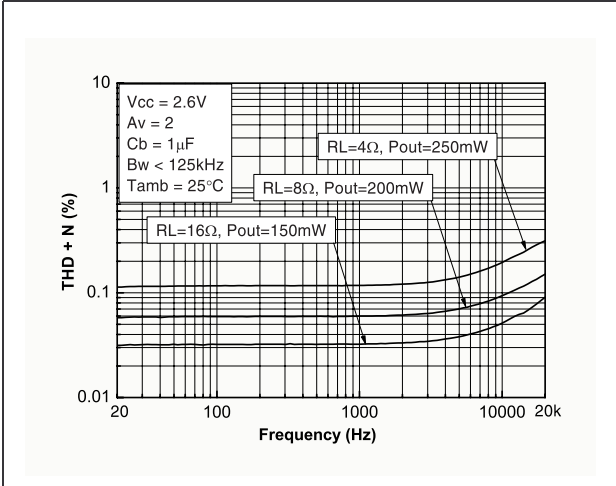


Figure 51. THD + N vs. frequency

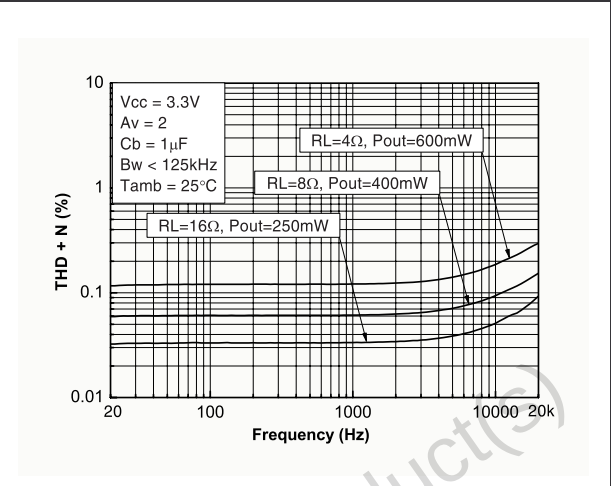


Figure 52. THD + N vs. frequency

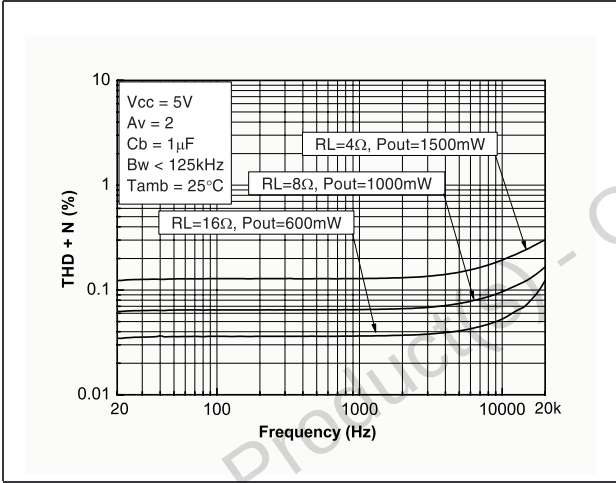


Figure 53. Crosstalk vs. frequency

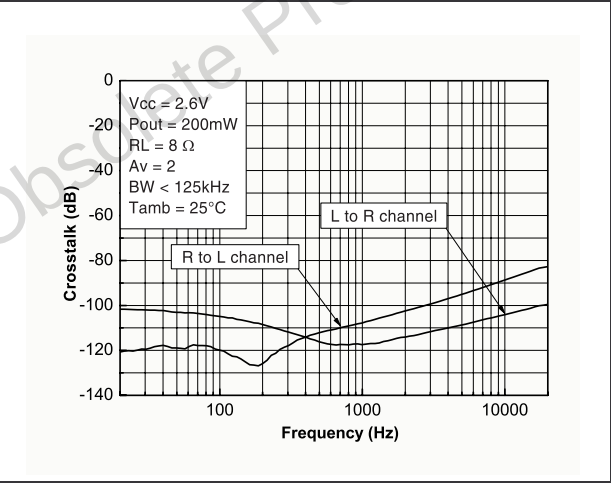


Figure 54. Crosstalk vs. frequency

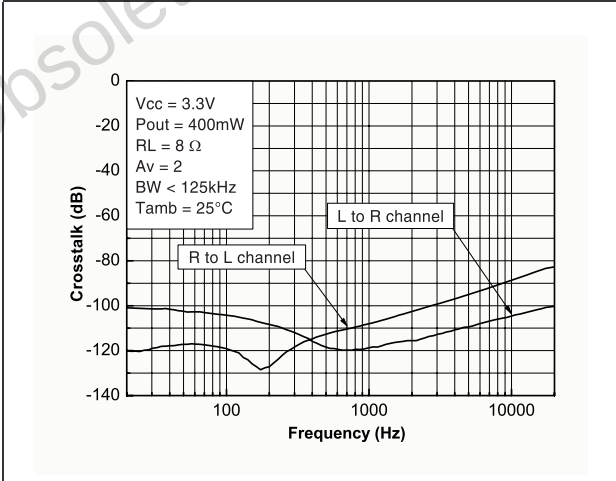


Figure 55. Crosstalk vs. frequency

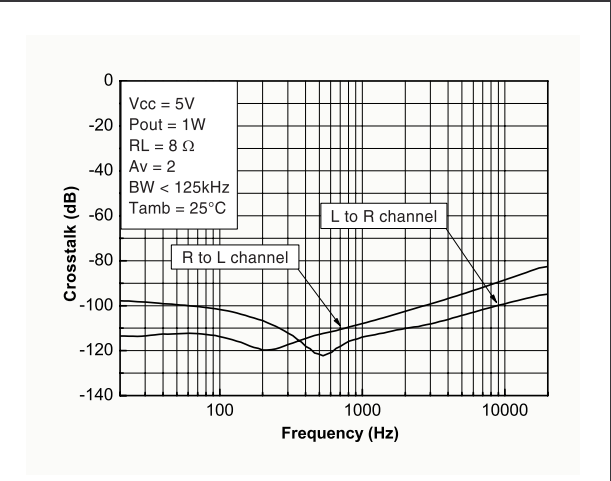


Figure 56. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

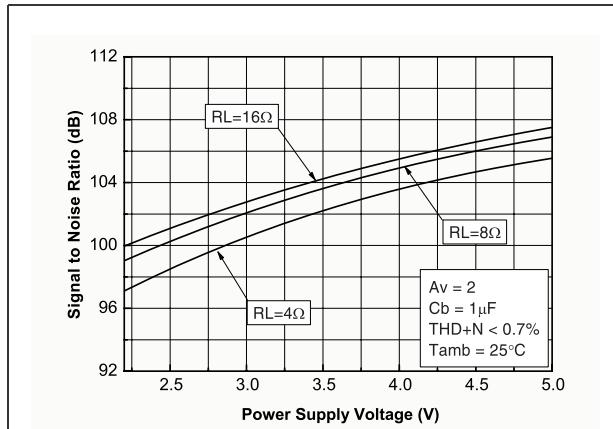


Figure 57. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

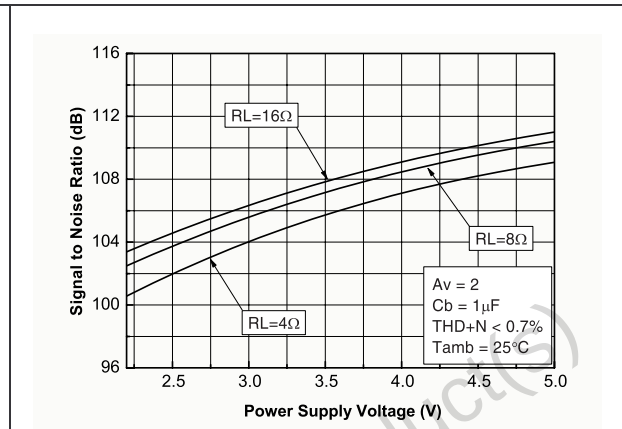


Figure 58. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

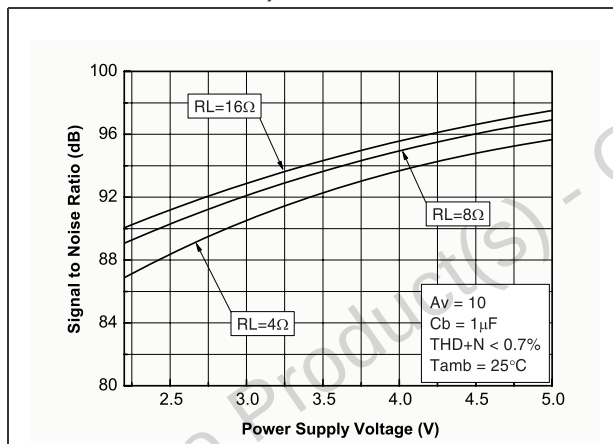


Figure 59. Signal to noise ratio vs. power supply with A weighted filter (20Hz to 20kHz)

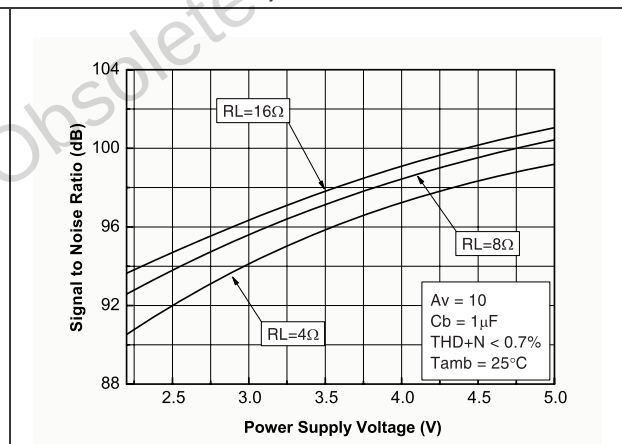
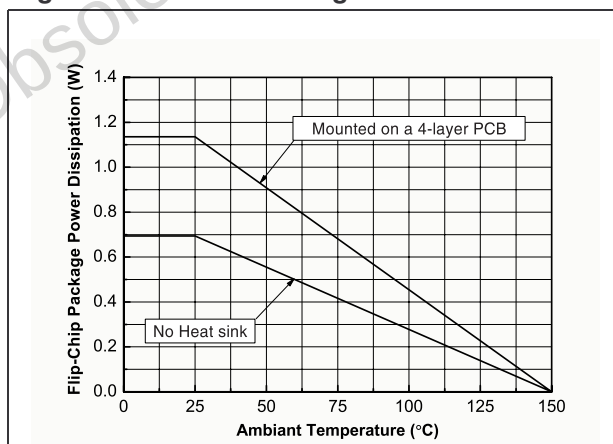


Figure 60. Power derating curves



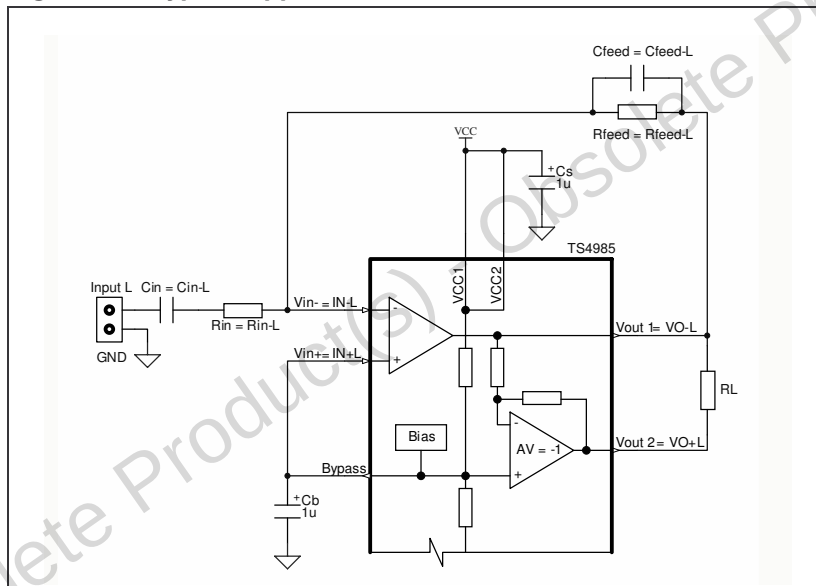
4 Application Information

The TS4985 integrates two monolithic power amplifiers with a BTL (Bridge Tied Load) output type (explained in more detail in [Section 4.1](#)). For this discussion, only the left-channel amplifier will be referred to.

Referring to the schematic in [Figure 61](#), we assign the following variables and values:

$$\begin{aligned} V_{in} &= IN-L \\ V_{out1} &= VO-L \\ V_{out2} &= VO+R \\ R_{in} &= Rin-L, \\ R_{feed} &= Rfeed-L \\ C_{feed} &= Cfeed-L \end{aligned}$$

Figure 61. Typical application schematic - left channel



4.1 BTL configuration principle

BTL (Bridge Tied Load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

$$\text{Single-ended output 1} = V_{out1} = V_{out} \text{ (V)},$$

$$\text{Single-ended output 2} = V_{out2} = -V_{out} \text{ (V)}, \quad V_{out1} - V_{out2} = 2V_{out} \text{ (V)}$$

The output power is:

$$P_{out} = \frac{(2V_{outRMS})^2}{R_L}$$

For the same power supply voltage, the output power in a BTL configuration is four times higher than the output power in a single-ended configuration.

4.2 Gain in typical application schematic

The typical application schematic (*Figure 61*) is shown on *page 18*.

In the flat region (no C_{in} effect), the output voltage of the first stage is:

$$V_{out1} = (-V_{in}) \frac{R_{feed}}{R_{in}} \quad (V)$$

For the second stage: $V_{out2} = -V_{out1}$ (V)

The differential output voltage is:

$$V_{out2} - V_{out1} = 2V_{in} \frac{R_{feed}}{R_{in}} \quad (V)$$

The differential gain, referred to as G_V for greater convenience, is:

$$G_V = \frac{V_{out2} - V_{out1}}{V_{in}} = 2 \frac{R_{feed}}{R_{in}}$$

V_{out2} is in phase with V_{in} and V_{out1} is phased 180° with V_{in} . This means that the positive terminal of the loudspeaker should be connected to V_{out2} and the negative to V_{out1} .

4.3 Low and high frequency response

In the low frequency region, C_{in} starts to have an effect. C_{in} forms with R_{in} a high-pass filter with a -3dB cut-off frequency:

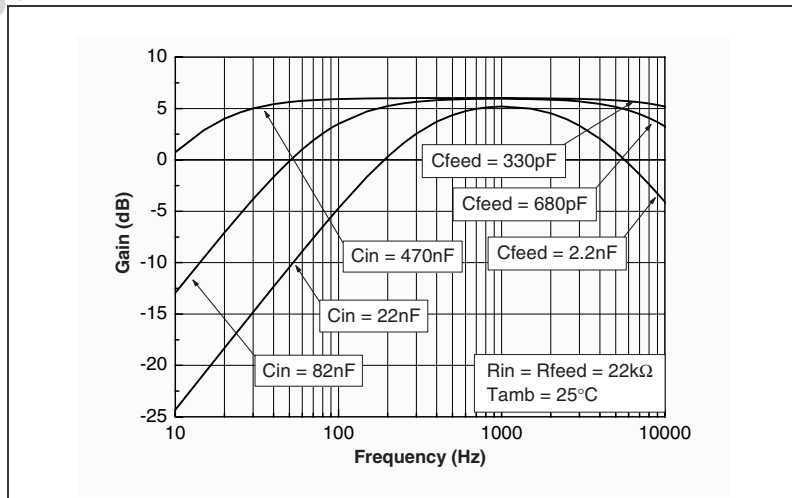
$$F_{CL} = \frac{1}{2\pi R_{in} C_{in}} \quad (Hz)$$

In the high frequency region, you can limit the bandwidth by adding a capacitor (C_{feed}) in parallel with R_{feed} . It forms a low-pass filter with a -3dB cut-off frequency. F_{CH} is in Hz.

$$F_{CH} = \frac{1}{2\pi R_{feed} C_{feed}} \quad (Hz)$$

The following graph (*Figure 62*) shows an example of C_{in} and C_{feed} influence.

Figure 62. Frequency response gain versus C_{in} & C_{feed}



4.4 Power dissipation and efficiency

Hypotheses:

- Voltage and current in the load are sinusoidal (V_{out} and I_{out}).
- Supply voltage is a pure DC source (V_{CC}).

Regarding the load we have:

$$V_{out} = V_{PEAK} \sin \omega t \quad (V)$$

and

$$I_{out} = \frac{V_{out}}{R_L} \quad (A)$$

and

$$P_{out} = \frac{V_{PEAK}^2}{2R_L} \quad (W)$$

Therefore, the average current delivered by the supply voltage is:

$$I_{CCAVG} = 2 \frac{V_{PEAK}}{\pi R_L} \quad (A)$$

The power delivered by the supply voltage is:

$$P_{supply} = V_{CC} \cdot I_{CCAVG} \quad (W)$$

Then, the **power dissipated by each amplifier** is:

$$P_{diss} = P_{supply} - P_{out} \quad (W)$$

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}} \cdot \sqrt{P_{out}} - P_{out} \quad (W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{out}} = 0$$

and its value is:

$$P_{dissmax} = \frac{2V_{CC}^2}{\pi^2 R_L} \quad (W)$$

Note: This maximum value is only depending on power supply voltage and load values.

The **efficiency**, η , is the ratio between the output power and the power supply:

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when $V_{PEAK} = V_{CC}$, so that:

$$\frac{\pi}{4} = 78.5\%$$

The TS4985 has two independent power amplifiers, and each amplifier produces heat due to its power dissipation. Therefore, the maximum die temperature is the sum of the each amplifier's maximum power dissipation. It is calculated as follows:

$P_{diss L}$ = Power dissipation due to the left channel power amplifier

$P_{diss R}$ = Power dissipation due to the right channel power amplifier

$Total P_{diss} = P_{diss L} + P_{diss R}$ (W)

In most cases, $P_{diss L} = P_{diss R}$, giving:

$$Total P_{diss} = 2P_{dissL} \quad (W)$$

or, stated differently:

$$Total P_{diss} = \frac{4\sqrt{2}V_{CC}}{\pi\sqrt{R_L}} \sqrt{P_{out}} - 2P_{out} \quad (W)$$

4.5 Decoupling the circuit

Two capacitors are needed to correctly bypass the TS4985. A power supply bypass capacitor C_S and a bias voltage bypass capacitor C_B .

C_S has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for C_S of 1μF, you can expect similar THD+N performances to those shown in the datasheet. For example:

- In the high frequency region, if C_S is lower than 1μF, it increases THD+N and disturbances on the power supply rail are less filtered.
- On the other hand, if C_S is higher than 1μF, those disturbances on the power supply rail are more filtered.

C_B has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region), in the following manner:

- If C_B is lower than 1μF, THD+N increases at lower frequencies and PSRR worsens.
- If C_B is higher than 1μF, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

Note that C_{in} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{in} , the higher the PSRR.

4.6 Wake-up time, T_{WU}

When the standby is released to put the device ON, the bypass capacitor C_b will not be charged immediately. As C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage is called wake-up time or T_{WU} and specified in electrical characteristics table with $C_b = 1\mu F$.

If C_b has a value other than 1μF, please refer to the graph in [Figure 63](#) to establish the wake-up time value.

Due to process tolerances, the maximum value of wake-up time could be established by the graph in [Figure 64](#).

Figure 63. Typical wake-up time vs. C_b

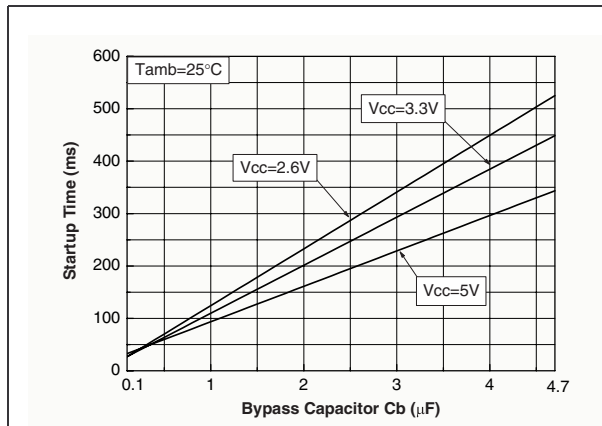
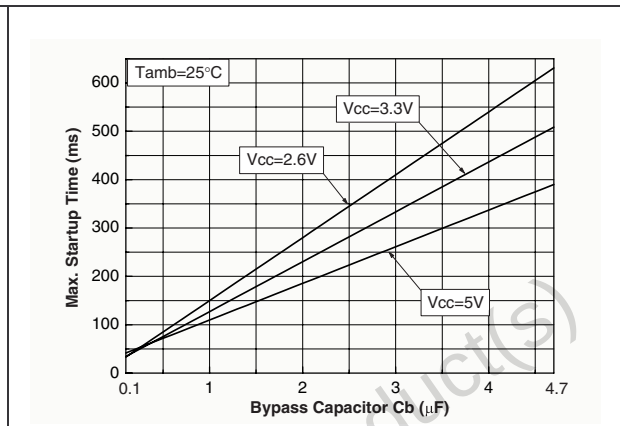


Figure 64. Maximum wake-up time vs. C_b



Note: Bypass capacitor C_b as also a tolerance of typically $\pm 20\%$. To calculate the wake-up time with this tolerance, refer to the previous graph (considering for example for $C_b = 1\mu F$ in the range of $0.8\mu F \leq 1\mu F \leq 1.2\mu F$).

4.7 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

Note: In shutdown mode, Bypass pin and Vin- pin are short-circuited to ground by internal switches. This allows for the quick discharge of the C_b and C_{in} capacitors.

4.8 Pop performance

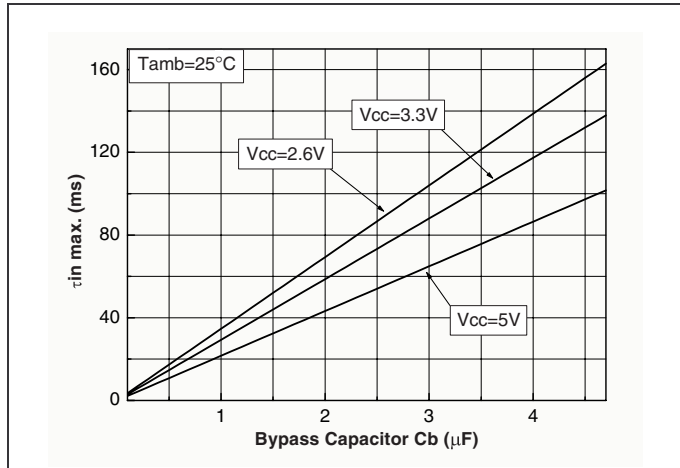
Pop performance is intimately linked with the size of the input capacitor C_{in} and the bias voltage bypass capacitor C_b .

The size of C_{in} is dependent on the lower cut-off frequency and PSRR values requested. The size of C_b is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover, C_b determines the speed with which the amplifier turns ON. In order to reach near zero pop and click, the equivalent input constant time is:

$$\tau_{in} = (R_{in} + 2k\Omega) \times C_{in} \text{ (s) with } R_{in} \geq 5k\Omega$$

must not reach the τ_{in} maximum value as indicated in the graph below in [Figure 65](#).

Figure 65. τ_{in} max. versus bypass capacitor

By following previous rules, the TS4985 can reach near zero pop and click even with high gains such as 20dB.

Example calculation:

With $R_{in} = 22k\Omega$ and a 20Hz, -3db low cut-off frequency, $C_{in} = 361nF$. So, $C_{in} = 390nF$ with standard value which gives a lower cut-off frequency equal to 18.5Hz. In this case, $(R_{in} + 2k\Omega) \times C_{in} = 9.36ms$. When referring to the previous graph, if $C_b = 1\mu F$ and $V_{cc} = 5V$, we read 20ms max. This value is twice as high as our current value, thus we can state that pop and click will be reduced to its lowest value. Minimizing both C_{in} and the gain benefits both the pop phenomena, and the cost and size of the application.

4.9 Dedicated standby control

TS4985 has two standby control inputs to allow to put each channel in standby mode independently. In case a channel is active and another one in standby mode it's very important to be in line with a following recommendation to reach near zero pop. When left (right) channel is active and right (left) channel is in standby mode it's necessary to put active channel in standby mode first and then immediately (with regard to Standby time) activate right (left) channel or both channels together in at the same moment.

4.10 Application example: differential-input BTL power stereo amplifier

The schematic in [Figure 65](#) shows how to design the TS4985 to work in differential-input mode. For this discussion, only the left-channel amplifier will be referred to.

Let:

$$R_{1R} = R_{2L} = R_1, R_{2R} = R_{2L} = R_2$$

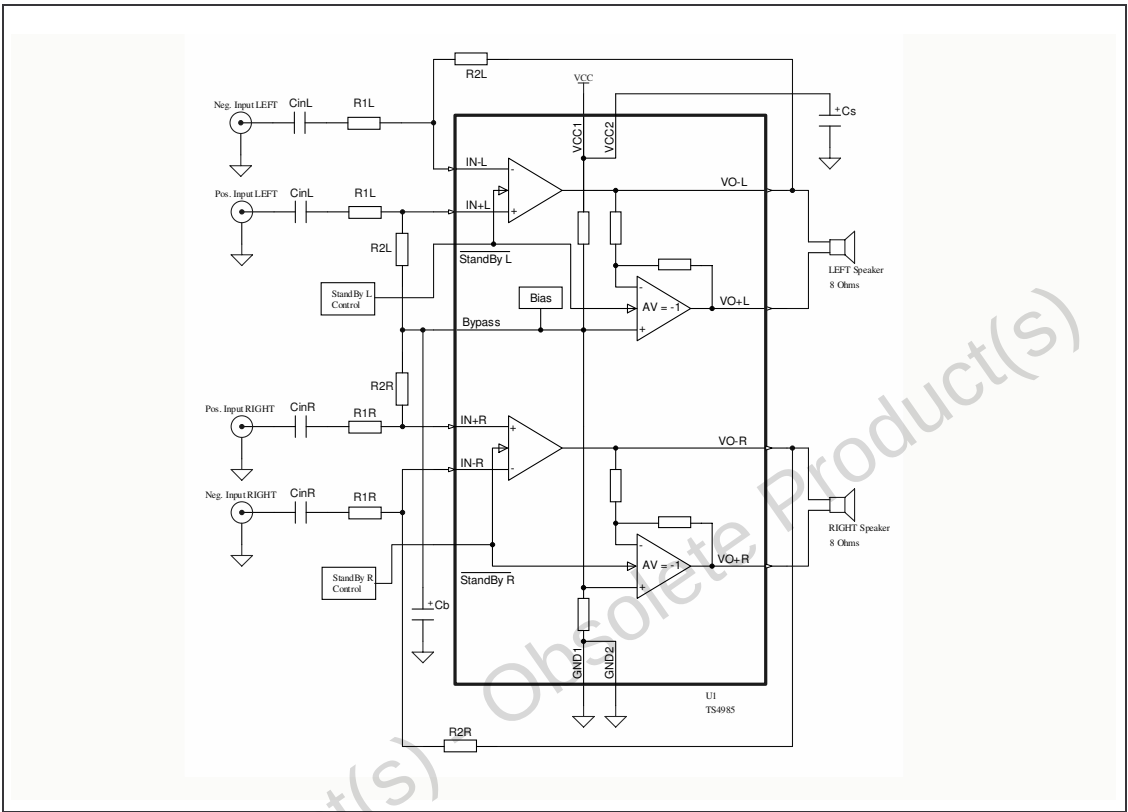
$$C_{inR} = C_{inL} = C_{in}$$

The gain of the amplifier is:

$$G_{vdif} = 2 \times \frac{R_2}{R_1}$$

In order to reach the optimal performance of the differential function, R_1 and R_2 should be matched at 1% maximum.

Figure 66. Differential input amplifier configuration



The value of the input capacitor C_{IN} can be calculated with the following formula, using the -3dB lower frequency required (where F_L is the lower frequency required):

$$C_{IN} \approx \frac{1}{2\pi R_1 F_L} \text{ (F)}$$

Note: This formula is true only if:

$$F_{CB} = \frac{1}{2\pi (R_1 + R_2) C_B} \text{ (Hz)}$$

is 5 times lower than F_L .

The following bill of materials ([Table 8](#)) is provided as an example of a differential amplifier with a gain of 2 and a -3dB lower cut-off frequency of about 80Hz.

Table 8. Example of a bill of materials

Designator	Part Type
$R_{1L} = R_{1R}$	20kΩ / 1%
$R_{2L} = R_{2R}$	20kΩ / 1%
$C_{inR} = C_{inL}$	100nF
$C_b = C_s$	1μF
U1	TS4985

4.11 Demoboard

A demoboard for the TS4985 in flip-chip package is available.

For more information about this demoboard, please refer to **Application Note AN2152**, which can be found on **www.st.com**.

Figure 67 shows the schematic of the demoboard. *Figure 68*, *Figure 69* and *Figure 70* show the component locations, top layer and bottom layer respectively.

Figure 67. Demoboard schematic

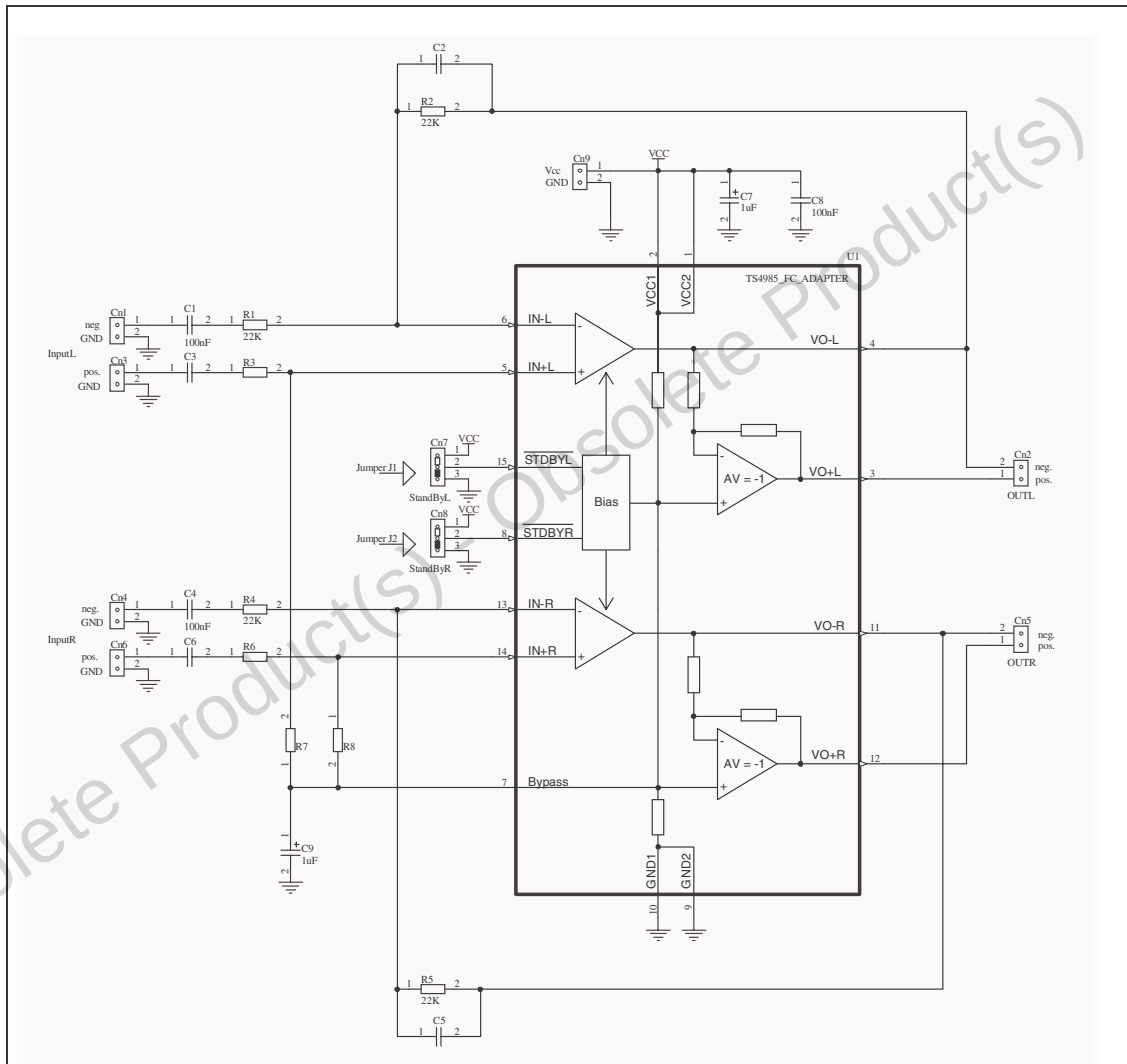


Figure 68. Component locations

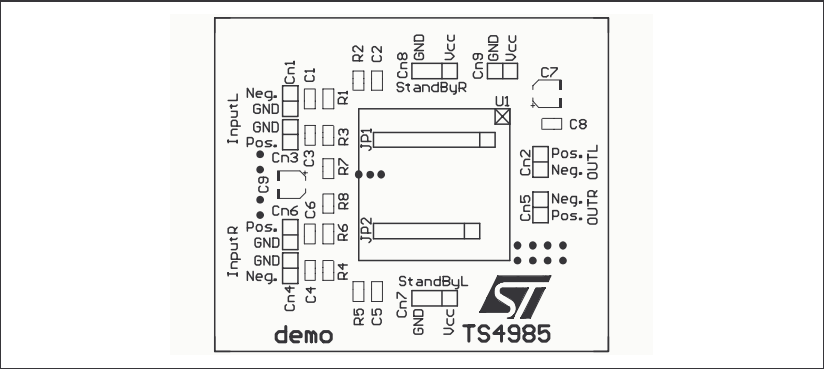


Figure 69. Top layer

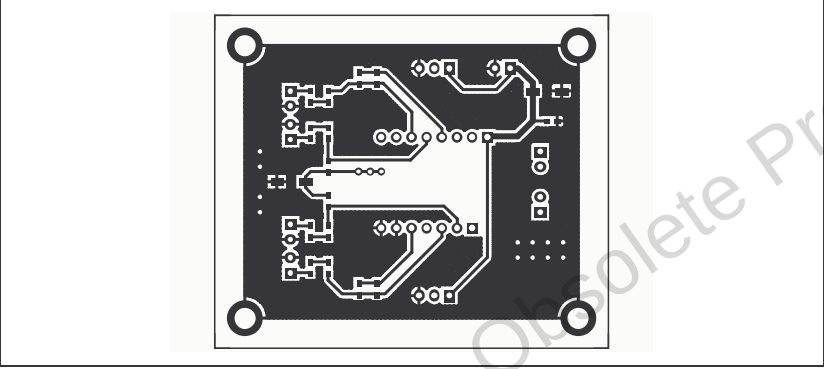
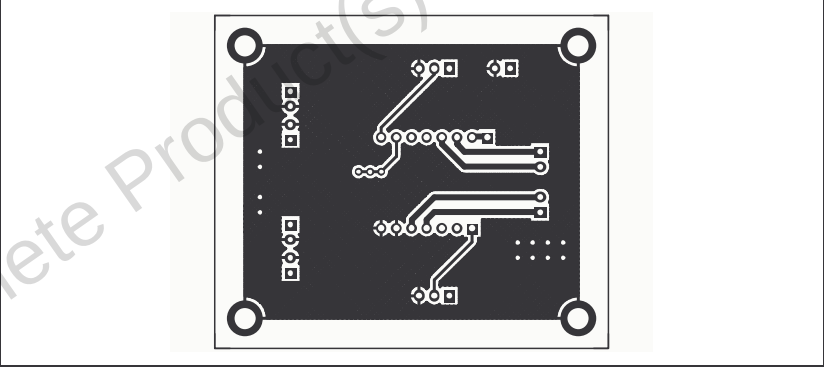


Figure 70. Bottom layer



5 Package Mechanical Data

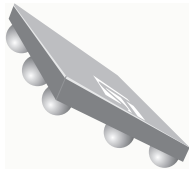


Figure 71. Pinout (top view)

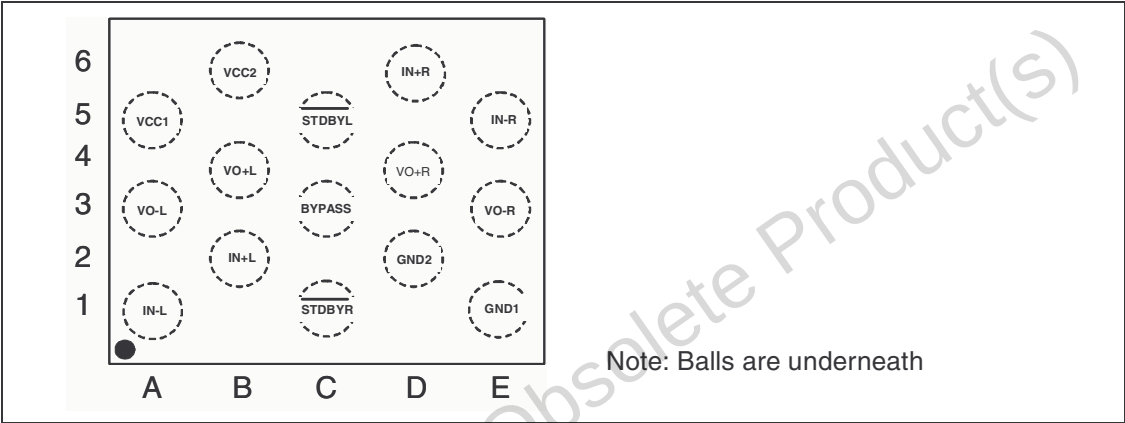


Figure 72. Marking (top view)

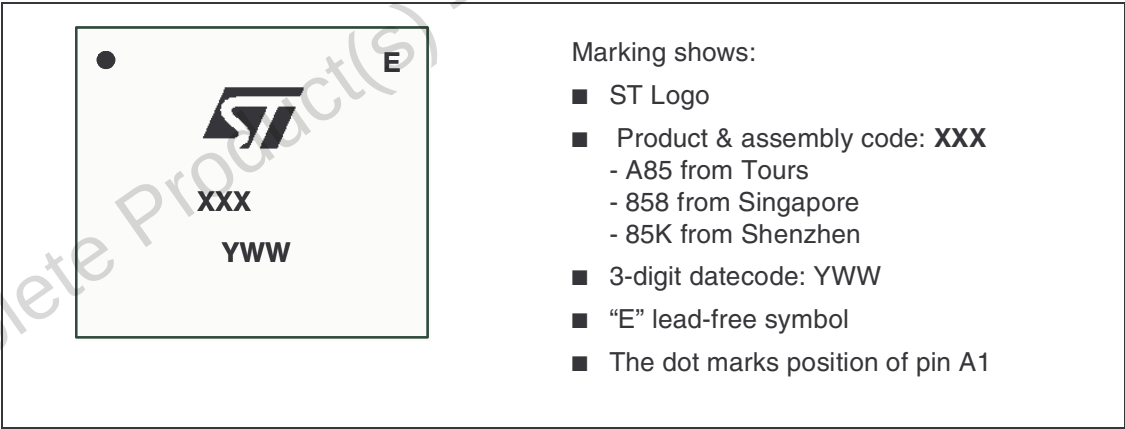


Figure 73. Package mechanical data for 15-bump flip-chip

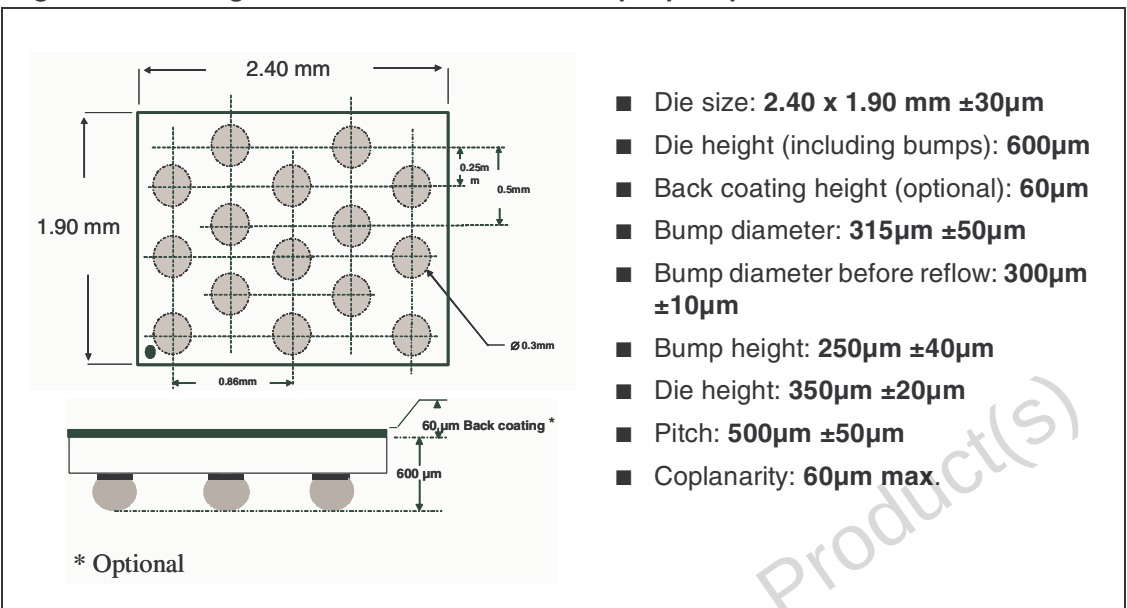
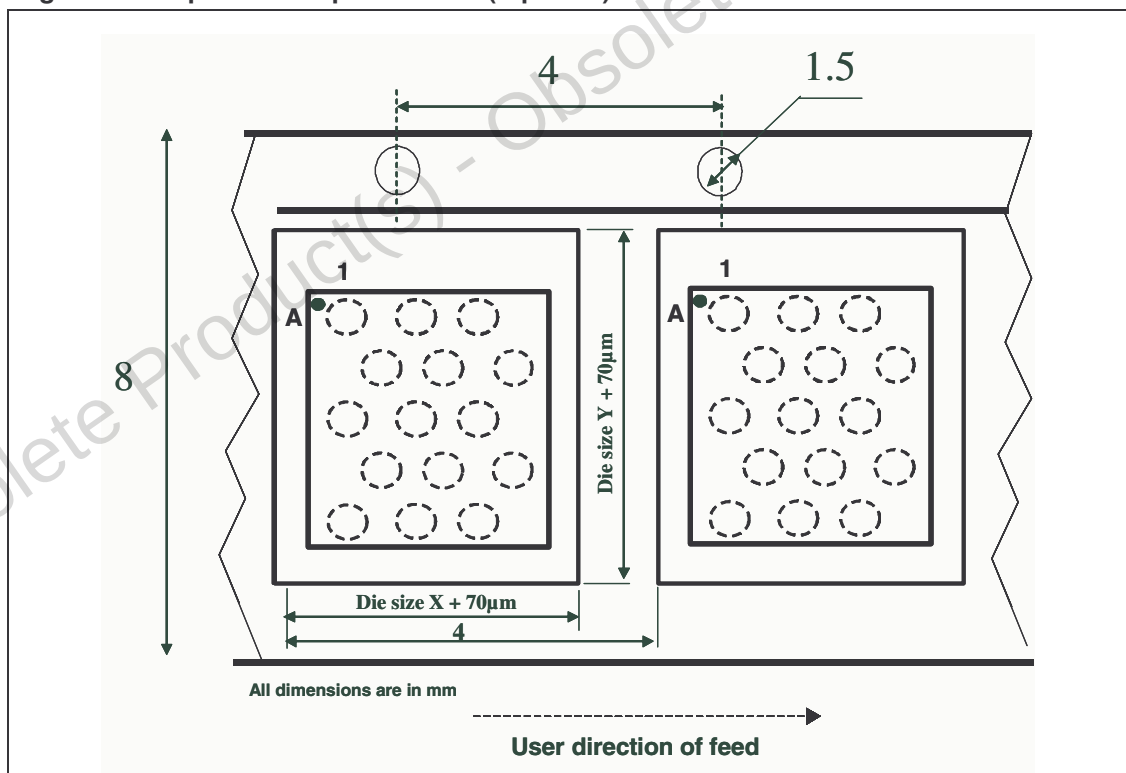


Figure 74. Tape & Reel specification (top view)



6 Revision History

Date	Revision	Changes
November 2004	1	First Release corresponding to the product preview version
May 2005	2	Product in full production

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