CMOS 66 MHz Monolithic 256×24 Color Palette RAM-DAC

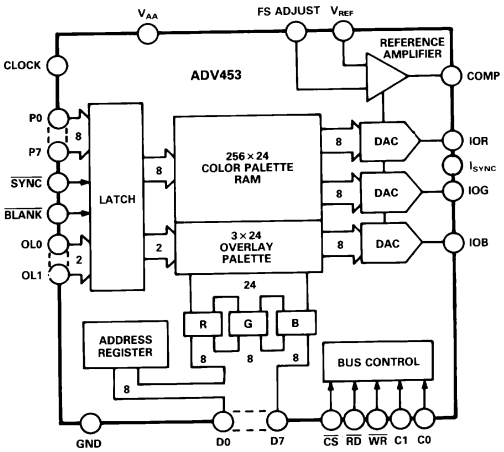
ADV453

FEATURES
66 MHz Pipelined Operation
Triple 8-Bit D/A Converters
256×24 Color Palette RAM
3×24 Overlay Registers
RS-343A/RS-170 Compatible Outputs
+5 V CMOS Monolithic Construction
40-Pin DIP or Small 44-Pin PLCC Package
Power Dissipation: 1000 mW

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES
66 MHz
40 MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV453 is a complete analog video output RAM-DAC on a single monolithic chip. It is specifically designed for high resolution color graphics systems. The part contains a 256 × 24 color lookup table, a 3 × 24 overlay palette as well as triple 8-bit video D/A converters. The ADV453 is capable of simultaneously displaying up to 259 colors, 256 from the lookup table and three from the overlay registers, out of a total color palette of 16.8 million addressable colors.

The three overlay registers allow for implementation of overlaying cursors, pull down menus and grids. There is an independent, asynchronous MPU bus which allows access to the color lookup table without affecting the input of video data via the pixel port. The ADV453 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV453 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6", 40-pin DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 66 MHz.
2. Compatible with a wide variety of high resolution color graphics systems including VGA* and Macintosh II.**
3. Three overlay registers allow for implementation of overlaying cursors, pull down menus and grids.
4. Guaranteed monotonic. Integral and differential nonlinearities guaranteed to be a maximum of ±1 LSB.
5. Low glitch energy, 50 pV secs.

*VGA is a trademark of International Business Machines Corp.
**Macintosh II is a registered trademark of Apple Computer Inc.

REV. B

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ADV453–SPECIFICATIONS

(V_{AA} = +5 V ± 5%, V_{REF} = +1.235 V, R_{SET} = 280 Ω. I_{SYNC} connected to IOG. All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±1	LSB max	Guaranteed Monotonic
Differential Nonlinearity	±1	LSB max	
Gray Scale Error	±5%	Gray Scale max	
Coding		Binary	
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	µA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance C_{IN}	10	pF typ	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	20	µA max	
Floating-State Output Capacitance	20	pF typ	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
	1.90	mA max	
Blank Level on IOR, IOB	0	µA min	Typically 5 µA
	50	µA max	
Blank Level on IOG	6.29	mA min	Typically 7.62 mA
	8.96	mA max	
Sync Level on IOG	0	µA min	Typically 5 µA
	50	µA max	
LSB Size	69.1	µA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	–1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF typ	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	
Input Current, I_{VREF}	–5	mA typ	
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	
Supply Current, I_{AA}	275	mA max	Typically 220 mA, 66 MHz Parts
	250	mA max	Typically 190 mA, 40 MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%, f = 1 kHz, COMP = 0.1 µF
Power Dissipation	1375	mW max	Typically 1000 mW, 66 MHz Parts
	1250	mW max	Typically 900 mW, 40 MHz Parts
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[2, 3]	–30	dB typ	
Glitch Impulse[2, 3]	50	pV secs typ	
DAC-to-DAC Crosstalk	–23	dB typ	

NOTES

[1]Temperature range (T_{MIN} to T_{MAX}); 0°C to +70°C.

[2]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, 37.5 Ω. D0–D7 output load ≤50 pF. See timing notes in Figure 2.

[3]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2 × clock rate.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA} = +5 V ± 5%, V_{REF} = +1.235 V, R_{SET} = 280 Ω. I_{SYNC} connected to IOG. All specifications T_{MIN} to T_{MAX}[2].)

Parameter	66 MHz Version	40 MHz Version	Units	Conditions/Comments
f_{MAX}	66	40	MHz max	Clock Rate
t_1	35	35	ns min	$\overline{CS}$, C0, C1 Setup Time
t_2	35	35	ns min	$\overline{CS}$, C0, C1 Hold Time
t_3	25	25	ns min	$\overline{RD}$, $\overline{WR}$ High Time
t_4	10	10	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_5	100	100	ns max	$\overline{RD}$ Asserted to Data Valid
t_6	15	15	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_7	50	50	ns min	$\overline{WR}$ Low Time
t_8	35	35	ns min	Write Data Setup Time
t_9	0	0	ns min	Write Data Hold Time
t_{10}	5	7	ns min	Pixel & Control Setup Time
t_{11}	2	3	ns min	Pixel & Control Hold Time
t_{12}	15	25	ns min	Clock Cycle Time
t_{13}	5	7	ns min	Clock Pulse Width High Time
t_{14}	5	7	ns min	Clock Pulse Width Low Time
t_{15}	20	20	ns typ	Analog Output Delay
	30	30	ns max	
t_{16}	3	3	ns typ	Analog Output Rise/Fall Time
t_{17}[3]	25	25	ns typ	Analog Output Settling Time
t_{PD}	$2\times t_{12}$	$2\times t_{12}$	ns max	Pipeline Delay
t_{SK}	1	1	ns typ	Analog Output Skew
	2	2	ns max	

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, 37.5 Ω. D0–D7 output load ≤50 pF. See timing notes in Figure 2.
[2]Temperature Range (T_{MIN} to T_{MAX}); 0°C to +70°C.
[3]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic.

Specifications subject to change without notice.

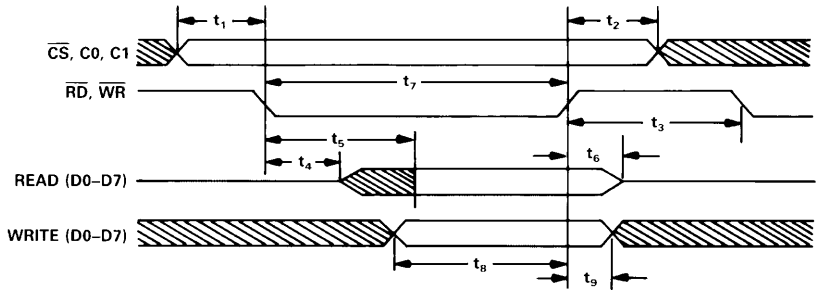


Figure 1. MPU Read/Write Timing

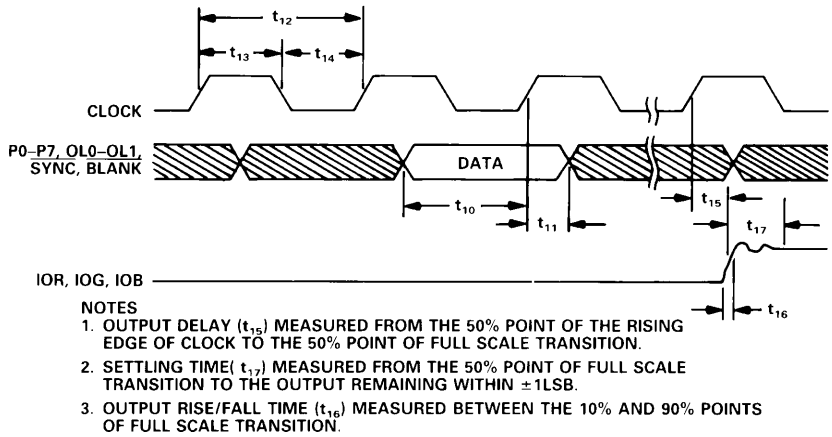


Figure 2. Video Input/Output Timing

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . +7 V
Voltage on Any Digital Pin . . . . GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . . 0°C to +70°C
Storage Temperature (T_S) . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (1 minute) . . . . . +220°C
IOR, IOB, IOG to GND[2] . . . . . 0 V to V_{AA}

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE

Model	Temperature Range	Speed	Package Option*
ADV453KN66	0°C to +70°C	66 MHz	N-40A
ADV453KN40	0°C to +70°C	40 MHz	N-40A
ADV453KP66	0°C to +70°C	66 MHz	P-44A
ADV453KP40	0°C to +70°C	40 MHz	P-44A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier.

RECOMMENDED OPERATING CONDITIONS

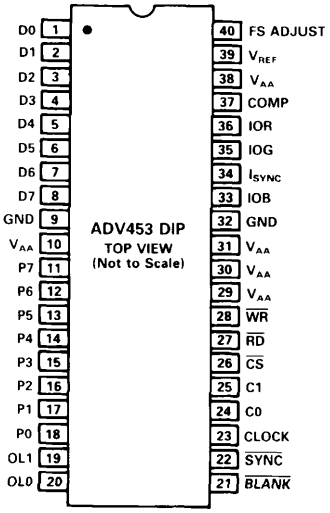
Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

CAUTION

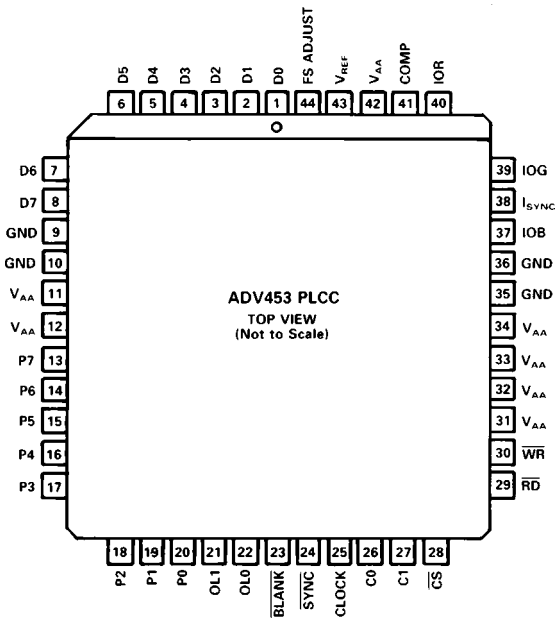
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV453 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{BLANK}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs to the blanking level, as shown in Table V. The $\overline{BLANK}$ signal is latched on the rising edge of CLOCK. While $\overline{BLANK}$ is at logical zero, the pixel inputs are ignored.
$\overline{SYNC}$	Composite sync control input (TTL compatible). A logical zero on the $\overline{SYNC}$ input switches off a 40 IRE current source on the I_{SYNC} output (see Figure 5). $\overline{SYNC}$ does not override any other control or data input, as shown in Table V; therefore, it should only be asserted during the blanking interval. $\overline{SYNC}$ is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7 and OL0–OL1 data inputs as well as the $\overline{SYNC}$ and $\overline{BLANK}$ control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 pixel select inputs are latched on the rising edge of CLOCK. P0 is the LSB. Unused pixel select inputs should be connected to GND.
OL0–OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information (see Table IV), i.e., the 256×24 color palette or the 3×24 overlay palette. When accessing the overlay palette, the P0–P7 inputs are ignored. OL0–OL1 are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable, as shown in Figure 4a. All three current outputs should have similar output loads whether or not they are all being used.
I_{SYNC}	Sync current output. This high impedance current source can be directly connected to the IOG output (see Figure 3). This allows sync information to be encoded onto the green channel. I_{SYNC} does not output any current while $\overline{SYNC}$ is at logical zero. The amount of current output at I_{SYNC} while $\overline{SYNC}$ is at logical one is given by: I_{SYNC} (mA) = 1,728* V_{REF}(V)/R_{SET}(Ω). If sync information is not required on the green channel, I_{SYNC} should be connected to GND.
FS ADJUST	Full scale adjust control. A resistor (R_{SET}) connected between this pin and GND (see Figure 6) controls the magnitude of the full scale video signal. Note that the IRE relationships in Figure 5 are maintained, regardless of the full scale output current. The relationship between R_{SET} and the full scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: IOG (mA) = (K + 326 + 1,728)* V_{REF}(V)/R_{SET}(Ω) The relationship between R_{SET} and the full scale output current on IOR and IOB is given by: IOR, IOB (mA) = (K + 326)* V_{REF}(V)/R_{SET}(Ω) where K = 3,993
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between COMP and V_{AA} (Figure 6).
V_{REF}	Voltage reference input. An external 1.235 V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 µF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA} (Figure 6.)
V_{AA}	Analog power supply (5 V ± 5%). All V_{AA} pins on the ADV453 must be connected.
GND	Analog ground. All GND pins must be connected.
$\overline{CS}$	Chip select control input (TTL compatible). $\overline{CS}$ must be at logical zero to enable the reading and writing of data to and from the device. The IOR, IOG and IOB outputs are forced to the black level while $\overline{CS}$ is at logical zero. Note that the ADV453 will not operate properly if $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are simultaneously at logical zero.
$\overline{WR}$	Write control input (TTL compatible). $\overline{CS}$ and $\overline{WR}$ must both be at logical zero when writing data to the device. D0–D7 data is latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. See Figure 1.
$\overline{RD}$	Read control input (TTL compatible). $\overline{CS}$ and $\overline{RD}$ must both be at logical zero when reading data from the device. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being carried out, i.e., address register, color palette RAM or overlay registers read or write operations. See Tables I, II, III.
D0–D7	Data bus (TTL compatible). Data is transferred to and from the address register, the color palette RAM and the overlay registers over this 8-bit bidirectional data bus. D0 is the least significant bit.

TERMINOLOGY

Blanking Level
The level separating the SYNC portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal (SYNC)
The position of the composite video signal which synchronizes the scanning process.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Sync Level
The peak level of the SYNC signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION

MPU Interface
As illustrated in the functional block diagram, the ADV453 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers. The color palette RAM and overlay color registers can be accessed only when $\overline{CS}$ is low. The Pixel and Overlay Select inputs are disabled while $\overline{CS}$ is low.

The C0 and C1 control inputs specify whether the MPU is accessing the address register, the color palette RAM or the overlay registers, as shown in Table I. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers.

Table I. Control Input Truth Table

$\overline{CS}$	C1	C0	Addressed by MPU
0	X	0	Address Register
0	0	1	Color Palette RAM
0	1	1	Overlay Register

To write color data, the MPU writes to the address register with either the address of the color palette RAM location or the address of the overlay register which is to be modified. The MPU performs three successive write cycles (8 bits of red data, 8 bits of green data and 8 bits of blue data). The color data is diverted to either the color palette RAM or the overlay registers, as determined by C0 and C1. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then automatically increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.

To read back color data, the MPU loads the address register (selecting RAM or overlay read mode) with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (8 bits each of red, green and blue data), using C0 and C1 to select either the color palette RAM or the overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green and blue data.

When $\overline{CS}$ is low i.e., during MPU read/write cycles, the video outputs are forced to the black level. During color palette RAM access, the address register resets to 00H following a blue read or write operation to RAM location FFH.

The three overlay registers can be accessed in the same way as the color palette RAM. The overlays are selected using C0 and C1 according to Table I. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the six most significant bits of the address register (ADDR2–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Color (RGB) data is normally loaded to the color palette RAM/overlay registers during video screen retrace, i.e., during the video waveform blanking period, see Figure 5.

To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table III. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing and Table III shows the associated functional instructions.

Table II. Address Register (ADDR) Operation

	Value	C1	C0	Addressed by MPU
ADDRa,b (Counts Modulo 3)	00	X	1	Red Value
	01	X	1	Green Value
	10	X	1	Blue Value
ADDR0–7 (Counts Binary)	00H–FFH	0	1	Color Palette RAM
	XXXX XX00	1	1	Reserved
	XXXX XX01	1	1	Overlay Color 1
	XXXX XX10	1	1	Overlay Color 2
	XXXX XX11	1	1	Overlay Color 3

NOTE
Control input C1 determines whether a read/write operation is performed on the color palette RAM or the overlay registers.

Table III. Truth Table for Read/Write Operations

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	C0	C1	ADDRb	ADDRa	Operation Performed	
0	1	0	0	X	X	X	Write Address Register;	D0–D7→ADDR0–7 0→ADDRa,b
0	1	0	1	X	0	0	Write Red Value;	Increment ADDRa-b
0	1	0	1	X	0	1	Write Green Value;	Increment ADDRa-b
0	1	0	1	X	1	0	Write Blue Value;	Modify RAM/Overlay Location Increment ADDR0–7 Increment ADDRa-b
0	0	1	0	X	X	X	Read Address Register;	ADDR0–7→D0–D7
0	0	1	1	X	0	0	Read Red Value;	Increment ADDRa-b
0	0	1	1	X	0	1	Read Green Value;	Increment ADDRa-b
0	0	1	1	X	1	0	Read Blue Value; Increment ADDRa-b	Increment ADDR0–7
0	0	0	X	X	X	X	Invalid Operation	

NOTE
Control input C1 determines whether a read/write operation is performed on the color palette RAM or the overlay registers.

Frame Buffer Interface

The P0–P7, OL0 and OL1 inputs are used to address the color palette RAM and overlay registers, as shown in Table IV. These inputs are latched on the rising edge of CLOCK and address any of the 256 locations in the color palette RAM or the three overlay registers. The addressed location contains 24 bits of color (8 bits of red, 8 bits of green and 8 bits of blue) information. This data is transferred to the three DACs and is then converted to an analog output (IOR, IOG and IOB), these outputs then control the red, green and blue electron guns in the monitor.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs are also latched on the rising edge of CLOCK. This is to maintain synchronization with the color data.

Table IV. Pixel and Overlay Control Truth Table

OL1	OL0	P0–P7	Addressed by Frame Buffer
0	0	00H	Color Palette RAM Location 00H
0	0	01H	Color Palette RAM Location 01H
•	•	•	•
•	•	•	•
0	0	FFH	Color Palette RAM Location FFH
0	1	XXH	Overlay Color 1
1	0	XXH	Overlay Color 2
1	1	XXH	Overlay Color 3

Analog Interface

The ADV453 has three analog outputs, corresponding to the red, green and blue video signals. A fourth analog output (I_{SYNC}) can be used if it is required to encode video synchronization information onto the green signal. In this case, I_{SYNC} is connected to IOG as shown in Figure 3. If it is not required to encode sync information onto the green signal (as would be the case if a separate synchronization circuit was used), I_{SYNC} should be connected to GND and the digital $\overline{\text{SYNC}}$ input pin should be tied low.

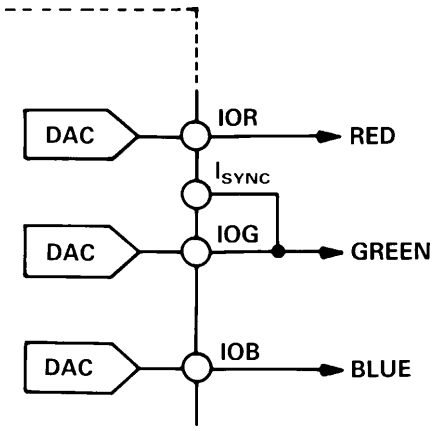


Figure 3. Encoding SYNC onto Green Signal

The red, green and blue analog outputs of the ADV453 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable. Figure 4a shows the required configuration for each of the three RGB outputs connected into a doubly-terminated 75 Ω load. This arrangement will develop RS-343A video output voltage levels across a 75 Ω monitor. A simple method of driving RS-170 video levels into a 75 Ω monitor is shown in Figure 4b. The output current levels of the DACs remain unchanged, but the source termination resistance, Z_S, on each of the three DACs is increased from 75 Ω to 150 Ω.

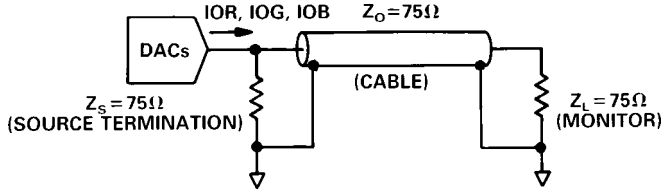


Figure 4a. Recommended Analog Output Termination for RS-343A

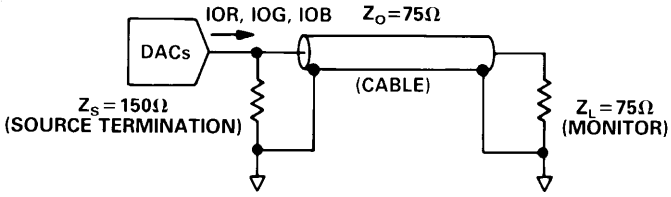
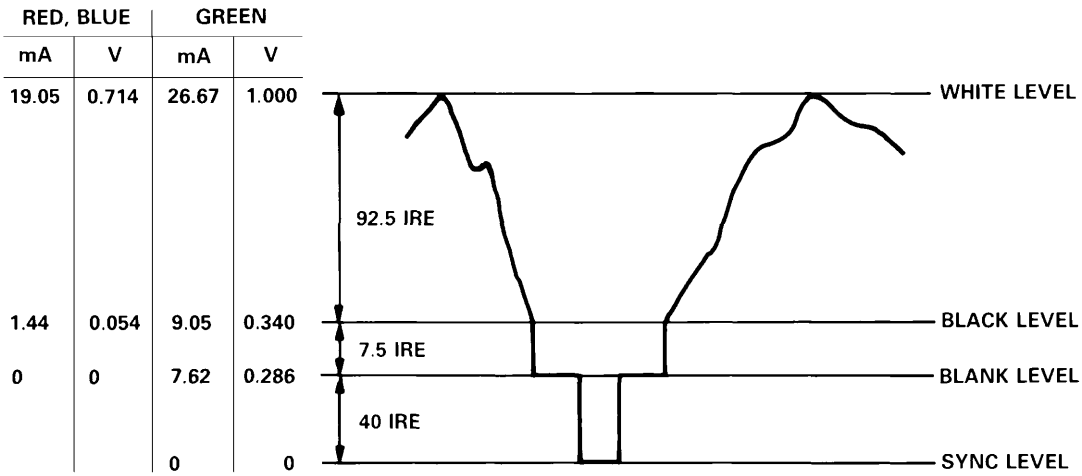


Figure 4b. Recommended Analog Output Termination for RS-170

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an application note entitled "Video Formats & Required Load Terminations," available from Analog Devices.

Figure 5 shows the video waveforms associated with the three RGB outputs, driving the doubly terminated 75 Ω load of Figure 4a. As well as the gray scale levels, black level to white level, the diagram also shows the contributions of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$. These control inputs add appropriately weighted currents to the analog outputs producing the specific output level requirements for video applications. Table V details how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs modify the output levels.



NOTES
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.
2. V_{REF} = 1.235V, R_{SET} = 280Ω, I_{SYNC} CONNECTED TO IOG.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 5. RGB Video Output Waveform

Table V. Video Output Truth Table

Description	IOG mA[1]	IOR, IOB, mA	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
White Level	26.67	19.05	1	1	FFH
Video	Video + 9.05	Video + 1.44	1	1	Data
Video to Blank	Video + 1.44	Video + 1.44	0	1	Data
Black Level	9.05	1.44	1	1	00H
Black to Blank	1.44	1.44	0	1	00H
Blank Level	7.62	0	1	0	XXH
SYNC Level	0	0	0	0	XXH

NOTE
[1]Typical with full Scale IOG = 26.67 mA. V_{REF} = 1.235 V, R_{SET} = 280 Ω, I_{SYNC} connected to IOG.

PC BOARD LAYOUT CONSIDERATIONS

The ADV453 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV453, it is imperative that great care be given to the PC board layout. The layout should be optimized for lowest noise on the ADV453 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

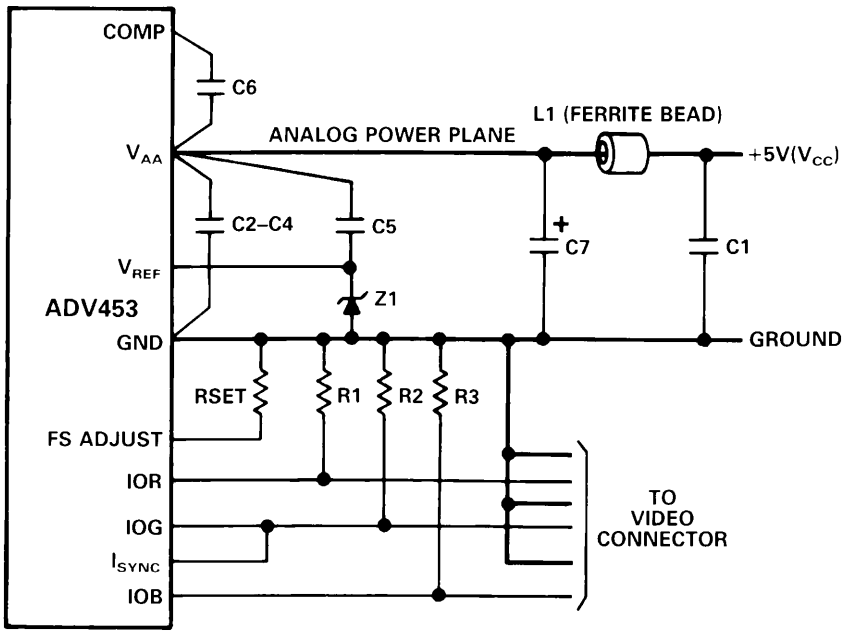
The ground plane should encompass all ADV453 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and all the digital signal traces leading up to the ADV453.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane should encompass the ADV453 (V_{AA}) and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figure 6. This bead should be located within three inches of the ADV453.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV453 power pins, voltage reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C6	0.1µF CERAMIC CAPACITOR	
C7	10µF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	280Ω 1% METAL FILM RESISTOR	DALE CMF-55C
Z1	1.235V VOLTAGE REFERENCE	ANALOG DEVICES AD589KH

Figure 6. ADV453 Typical Connection Diagram and Component List

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors, see Figure 6.

Optimum performance is achieved by the use of 0.1 µF ceramic capacitors. Each of the three groups of V_{AA} should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV453 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three-terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the ADV453 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV453 should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV453 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

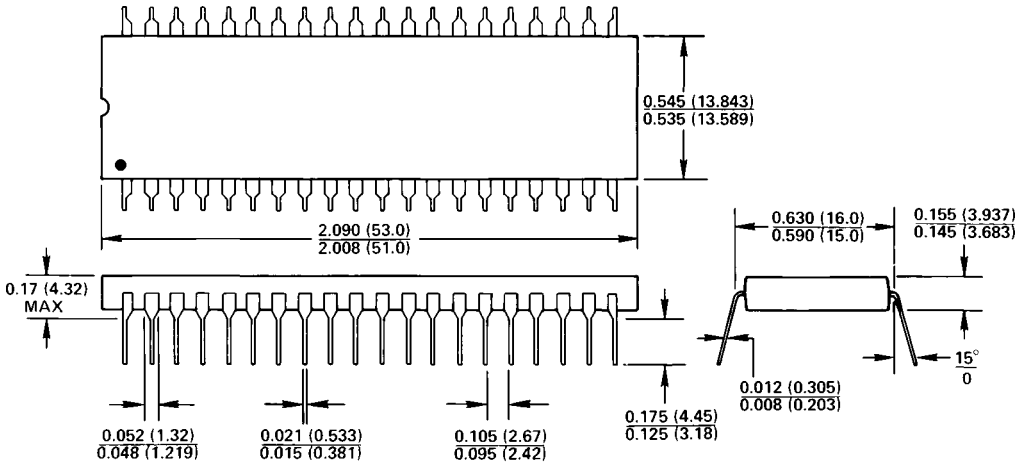
The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω. This termination resistance should be as close as possible to the ADV453 to minimize reflections.

OUTLINE DIMENSIONS

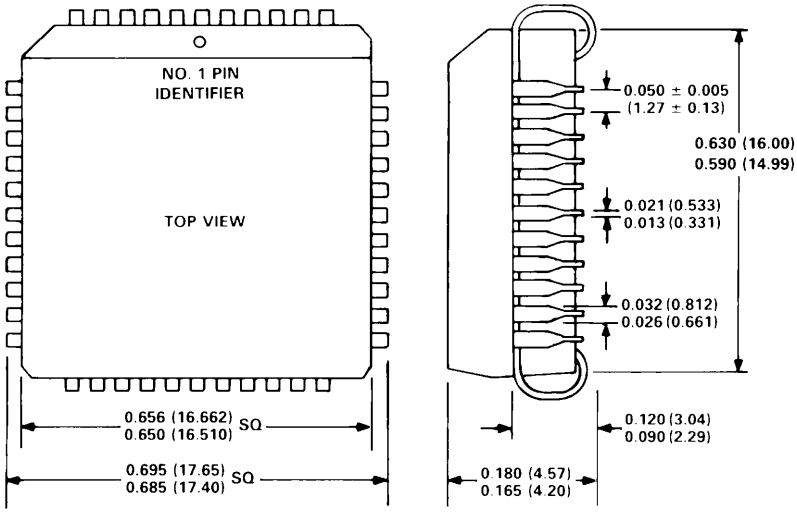
Dimensions shown in inches and (mm).

40-Pin Plastic DIP (N-40A)



LEAD NO. 1 IDENTIFIED BY DOT, NOTCH OR "1".
LEADS ARE SOLDER PLATED KOVAR OR ALLOY 42.

44-Terminal Plastic Leaded Chip Carrier (P-44A)



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