# AS1702 - AS1705

**DataSheet**

## 1.8W Single-Channel Audio Power Amplifiers

## 1 General Description

The AS1702 - AS1705 are single-channel differential audio power-amplifiers designed to drive 4 and 8Ω loads. The integrated gain circuitry of these amplifiers and their small size make them ideal for 2.7- to 5V-powered portable audio devices.

The differential input design improves noise rejection and provides common-mode rejection. A bridge-tied load (BTL) design minimizes external component count, while providing high-fidelity audio power amplification.

The devices deliver 1.8W continuous average power per channel to a 4Ω load with less than 1% total harmonic distortion (plus noise), while operating from a single 2.7 to 5V supply.

For reduced component designs, the devices are available with different gain levels as shown in Table 1.

*Table 1. Standard Products*

| Model | Gain |
|---|---|
| AS1702 | Adjustable (via external components) |
| AS1703 | AV = 0dB |
| AS1704 | AV = 3dB |
| AS1705 | AV = 6dB |

Integrated shutdown circuitry disables the bias generator and amplifiers, and reduces quiescent current consumption to less than 100nA. The shutdown input can be set active-high or active-low. All devices contain click-and-pop suppression circuitry that reduces audible clicks and pops during power-up and shutdown.

The AS1702 - AS1705 are pin compatible with the LM4895 and the MAX9718A/B/C/D. The devices are available in a 10-pin MSOP package and a 10-pin DFN package.

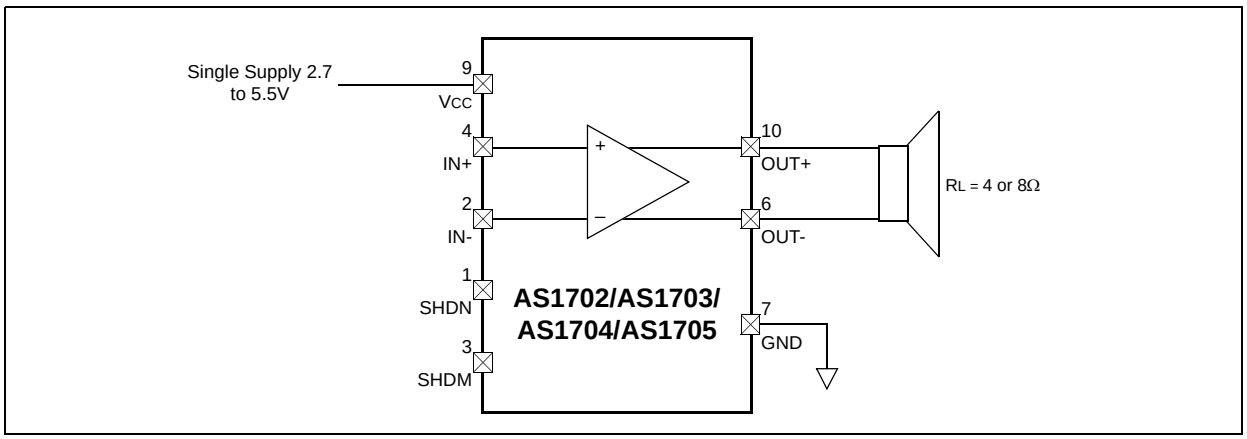
## 2 Key Features

- 2.7 to 5.5V (VCC) Single-Supply Operation
- THD+N: 1.8W into 4Ω at 1% (per Channel)
- Differential Input
- Adjustable Gain Option (AS1702)
- Internal Fixed Gain to Reduce External Component Count (AS1703, AS1704, AS1705)
- <100nA Low-Power Shutdown Mode
- Click and Pop Suppression
- Pin-Compatible to National Semiconductor LM4895 (AS1705) and Maxim MAX9718A/B/C/D
- Operating Temperature Range: -40 to +85ºC
- Package Types
  - 10-pin MSOP
  - 10-pin DFN

## 3 Applications

The devices are ideal as audio front-ends for battery powered audio devices such as MP3 and CD players, mobile phones, PDAs, portable DVD players, and any other hand-held battery-powered device.

*Figure 1. Simplified Block Diagram*



# 4 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 3 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 2. Absolute Maximum Ratings*

| Parameter | Min | Max | Unit | Comments |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$ to GND) | -0.3 | +7 | V | |
| Any Other Pin to GND | -0.3 | $V_{CC}$ + 0.3 | V | |
| Input Current (Latchup Immunity) | -50 | 50 | mA | *JEDEC 17* |
| Continuous Power Dissipation ($T_{AMB}$ = +70ºC) † | | 600 | mW | MSOP-10 |
| Continuous Power Dissipation ($T_{AMB}$ = +25ºC) † | | 1,000 | mW | MSOP-10 |
| Electro-Static Discharge (ESD) | | 1 | kV | *Human Body Model* and *MIL-Std883E 3015.7* methods |
| Operating Temperature Range ($T_{AMB}$) | -40 | +85 | ºC | |
| Storage Temperature Range | -65 | +150 | ºC | |
| Package Body Temperature | | +260 | ºC | The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"* |

† Using PCB metal plane and thermally-conductive paste.

# 5 Electrical Characteristics

## 5V Operation

*Table 3. Electrical Characteristics – 5V Supply, $T_{AMB}$ = +25ºC (unless otherwise specified)*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | $T_{AMB}$ = -40 to +85ºC | | 2.7 | | 5.5 | V |
| $I_{CC}$ | Supply Current [1] | $V_{IN-}$ = $V_{IN+}$ = $V_{BIAS}$;$T_{AMB}$ = -40 to +85ºC | | | 8 | 10.4 | mA |
| $I_{SHDN}$ | Shutdown Supply | SHDN = SHDM = GND | | | 0.05 | 1 | µA |
| $V_{IH}$ | SHDN, SHDM Threshold | | | 0.7 x $V_{CC}$ | | | V |
| $V_{IL}$ | | | | | | 0.3 x $V_{CC}$ | |
| $V_{BIAS}$ | Common-Mode Bias Voltage [2] | | | $V_{CC}$/2 - 5% | $V_{CC}$/2 | $V_{CC}$/2 + 5% | V |
| $V_{OS}$ | Output Offset Voltage | $V_{IN-}$ = $V_{IN+}$ = $V_{BIAS}$ | $A_V$ = 0dB (AS1703) | | ±1 | ±10 | mV |
| | | | $A_V$ = 3dB (AS1704) | | ±1 | ±15 | |
| | | | $A_V$ = 6dB (AS1705) | | ±1 | ±20 | |
| $V_{IC}$ | Common-Mode Input Voltage [3] | Inferred from CMRR Test | $A_V$ = 0dB (AS1703) | 0.2 | | $V_{CC}$ - 0.2 | V |
| | | | $A_V$ = 3dB (AS1704) | 0.9 | | $V_{CC}$ - 0.9 | |
| | | | $A_V$ = 6dB (AS1705) | 1.5 | | $V_{CC}$ - 1.5 | |
| | | External Gain AS1702 | | 1.5 | | $V_{CC}$ - 1.5 | |
| $R_{IN}$ | Input Impedance | AS1703, AS1704, AS1705 | | 10 | 15 | 20 | kΩ |
| CMRR | Common-Mode Rejection Ratio | $f_N$ = 1kHz | | | -64 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_{IN-}$ = $V_{IN+}$ = $V_{BIAS}$; $V_{RIPPLE}$ = 200mVp-p; $R_L$ = 8Ω; $C_{BIAS}$ = 1µF | f = 217Hz | | -79 | | dB |
| | | | f = 1kHz | | -73 | | |
| $P_{OUT}$ | Output Power [4] | THD+N = 1%; $f_{IN}$ = 1kHz | $R_L$ = 8Ω | 0.8 | 1.25 | | W |
| | | | $R_L$ = 4Ω | | 1.8 | | |
| THD+N | Total Harmonic Distortion plus Noise [5] | $R_L$ = 4Ω, $f_{IN}$ = 1kHz, $P_{OUT}$ = 1.28W, $V_{CC}$ = 5V, $A_V$ = 6dB | | | 0.06 | | % |
| | | $R_L$ = 8Ω, $f_{IN}$ = 1kHz, $P_{OUT}$ = 0.9W, $V_{CC}$ = 5V, $A_V$ = 6dB | | | 0.03 | | |
| | Gain Accuracy | AS1703, AS1704, AS1705 | | | ±1 | ±2 | % |
| | Thermal Shutdown Threshold | | | | +145 | | ºC |
| | Thermal Shutdown Hysteresis | | | | 9 | | ºC |
| $t_{PU}$ | Power-up/Enable from Shutdown Time | | | | 125 | | ms |
| $t_{SHDN}$ | Shutdown Time | | | | 3.5 | | µs |
| $V_{POP}$ | Turn-Off Transient [6] | | | | 50 | | mV |

1. Quiescent power supply current is specified and tested with no load. Quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
2. Common-mode bias voltage is the voltage on BIAS and is nominally $V_{CC}$/2.
3. Guaranteed by design.
4. Guaranteed by design.
5. Measurement bandwidth for THD+N is 22Hz to 22kHz.
6. Peak voltage measured at power-on, power-off, into or out of SHDN. Bandwidth defined by A-weighted filters, inputs at AC GND. $V_{CC}$ rise and fall times ≥ 1ms.

## 3V Operation

*Table 4. Electrical Characteristics – 3V Supply, $T_{AMB}$ = +25ºC (unless otherwise specified)*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply Current [1] | $V_{IN-}$ = $V_{IN+}$ = $V_{BIAS}$; $T_{AMB}$ = -40 to +85ºC, per amplifier | | | 7.5 | | mA |
| $I_{SHDN}$ | Shutdown Supply | SHDN = SHDM = GND per amplifier | | | 0.05 | 1 | µA |
| $V_{IH}$ | SHDN, SHDM Threshold | | | 0.7 x $V_{CC}$ | | | V |
| $V_{IL}$ | | | | | | 0.3 x $V_{CC}$ | |
| $V_{BIAS}$ | Common-Mode Bias Voltage [2] | | | $V_{CC}$/2 - 5% | $V_{CC}$/2 | $V_{CC}$/2 + 5% | V |
| $V_{OS}$ | Output Offset Voltage | $V_{IN-}$ = $V_{IN+}$ = $V_{BIAS}$ | $A_V$ = 0dB (AS1703) | | ±1 | ±10 | mV |
| | | | $A_V$ = 3dB (AS1704) | | ±1 | ±15 | |
| | | | $A_V$ = 6dB (AS1705) | | ±1 | ±20 | |
| $V_{IC}$ | Common-Mode Input Voltage [3] | Inferred from CMRR Test | $A_V$ = 0dB (AS1703) | 0.2 | | $V_{CC}$ - 0.2 | mV |
| | | | $A_V$ = 3dB (AS1704) | 0.6 | | $V_{CC}$ - 0.6 | |
| | | | $A_V$ = 6dB (AS1705) | 1.0 | | $V_{CC}$ - 1.0 | |
| | | External gain AS1702 | | 1.0 | | $V_{CC}$ - 1.0 | |
| $R_{IN}$ | Input Impedance | AS1703, AS1704, AS1705 | | 10 | 15 | 20 | kΩ |
| CMRR | Common-Mode Rejection Ratio | $f_N$ = 1kHz | | | -64 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_{IN-}$ = $V_{IN+}$ = $V_{BIAS}$; $V_{RIPPLE}$ = 200mVp-p; $R_L$ = 8Ω; $C_{BIAS}$ = 1µF | f = 217Hz | | -79 | | dB |
| | | | f = 1kHz | | -73 | | |
| $P_{OUT}$ | Output Power [4] | $R_L$ = 4Ω, THD+N = 1%; $f_{IN}$ = 1kHz | | | 640 | | mW |
| | | $R_L$ = 8Ω, THD+N = 1%; $f_{IN}$ = 1kHz | | | 440 | | |
| THD+N | Total Harmonic Distortion plus Noise [5] | $R_L$ = 4Ω, $f_{IN}$ = 1kHz, $P_{OUT}$ = 460mW, $A_V$ = 6dB | | | 0.06 | | % |
| | | $R_L$ = 8Ω, $f_{IN}$ = 1kHz, $P_{OUT}$ = 330mW, $A_V$ = 6dB | | | 0.04 | | |
| | Gain Accuracy | AS1703, AS1704, AS1705 | | | ±1 | ±2 | % |
| | Thermal Shutdown Threshold | | | | +145 | | ºC |
| | Thermal Shutdown Hysteresis | | | | 9 | | ºC |
| $t_{PU}$ | Power-up/Enable from Shutdown Time | | | | 125 | | ms |
| $t_{SHDN}$ | Shutdown Time | | | | 3.5 | | µs |
| $V_{POP}$ | Turn-Off Transient [6] | | | | 50 | | mV |

1. Quiescent power supply current is specified and tested with no load. Quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier. Guaranteed by design.
2. Common-mode bias voltage is the voltage on BIAS and is nominally $V_{CC}$/2.
3. Guaranteed by design.
4. Guaranteed by design.
5. Measurement bandwidth for THD+N is 22Hz to 22kHz.
6. Peak voltage measured at power-on, power-off, into or out of SHDN. Bandwidth defined by A-weighted filters, inputs at AC GND. $V_{CC}$ rise and fall times ≥ 1ms.

# 6 Typical Operating Characteristics

*Figure 2. THD + Noise vs. Frequency; $V_{DD}$ = 3V, $R_L$ = 4Ω, AV = 2*

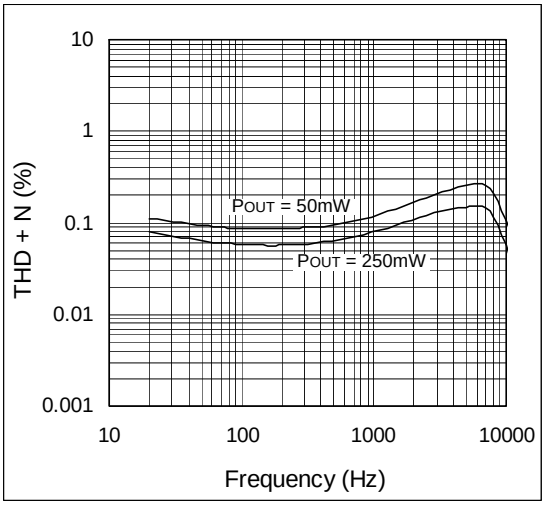



*Figure 3. THD + Noise vs. Frequency; $V_{DD}$ = 3V, $R_L$ = 8Ω, Av = 2*

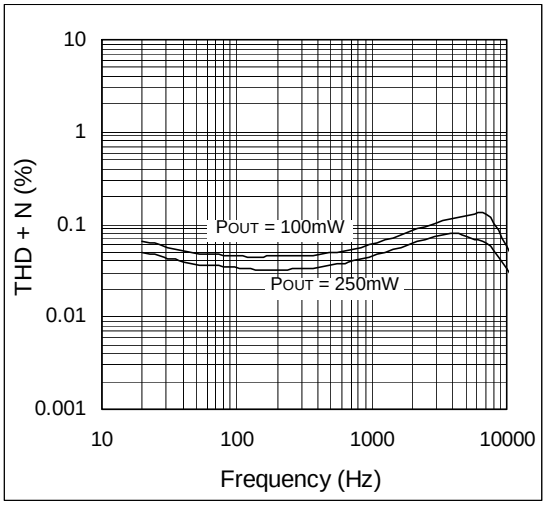



*Figure 4. THD + Noise vs. Frequency; $V_{DD}$ =5V, $R_L$ = 4Ω, Av = 2*

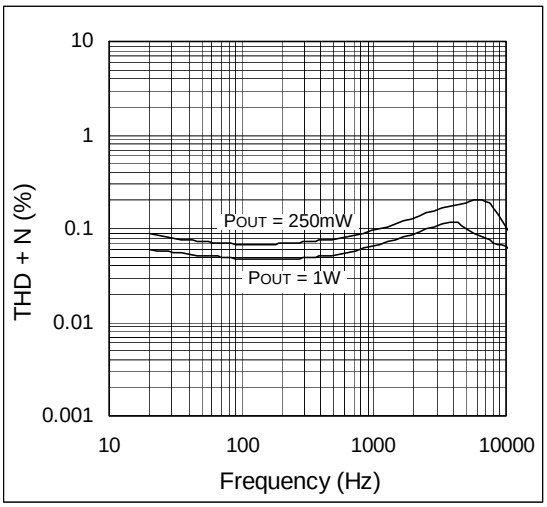



*Figure 5. THD + Noise vs. Frequency; $V_{DD}$ = 5V, $R_L$ = 8Ω, Av = 2*

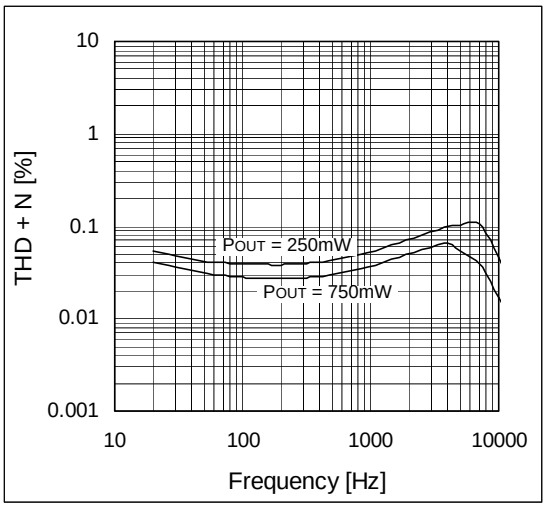



*Figure 6. THD + Noise vs. Frequency; $V_{DD}$ = 5V, $R_L$ = 4Ω, Av = 4*

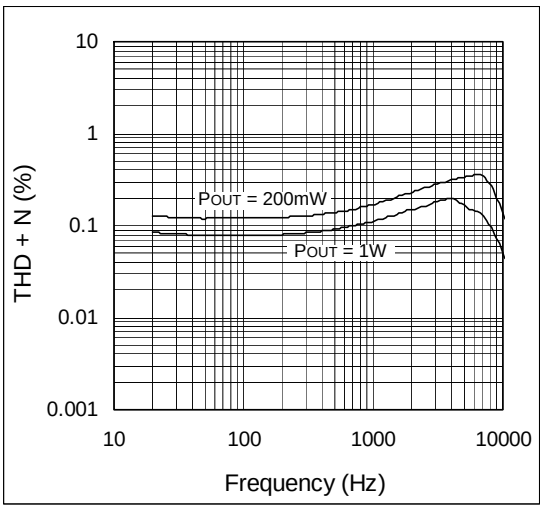



*Figure 7. THD + Noise vs. Output Power; $V_{DD}$ = 5V, $R_L$ = 8Ω, Av = 4*

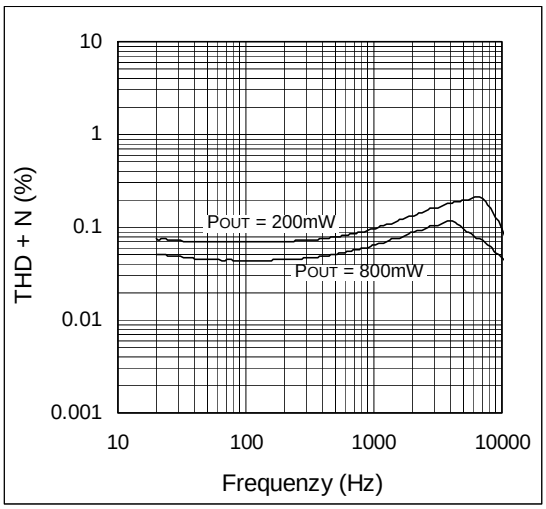


*Figure 8. THD + Noise vs. Output Power; VDD = 3V, RL = 4Ω, Av = 2*

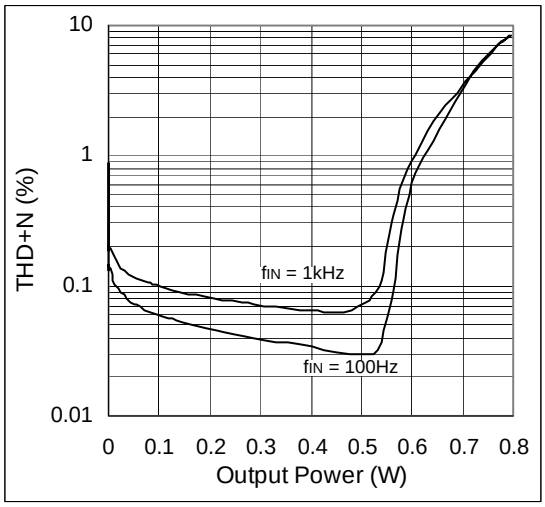



*Figure 9. THD + Noise vs. Output Power; VDD = 3V, RL = 8Ω, Av = 2*

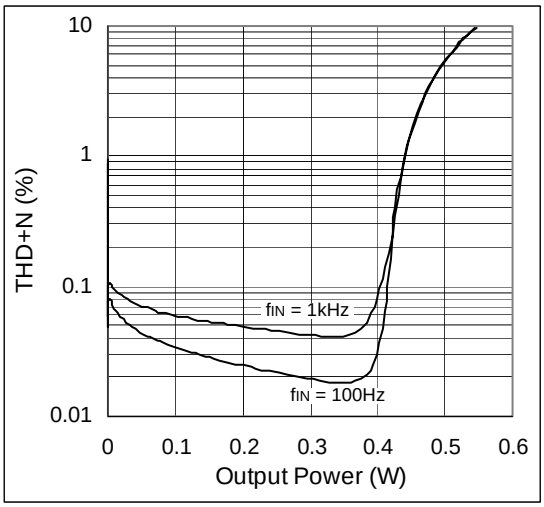



*Figure 10. THD + Noise vs. Output Power; VDD = 3V, RL = 4Ω, Av = 4*

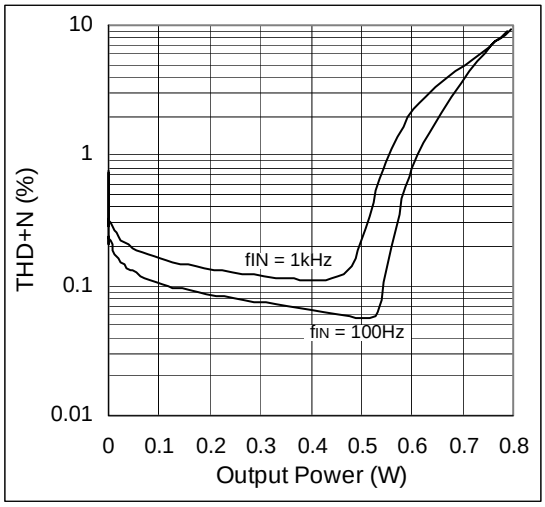



*Figure 11. THD + Noise vs. Output Power; VDD = 3V, RL = 8Ω, Av = 4*

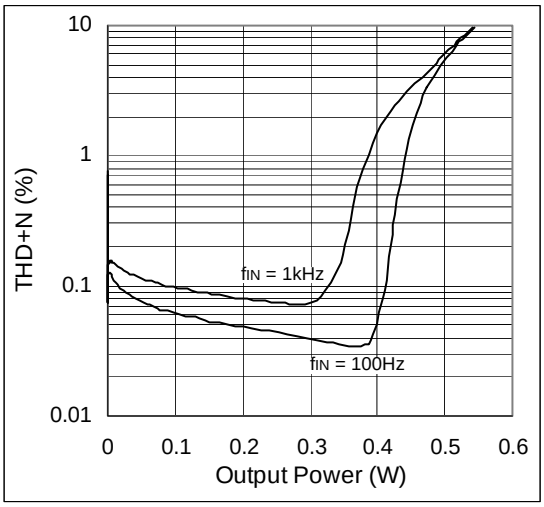



*Figure 12. THD + Noise vs. Output Power; VDD = 5V, RL = 4Ω, Av = 2*

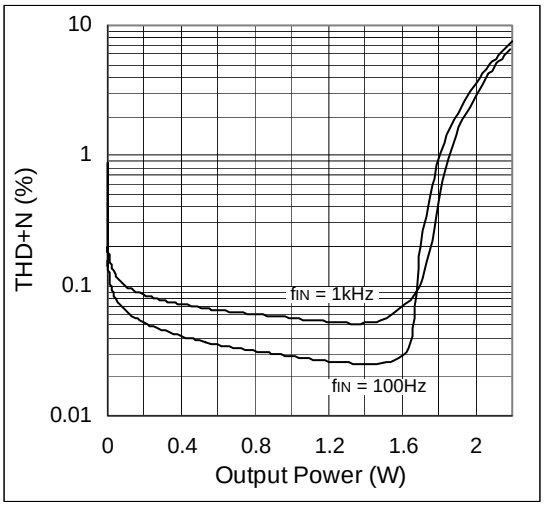



*Figure 13. THD + Noise vs. Output Power; VDD = 5V, RL = 8Ω, Av = 2*

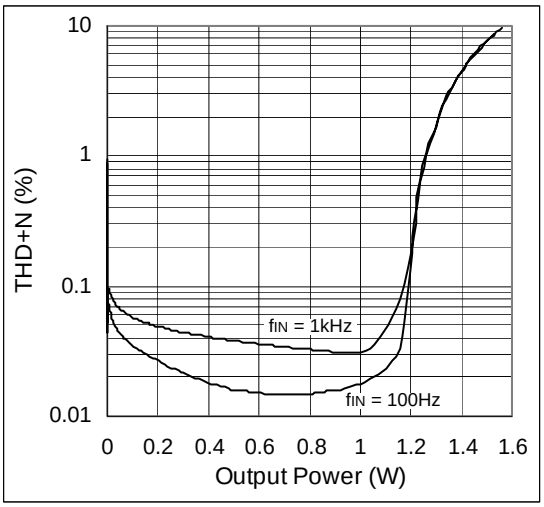


*Figure 14. THD + Noise vs. Output Power; $V_{DD}$ = 5V, $R_L$ = 4Ω, Av = 4*

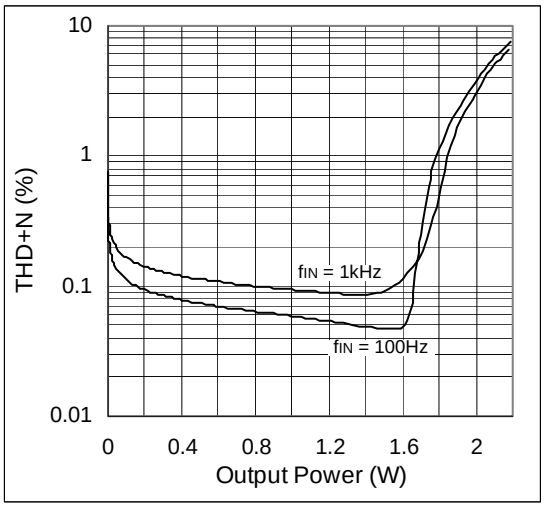



*Figure 15. THD + Noise vs. Output Power; $V_{DD}$ = 5V, $R_L$ = 8Ω, Av = 4*

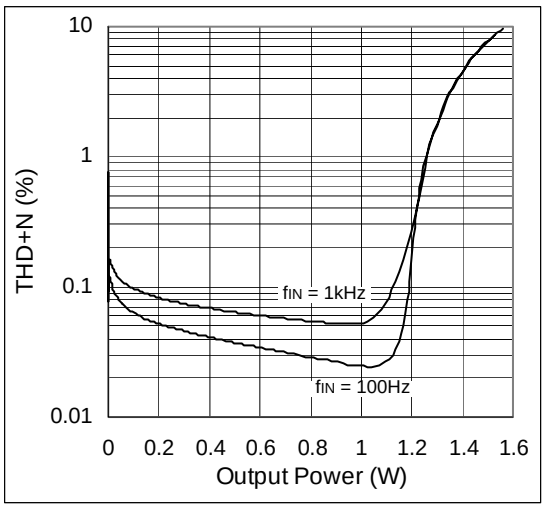



*Figure 16. Output Power vs. Load Resistance; $V_{DD}$ = 3V*

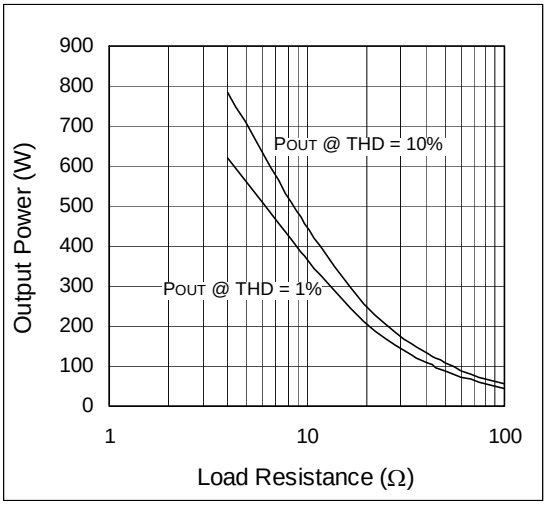



*Figure 17. Output Power vs. Load Resistance; $V_{DD}$ = 5V*

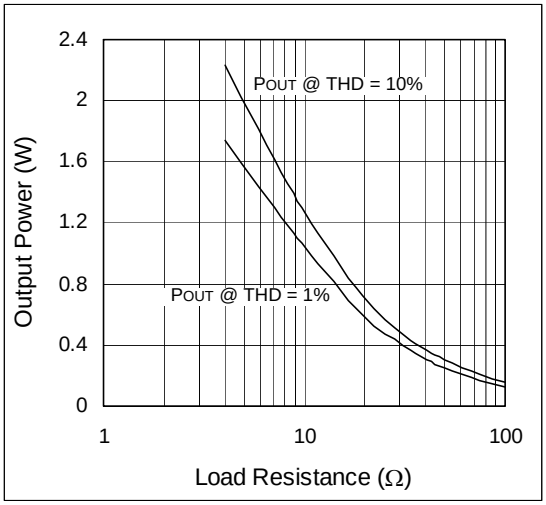



*Figure 18. Output Power vs. Supply Voltage; $R_L$ = 4Ω*

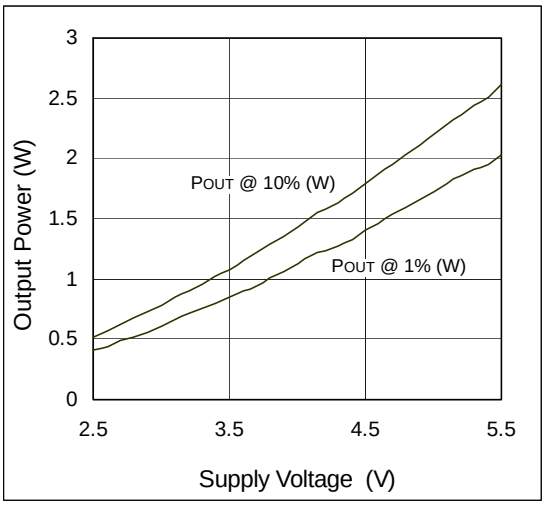



*Figure 19. Output Power vs. Supply Voltage; $R_L$ = 8Ω*

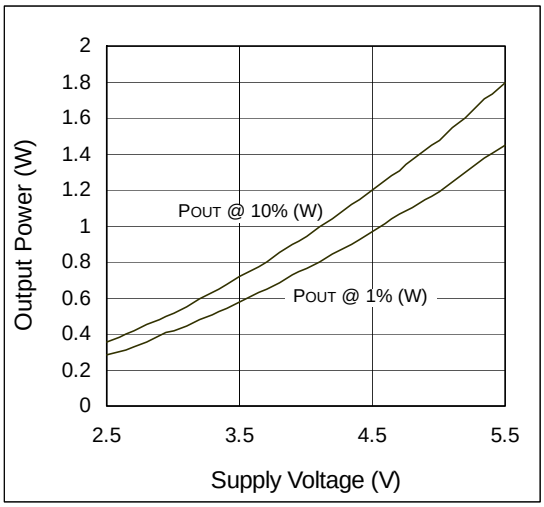


*Figure 20. Power Dissipation vs. Output Power; $V_{DD}$ = 3V, $R_L$ = 4Ω, Av = 2. f = 1kHz*

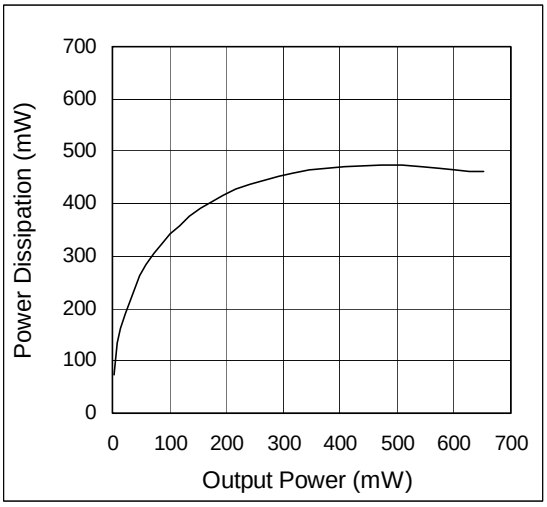



*Figure 21. Power Dissipation vs. Output Power; $V_{DD}$ = 3V, $R_L$ = 8Ω, Av = 2, f = 1kHz*

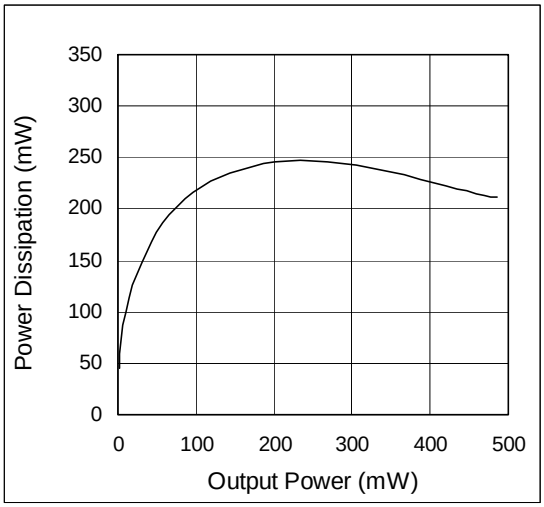



*Figure 22. Power Dissipation vs. Output Power; $V_{DD}$ = 5V, $R_L$ = 4Ω, Av = 2. f = 1kHz*

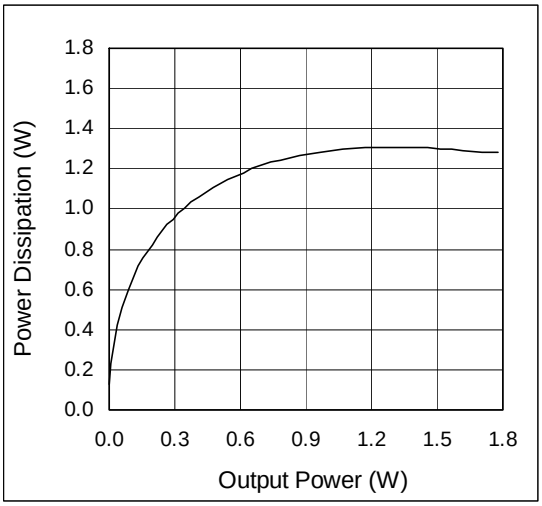



*Figure 23. Power Dissipation vs. Output Power; $V_{DD}$ = 5V, $R_L$ = 8Ω, Av = 2. f = 1kHz*

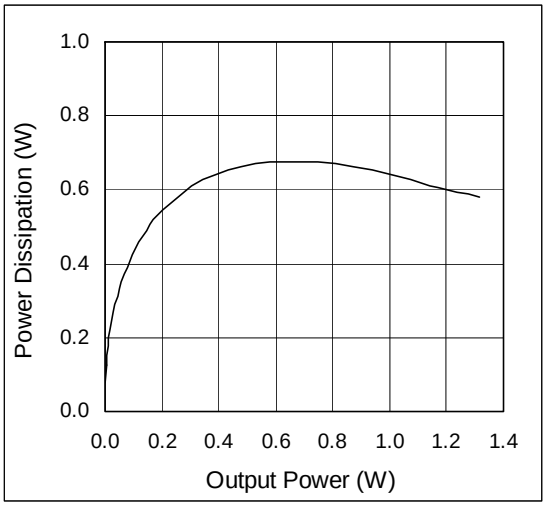



*Figure 24. Shutdown Hysteresis Voltage; $V_{DD}$ = 3V*

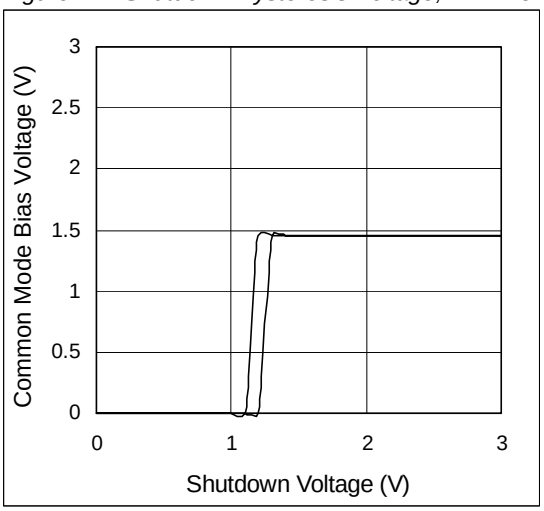



*Figure 25. Shutdown Hysteresis Voltage; $V_{DD}$ = 5V*

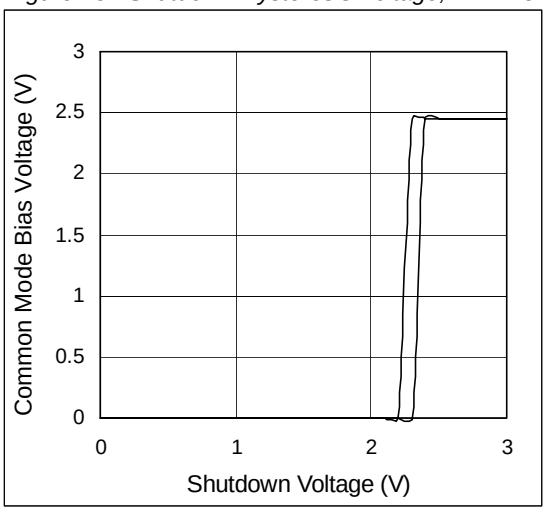


*Figure 26. Shutdown Current vs. Temperature*

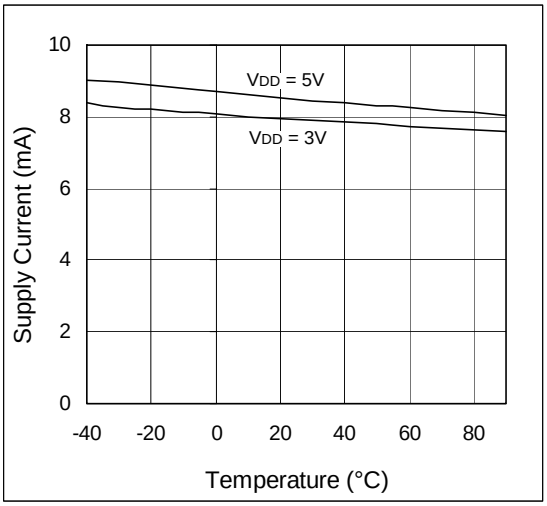



*Figure 27. Shutdown Current vs. Temperature*

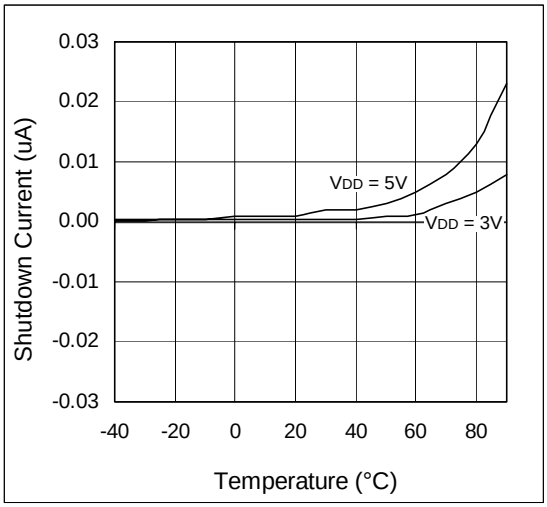
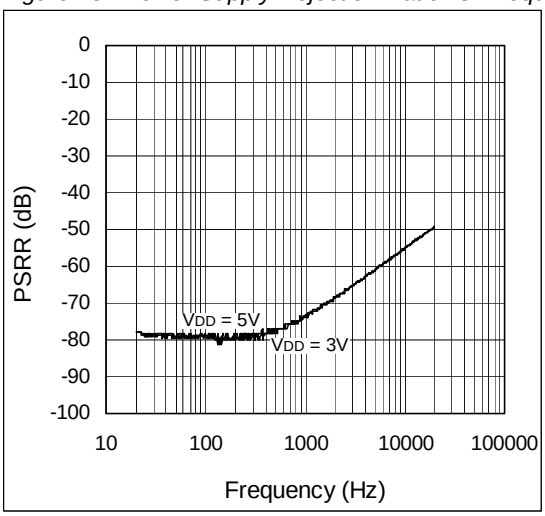


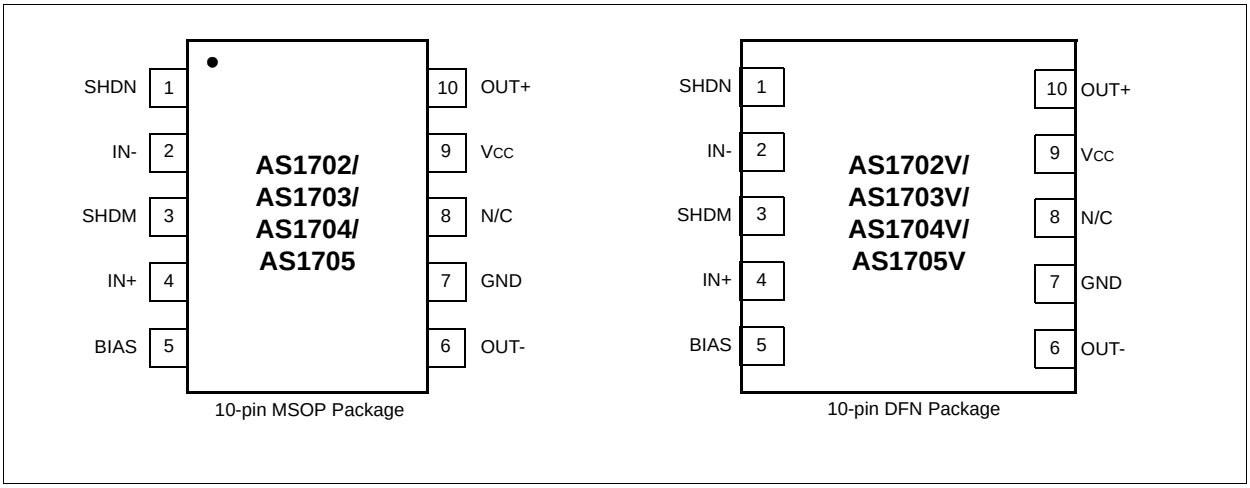

*Figure 28. Power Supply Rejection Ratio vs. Frequency*



# 7 Pinout

## Pin Assignments

*Figure 29. Pin Assignments (Top View)*




## Pin Descriptions

*Table 5. Pin Descriptions – MSOP-10 and TDFN-10 Package*

| Pin | Name | Description |
|---|---|---|
| 1 | SHDN | **Shutdown Input**. The polarity of this pin is dependent on the state of pin SHDM. |
| 2 | IN- | **Inverting Input** |
| 3 | SHDM | **Shutdown-Mode Polarity Input**. This pin controls the polarity of pin SHDN. Connect this pin high for an active-high SHDN input. Connect this pin low for an active-low SHDN input (see Table 6 on page 11). |
| 4 | IN+ | **Non-Inverting Input** |
| 5 | BIAS | **DC Bias Bypass** |
| 6 | OUT- | **Bridge Amplifier Negative Output** |
| 7 | GND | **Ground** |
| 8 | N/C | **Not Connected**. No internal connection. |
| 9 | VCC | **Power Supply** |
| 10 | OUT+ | **Bridge Amplifier Positive Output** |

# 8 Detailed Description

The AS1702 - AS1705 are 1.8W high output-current audio amplifiers (configured as BTL amplifiers), and contain integrated low-power shutdown and click- and pop-suppression circuitry. Two inputs (SHDM and SHDN) allow shutdown mode to be configured as active-high or active-low (see Shutdown Mode on page 11).

Each device has either adjustable or fixed gains (0dB, 3dB, 6dB) (see Ordering Information on page 19).

## Bias

The devices operate from a single 2.7 to 5.5V supply and contain an internally generated, common-mode bias voltage of:

$$\frac{V_{CC}}{2} \quad \text{(EQ 1)}$$

referenced to ground. Bias provides click-and-pop suppression and sets the DC bias level for the audio outputs. Select the value of the bias bypass capacitor as described in Section BIAS Capacitor on page 15.

**Note:** Do not connect external loads to BIAS as this can adversely affect overall device performance.

## Shutdown Mode

All devices implement a 100nA, low-power shutdown circuit which reduces quiescent current consumption. As shutdown mode commences, the bias circuitry is automatically disabled, the device outputs go high impedance, and bias is driven to GND.

The SHDM input controls the polarity of SHDN:

- Drive SHDM high for an active-low SHDN input.
- Drive SHDM low for an active-high SHDN input.

*Table 6. Shutdown Mode Selection Configurations*

| SHDM | SHDN | Mode |
|---|---|---|
| 0 | 0 | Shutdown Mode Enabled |
| 0 | 1 | Normal Operation Enabled |
| 1 | 0 | Normal Operation Enabled |
| 1 | 1 | Shutdown Mode Enabled |

## Click-and-Pop Suppression

During power-up, the device common-mode bias voltage ($V_{BIAS}$ (see page 3)) ramps to the DC bias point. When entering shutdown, the device outputs are driven high impedance to 100kΩ between both outputs minimizing the energy present in the audio band, thus preventing clicks and pops.

# 9 Application Information

*Figure 30. AS1702 Typical Application Diagram*

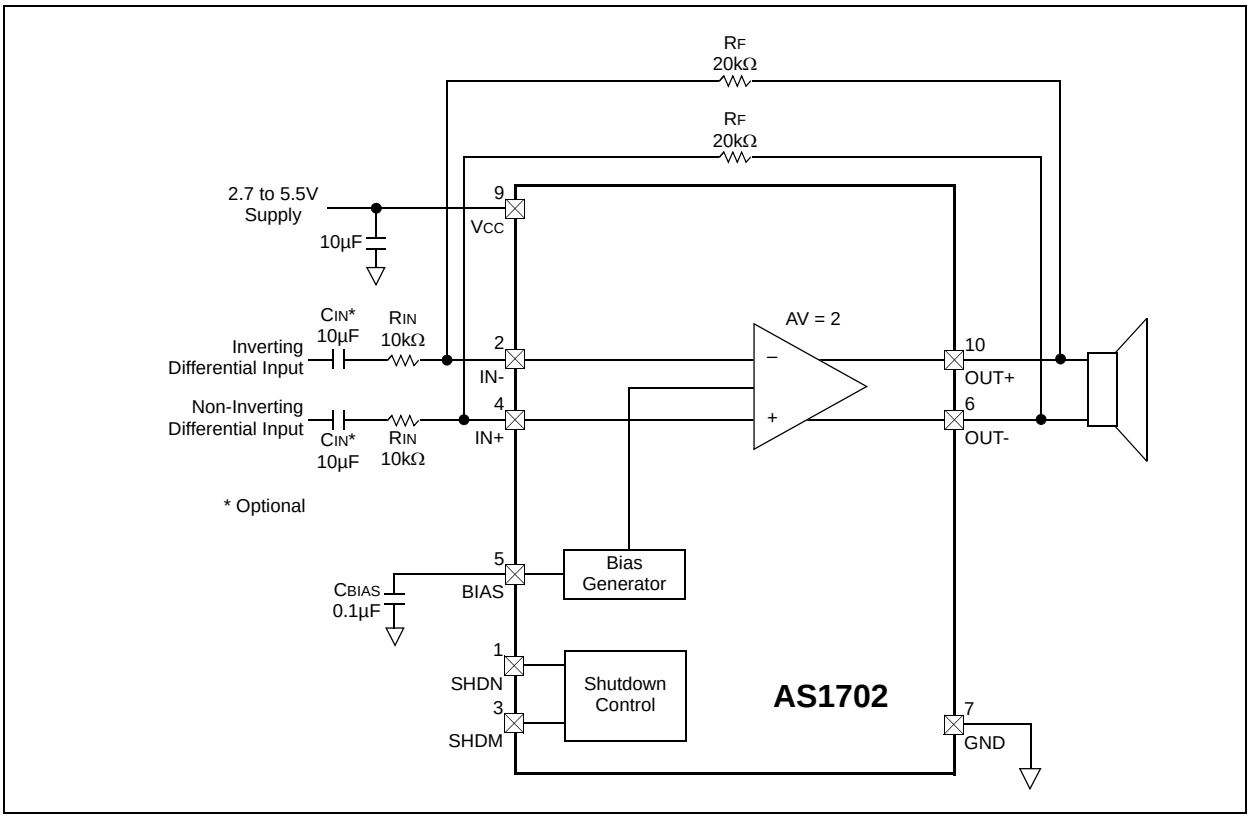
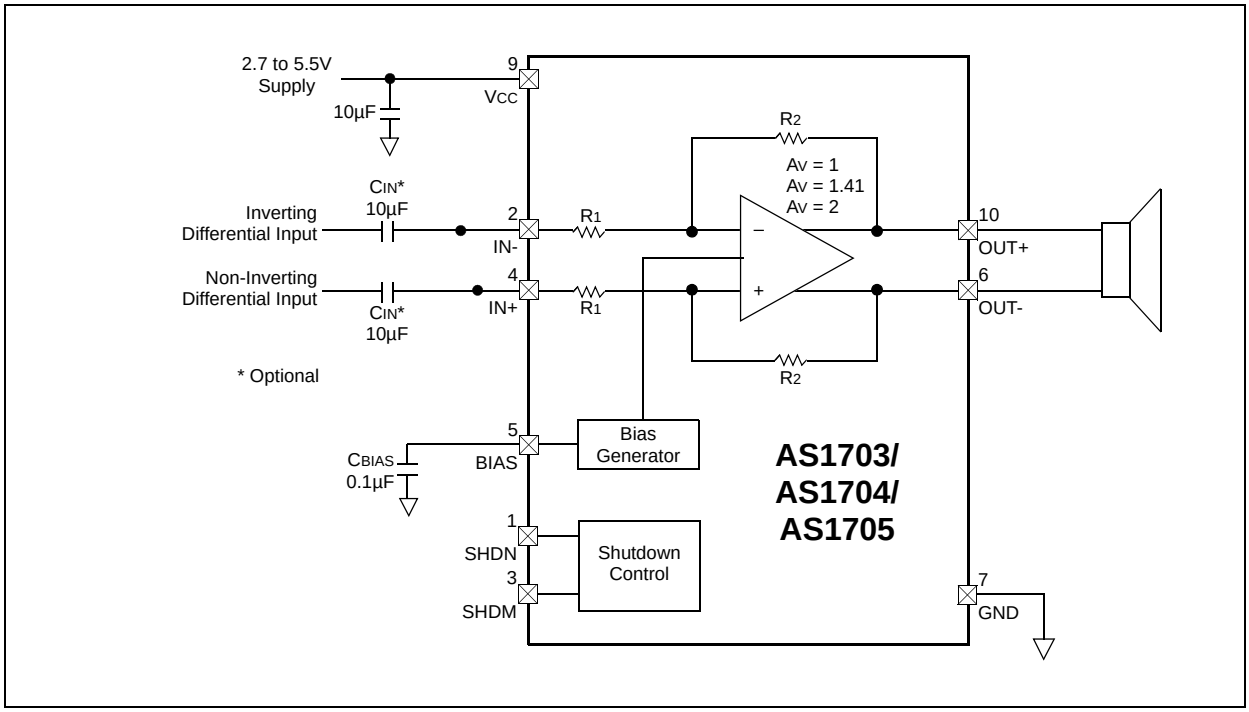


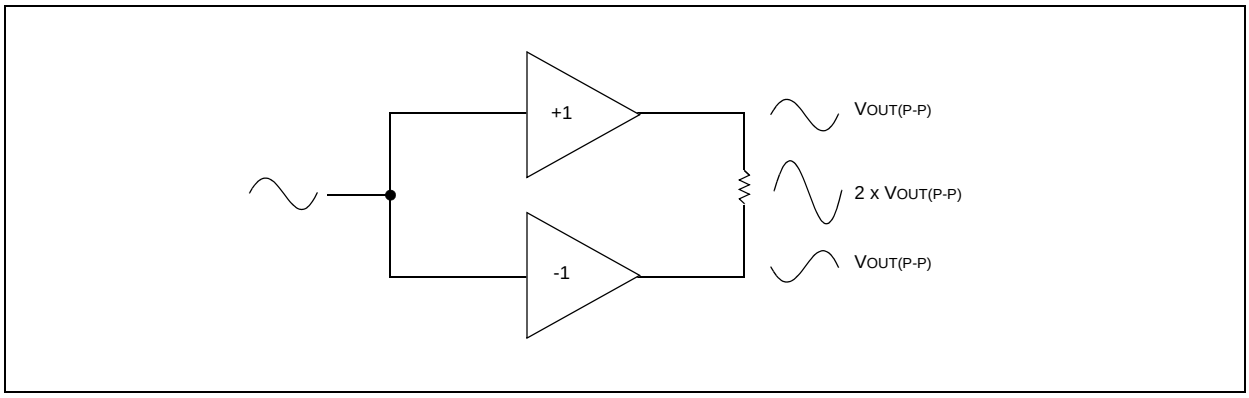

*Figure 31. AS1703, AS1704, AS1705 Typical Application Diagram*



## BTL Amplifier

All devices are designed to drive loads differentially in a bridge-tied load (BTL) configuration.

*Figure 32. Bridge Tied Load Configuration*




The BTL configuration doubles the output voltage (illustrated in Figure 32) compared to a single-ended amplifier under similar conditions. Thus, the differential gain of the device ($A_{VD}$) is twice the closed-loop gain of the input amplifier. The effective gain is given by:

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}} \quad \text{(EQ 2)}$$

Substituting 2 x $V_{OUT(P-P)}$ for $V_{OUT(P-P)}$ into (EQ 3) and (EQ 4) yields four times the output power due to doubling of the output voltage:

$$V_{RMS} = \frac{V_{OUT(P-P)}}{2\sqrt{2}} \quad \text{(EQ 3)}$$

$$P_{OUT} = \frac{V_{RMS}^2}{R_L} \quad \text{(EQ 4)}$$

Since the BTL outputs are biased at mid-supply, there is no net DC voltage across the load. This eliminates the need for the large, expensive, performance degrading DC-blocking capacitors required by single-ended amplifiers.

## Power Dissipation and Heat Sinking

Normally, the devices dissipate a significant amount of power. The maximum power dissipation is given in Table 2 as Continuous Power Dissipation, or it can be calculated by:

$$P_{DISSPKF(MAX)} = \frac{T_{J(MAX)} - T_A}{\Theta_{JA}} \quad \text{(EQ 5)}$$

where $T_{J(MAX)}$ is +150ºC, $T_{AMB}$ (see Table 2) is the ambient temperature, and $\Theta_{JA}$ is the reciprocal of the derating factor in ºC/W as specified in Table 2. For example, $\Theta_{JA}$ of the TQFN package is +59.2ºC/W.

The increased power delivered by a BTL configuration results in an increase in internal power dissipation versus a single-ended configuration. The maximum internal power dissipation for a given $V_{CC}$ and load is given by:

$$P_{DISSPKF(MAX)} = \frac{2V_{CC}^2}{\pi^2 R_L} \quad \text{(EQ 6)}$$

If the internal power dissipation exceeds the maximum allowed for a given package, power dissipation should be reduced by increasing the ground plane heat-sinking capabilities and increasing the size of the device traces (see Layout and Grounding Considerations on page 15). Additionally, reducing $V_{CC}$, increasing load impedance, and decreasing ambient temperature can reduce device power dissipation.

The integrated thermal-overload protection circuitry limits the total device power dissipation. Note that if the junction temperature is ≥ +145ºC, the integrated thermal-overload protection circuitry will disable the amplifier output stage. If the junction temperature is reduced by 9°, the amplifiers will be re-enabled.

**Note:** A pulsing output under continuous thermal overload results as the device heats and cools.

## Fixed Differential Gain (AS1703, AS1704, and AS1705)

The AS1703, AS1704, and AS1705 contain different internally-fixed gains (see Ordering Information on page 19). A fixed gain facilitates simplified designs, decreased footprint size, and elimination of external gain-setting resistors.

The fixed gain values are achieved using resistors $R_1$ and $R_2$ (see Figure 31 on page 12).

## Adjustable Differential Gain (AS1702)

### Gain-Setting Resistors

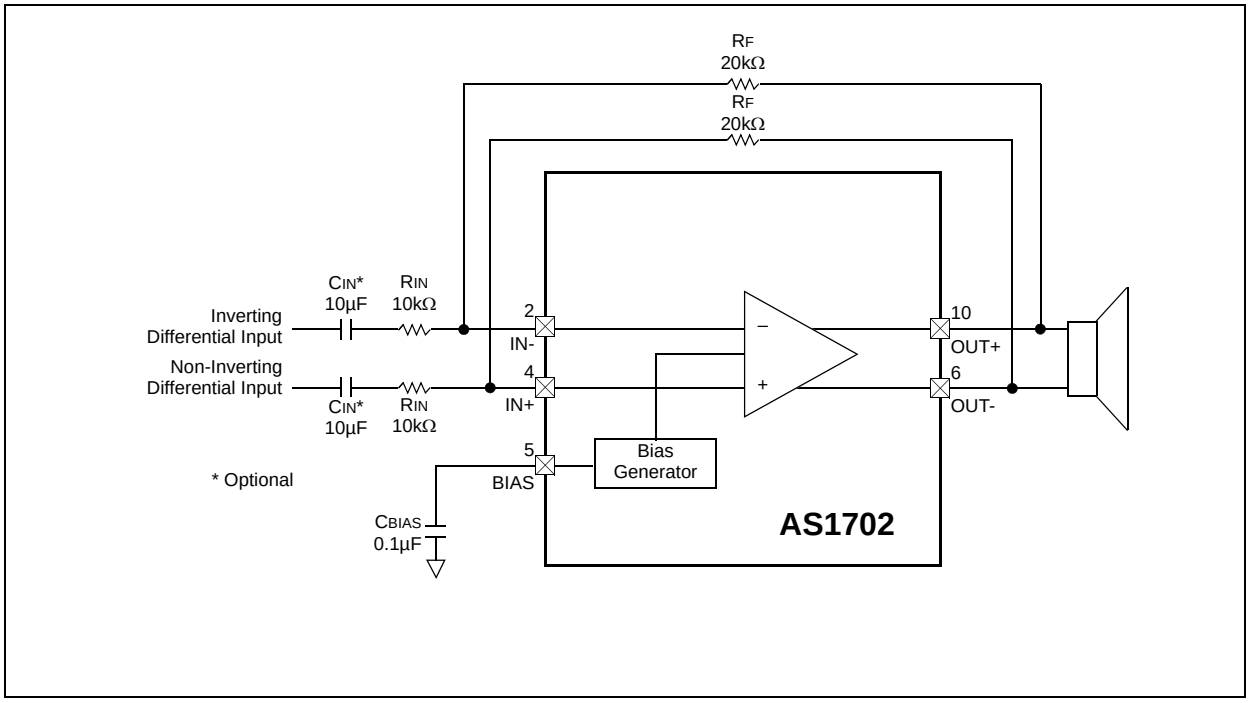
The AS1702 uses external feedback resistors, $R_F$ and $R_{IN}$ (Figure 33), to set the gain of the device as:

$$A_V = \frac{R_F}{R_{IN}} \qquad \text{(EQ 7)}$$

where $A_V$ is the desired voltage gain. For example, $R_{IN}$ = 10kΩ, $R_F$ = 20kΩ yields a gain of 2V/V, or 6dB.

**Note:** $R_F$ can be either fixed or variable, allowing the gain to be controlled by software (using a AS150x digital potentiometer. For more information on the AS1500 family of digital potentiometers, refer to the latest version of the AS150x data sheet, available from the austriamicrosystems website http://www.austriamicrosystems.com.)

*Figure 33. Setting the AS1702 Gain*



### Input Filter

The BTL inputs can be biased at voltages other than mid-supply. However, the integrated common-mode feedback circuit adjusts for input bias, ensuring the outputs are still biased at mid-supply. Input capacitors are not required if the common-mode input voltage ($V_{IC}$) is within the range specified in Table 3 and Table 4.

Input capacitor $C_{IN}$ (if used), in conjunction with $R_{IN}$, forms a high-pass filter that removes the DC bias from an incoming signal. The AC coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the high-pass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{(EQ 8)}$$

Setting $f_{-3dB}$ too high affects the low-frequency response of the amplifier. Capacitors with dielectrics that have low-voltage coefficients such as tantalum or aluminum electrolytic should be used, since capacitors with high-voltage coefficients, such as ceramics, can increase distortion at low frequencies.

### BIAS Capacitor

BIAS is the output of the internally generated $V_{CC}/2$ bias voltage. The BIAS bypass capacitor, $C_{BIAS}$, improves PSRR and THD+N by reducing power supply noise and other noise sources at the common-mode bias node, and also generates the click- and pop-less DC bias waveform for the amplifiers. Bypass BIAS with a 0.1µF capacitor to GND. Larger values of $C_{BIAS}$ (up to 1µF) improve PSRR, but increase $t_{ON}/t_{OFF}$ times. For example, a 1µF $C_{BIAS}$ capacitor increases $t_{ON}/t_{OFF}$ by 10 and improves PSRR by 20dB (at 1kHz).

**Note:** Do not connect external loads to BIAS.

### Supply Bypassing

Proper power supply bypassing – connect a 10µF ceramic capacitor ($C_{BIAS}$) from $V_{CC}$ to GND – will ensure low-noise, low-distortion performance of the device. Additional bulk capacitance can be added as required.

**Note:** Place $C_{BIAS}$ as close to the device as possible.

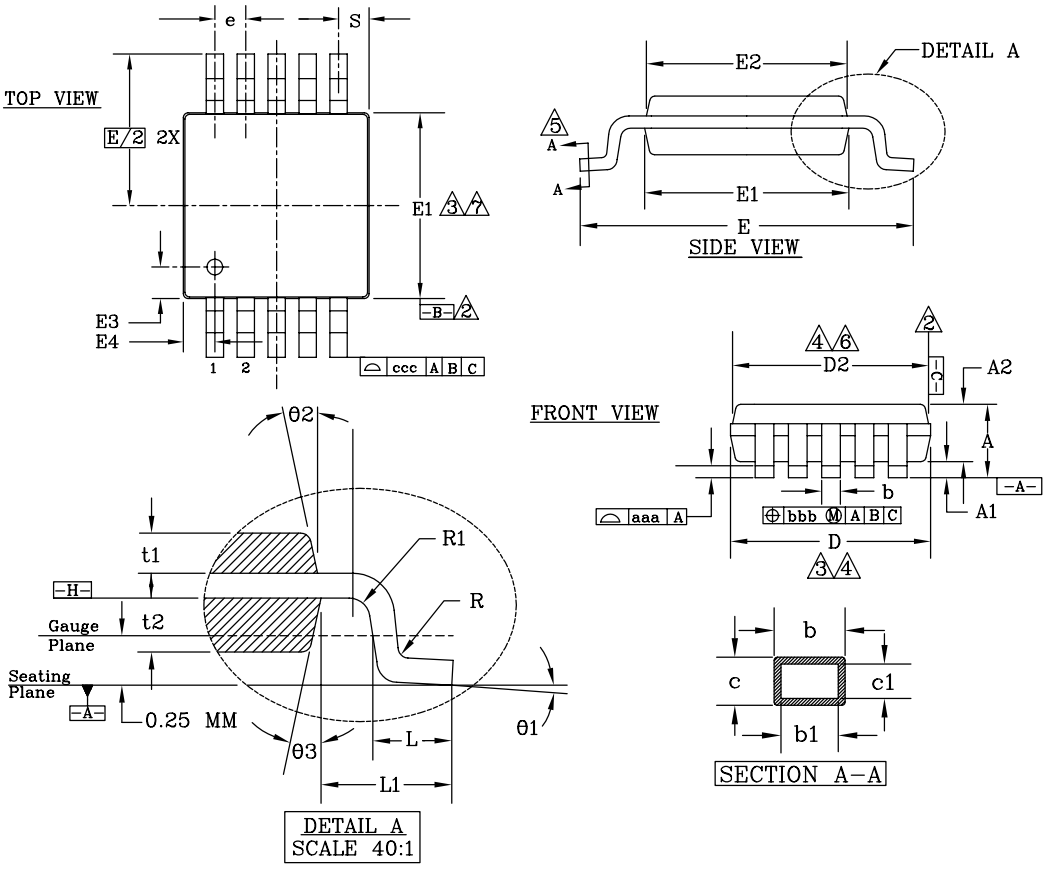
## Layout and Grounding Considerations

Well designed PC board layout is essential for optimizing device performance. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance and route heat away from the device.

Good grounding improves audio performance and prevents digital switching noise from coupling onto the audio signal.

# 10 Package Drawings and Markings

*Figure 34. 10-pin MSOP Package*

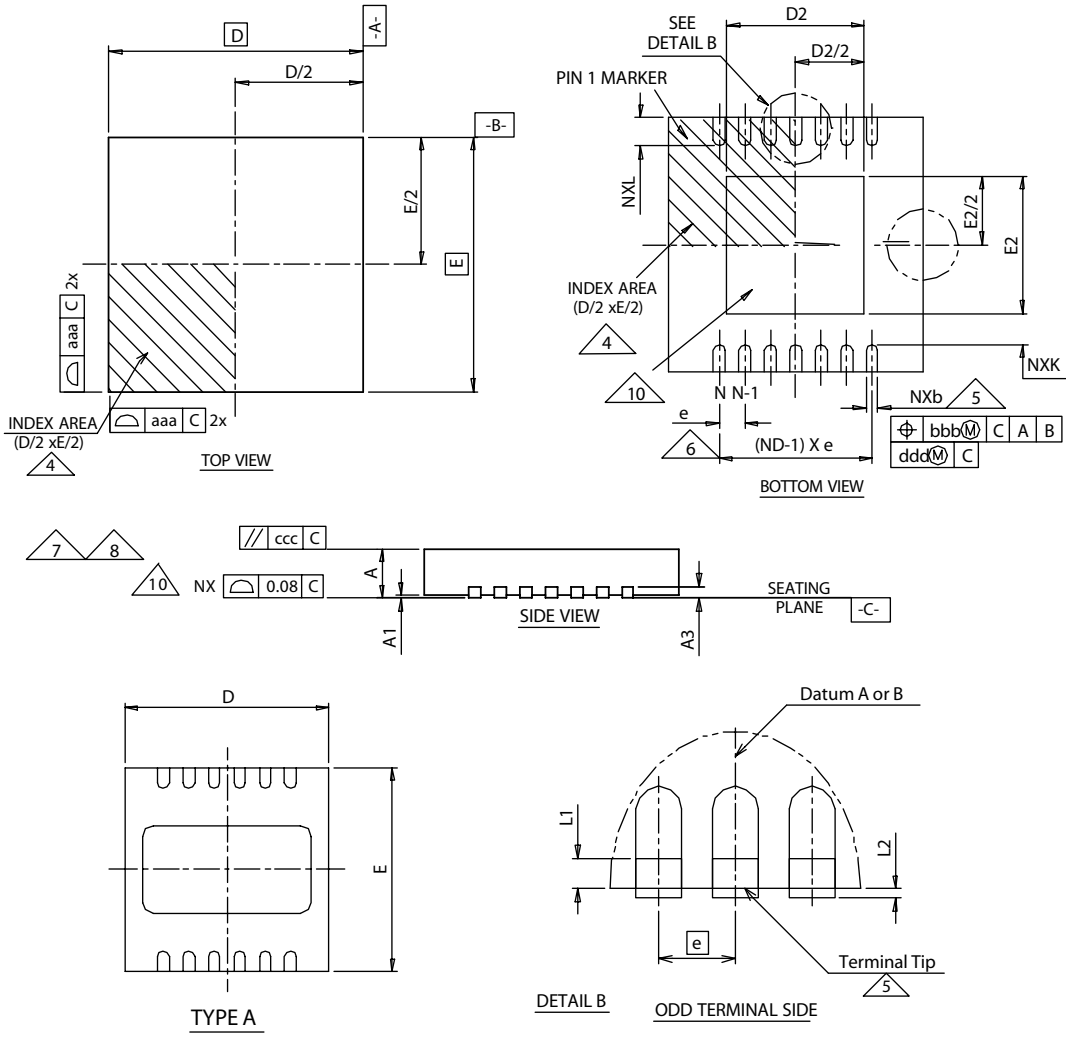



| Symbol | Typ | ±Tol | Symbol | Typ | ±Tol |
|---|---|---|---|---|---|
| A | 1.10 | Max | b | 0.23 | +0.07/-0.08 |
| A1 | 0.10 | ±0.05 | b1 | 0.20 | ±0.05 |
| A2 | 0.86 | ±0.08 | c | 0.18 | ±0.05 |
| D | 3.00 | ±0.10 | c1 | 0.15 | +0.03/-0.02 |
| D2 | 2.95 | ±0.10 | θ1 | 3.0º | ±3.0º |
| E | 4.90 | ±0.15 | θ2 | 12.0º | ±3.0º |
| E1 | 3.00 | ±0.10 | θ3 | 12.0º | ±3.0º |
| E2 | 2.95 | ±0.10 | L | 0.55 | ±0.15 |
| E3 | 0.51 | ±0.13 | L1 | 0.95BSC | - |
| E4 | 0.51 | ±0.13 | aaa | 0.10 | - |
| R | 0.15 | +0.15/-0.08 | bbb | 0.08 | - |
| R1 | 0.15 | +0.15/-0.08 | ccc | 0.25 | - |
| t1 | 0.31 | ±0.08 | e | 0.50 BSC | - |
| t2 | 0.41 | ±0.08 | S | 0.50 BSC | - |

**Notes:**

1. All dimensions are in millimeters (angle in degrees), unless otherwise specified.
2. Datums B and C to be determined at datum plane H.
3. Dimensions D and E1 are to be determined at datum plane H.
4. Dimensions D2 and E2 are for top package and D and E1 are for bottom package.
5. Cross section A-A to be determined at 0.12 to 0.25mm from the lead tip.
6. Dimensions D and D2 do not include mold flash, protrusion, or gate burrs.
7. Dimension E1 and E2 do not include interlead flash or protrusion.

*Figure 35. 10-pin DFN Package (3.0x3.0mm)*




| Symbol | Min | Typ | Max | Notes |
|---|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 | 1, 2 |
| A1 | 0.00 | 0.02 | 0.05 | 1, 2 |
| A3 | | 0.20 REF | | 1, 2 |
| L1 | | | 0.15 | 1, 2 |
| L2 | | | 0.13 | 1, 2 |
| θ | 0º | | 14º | 1, 2 |
| K | 0.20 | | | 1, 2 |
| K2 | 0.17 | | | 1, 2 |
| b | 0.18 | 0.25 | 0.30 | 1, 2, 5 |
| e | | 0.5 | | |
| aaa | | 0.15 | | 1, 2 |
| bbb | | 0.10 | | 1, 2 |
| ccc | | 0.10 | | 1, 2 |
| ddd | | 0.05 | | 1, 2 |
| eee | | 0.08 | | 1, 2 |
| ggg | | 0.10 | | 1, 2 |

| Variations | | | | |
|---|---|---|---|---|
| **Symbol** | **Min** | **Typ** | **Max** | **Notes** |
| D BSC | | 3.00 | | 1, 2 |
| E BSC | | 3.00 | | 1, 2 |
| D2 | 2.20 | | 2.70 | 1, 2 |
| E2 | 1.40 | | 1.75 | 1, 2 |
| L | 0.30 | 0.40 | 0.50 | 1, 2 |
| N | | 10 | | 1, 2 |
| ND | | 5 | | 1, 2, 5 |

# 11 Ordering Information

The devices are available as the standard products shown in Table 7.

*Table 7. Ordering Information*

| Model | Description | Gain | Package Type | Delivery Form |
|---|---|---|---|---|
| AS1702-T | 1.8W Single-Channel Audio Power Amplifier | Adjustable | 10-pin MSOP, 3x3x0.8mm | Tape and Reel |
| AS1703-T | | Av = 0dB | | |
| AS1704-T | | Av = 3dB | | |
| AS1705-T | | Av = 6dB | | |
| AS1702V-T | | Adjustable | 10-pin DFN, 3x3x0.8mm | Tape and Reel |
| AS1703V-T | | Av = 0dB | | |
| AS1704V-T | | Av = 3dB | | |
| AS1705V-T | | Av = 6dB | | |

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