HFM1202

Ethernet Receiver

FEATURES

- -35 dBm to -12 dBm sensitivity
- Differential data outputs (ECL compatible)
- Signal Quality Detect and Packet Detect outputs (open collector)
- Adjustable signal quality detect level
- ST® interface
- 500 Ω output drive capability
- Monolithic design - less board space, high reliability

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DESCRIPTION

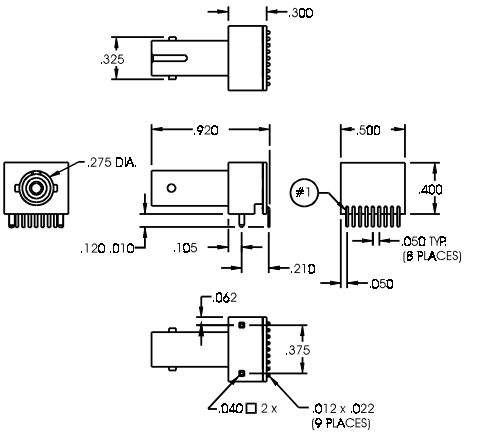
The HFM1202-331 Ethernet fiber optic receiver module is designed for use in computer LAN (10 Mb/s Ethernet) applications. The 9 pin Next Generation module is intended for use in applications such as IEEE 802.3 10 BASE FB/FL and FOIRL signal standards. A PIN photodiode plus pre-amp is mounted in the fiber optic connector for maximum shielding, and provides amplification and current-to-voltage conversion. The post-amp IC provides final amplification to the logic output levels (see BLOCK DIAGRAM). Signal Quality Detect, Packet Detect and Differential Data outputs are available. Differential ECL compatible data minimizes pulse width distortion and allows capacitive coupling to ECL logic. The HFM1202 has a 500 Ω output drive capability on each data output. An internally regulated power supply increases power supply rejection.

Case ground is separated from circuit ground, allowing feedthrough mounting of the barrel.

APPLICATION

Average-to-peak input level monitoring aids in the generation of the signal quality logic signal ($\overline{SQ}$) when the input level is adequate for 10^{-10} BER. The open collector output timing response of $\overline{SQ}$ is intended to meet 802.3 requirements over -32.5 dBm to -12 dBm average power levels. An additional current source output (SQLED) is available to drive an external LED indicator (LED ON indicates poor signal quality). If this output is not used, it should be tied to +12 V.

OUTLINE DIMENSIONS in inches (mm)



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Pinout

1. GND ground
2. Vcc
3. Output +
4. Output -
5. Hi GND
6. $\overline{PKT}$
7. SQ LED
8. $\overline{SQ}$
9. ADJ

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APPLICATION (continued)

Resistor R_{ADJ} adjusts the $\overline{SQ}$ threshold upward. A 70 µA current from this node to ground increases the threshold by 1 dB of optical power. R_{ADJ}'s high side is at 4.3 V (nominal).

The open collector output ($\overline{PKT}$) indicates presence of a valid Ethernet packet. This output goes low following the first two data edges that are 200 ns or less apart at the start of a packet. It returns high before the end of the first cycle of a valid 1 MHz idle signal.

The HFM1202 is designed to operate with a 12 V supply (normally present in FOIRL interfaces and personal computer backplanes). The module requires a minimum +8.5 V total voltage. If a +12 V supply is not available, +5 V to V_{CC} pin and -5 V to GND pin will operate the module. Since the outputs are typically AC coupled, this voltage shift is generally not a problem. Data out2 (+) is positive with respect to data out1 (-) when no light is present at the optical input.

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ELECTRO-OPTICAL CHARACTERISTICS (Over 0 to 70°C, V_{CC} = 11.25 to 15.75 VDC unless otherwise stated)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Data Rate			10		Mbd	Manchester coding
Input Power		-35		-12	dBm	Average power (10^{-10} BER)
Supply Current			32	43	mA	Excluding $\overline{SQ}$, SQLED, $\overline{PKT}$
Propagation Delay			28	40	ns	
Jitter (uncorrelated)			0.4	0.6	ns	RMS, -32.5 dBm average input
Pulse Width Distortion (1)				7	ns	$\overline{SQ}$ Low, -12 dBm average input
Signal Quality Detect ($\overline{SQ}$) (2)			-35	-32.5	dBm average	Threshold for $\overline{SQ}$, high to low Transition
Signal Quality Detect Hysteresis			-1.3		dB	Threshold change for $\overline{SQ}$ low to high transition
Delay Time (acceptable level) (3)				4	µs	P_{IN} > -30 dBm average
Delay Time (unacceptable level)		3		20	µs	P_{IN} < -12 dBm average
Packet Detection ($\overline{PKT}$)						Bit times @ 10 Mbd (with < 20 p_F and 4 kΩ load)
Delay of Packet Start				2		
End of Packet Delay				4		
Optical Idle Signal						
Frequency		0.85	1	1.25	MHz	PKT DE assertion
Duty Cycle		45		55	%	
Output (Out1/Out2)						
Load		500			Ω	
Output Swing		1	1.6		V	Peak to peak
			+1000		ppm/°C	Over temperature
$\overline{SQ}$/$\overline{PKT}$ V_{OL}				0.4	V	I_{OL} ≤ 3 mA
SQLED Sink Current			12		mA	

Notes

1. Using a 10 MHz square wave input optical signal; t_r= 7 ns, t_f= 10 ns. The maximum PWD specified could be achieved by the user in system operation at 70°C.
2. Using R_{ADJ} = infinity Ohms.
3. See Figure 1.

ABSOLUTE MAXIMUM RATINGS

(25°C Free-Air Temperature unless otherwise noted)

Supply voltage (V_{CC})	8.5 to 15.75 V
Temperature	-40 to +85°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Supply voltage (V_{CC})	11.25 to 12.75 V
Temperature	0 to +70°C

ORDER GUIDE

Description	Catalog Listing
Fiber Optic Ethernet Receiver, 9 pin package	HFM1202-331

CAUTION

The inherent design of this component causes it to be sensitive to electrostatic discharge (ESD). To prevent ESD-induced damage and/or degradation to equipment, take normal ESD precautions when handling this product.

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FIBER INTERFACE

Honeywell receivers are designed to interface with multimode fibers (50/125 to 200/230 micron diameter). Final testing is performed with a 62.5/125 micron core fiber. Low cost 50/125 and 62.5/125 micron fibers are good for high bandwidth applications. 100/140 and 200/230 micron fibers result in greater power coupling by the transmitter, making it easier to splice or connect in bulkhead areas.

BLOCK DIAGRAM

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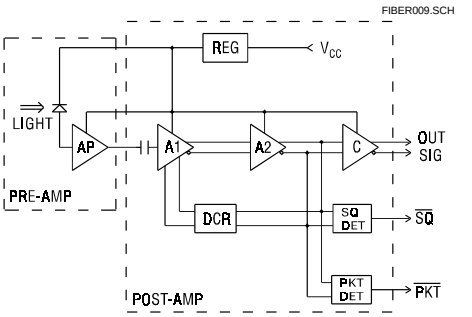

TYPICAL CIRCUIT CONFIGURATION

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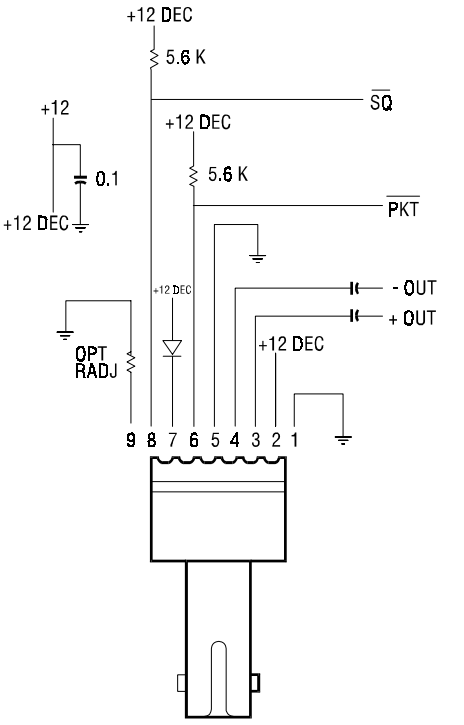

Fig. 1 SQ Transition Delay vs Power

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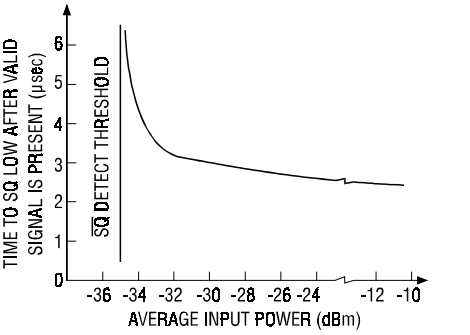

Fig. 2 Spectral Responsivity

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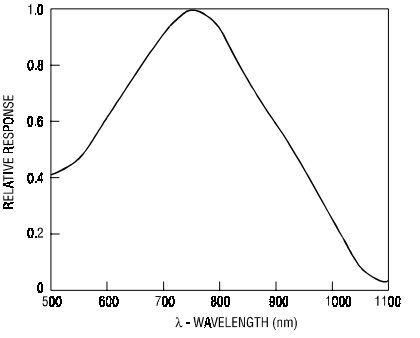

All Performance Curves Show Typical Values

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