

Low-power, High-performance $\Delta\Sigma$ Modulators

Features

- Fourth-order $\Delta\Sigma$ Architecture
- Clock-jitter-tolerant Architecture
- Input Voltage: 5 V_{pp} Fully Differential
- High Dynamic Range
 - 127 dB SNR @ 215 Hz BW (2 ms Output)
 - 124 dB SNR @ 430 Hz BW (1 ms Output)
- Low Total Harmonic Distortion
 - -118 dB THD Typical, -112 dB THD Maximum
- Low Power Consumption
 - Normal Mode: 25 mW per Channel
 - Low-power Mode: 15 mW per Channel
- Small Footprint, 24-pin SSOP Package
- Single- or Multi-channel System Support
 - 1-channel System: CS5371
 - 2-channel System: CS5372
 - 3-channel System: CS5371 + CS5372
 - 4-channel System: CS5372 + CS5372
- Single or Dual Power Supply Configurations
 - VA+ = +5 V; VA- = 0 V; VD = +3.3 V to +5 V
 - VA+ = +2.5 V; VA- = -2.5 V; VD = +3.3 V

Description

The CS5371 and CS5372 are one- and two-channel, high dynamic range, fourth-order $\Delta\Sigma$ modulators intended for geophysical and sonar applications. Used in combination with the CS5376A or CS5378 digital filters, a unique high-resolution A/D measurement system results.

The CS5371 and CS5372 have high dynamic range (127 dB @ 215 Hz bandwidth) and low total harmonic distortion (typically -118 dB THD), with very low power consumption per channel. In normal mode (LPWR=0, MCLK=2.048MHz), power consumption is 25 mW per channel, and in low-power mode (LPWR=1, MCLK=1.024MHz), power consumption is 15 mW per channel. Each modulator can be independently powered down to 1 mW per channel, and by halting the input clock, they will enter a micropower state using only 10 μ W per channel.

The modulators generate an oversampled serial bit stream at 512 kbits per second when operated from a clock frequency of 2.048 MHz. They are available in a small 24-pin SSOP package, providing exceptional performance in a very small footprint.

ORDERING INFORMATION

See [page 21](#).

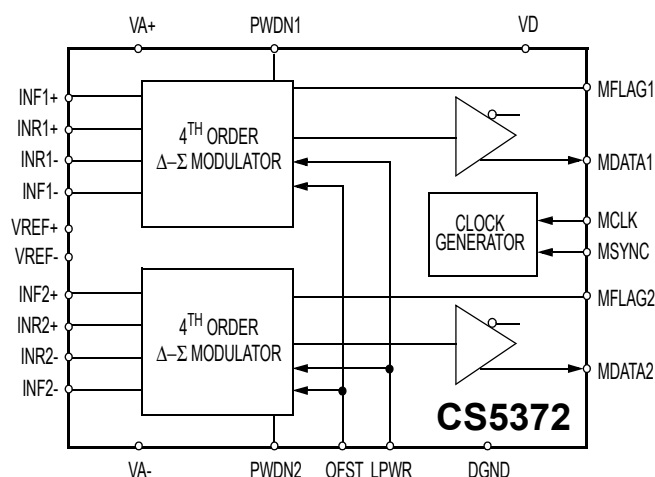
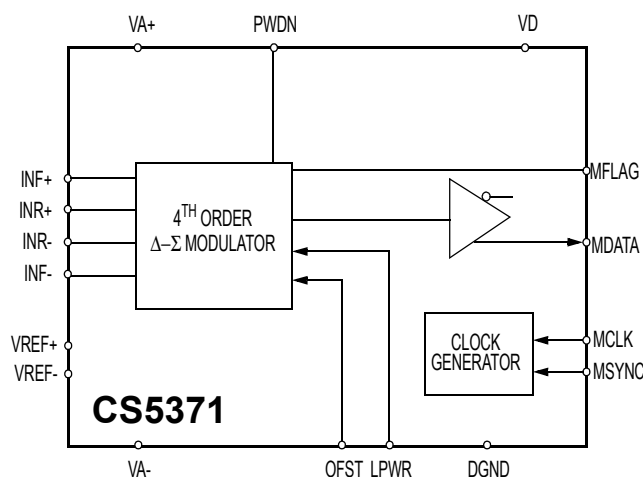


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1. CHARACTERISTICS & SPECIFICATIONS

ANALOG CHARACTERISTICS Notes: $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{A+} = 5\text{V}$ or $2.5\text{V} \pm 5\%$; $V_{A-} = 0\text{V}$ or $-2.5\text{V} \pm 5\%$; $V_D = 5\text{V}$ or $3.3\text{V} \pm 5\%$; $DGND = 0\text{V}$; $MCLK = 2.048\text{ MHz}$; $[(VREF+) - (VREF-)] = 2.5\text{V}$; Devices are connected as shown in Figure 3, the System Connection Diagram.

Parameter	Symbol	CS5371-BS / CS5372-BS			Unit
		Min	Typ	Max	
Specified Temperature Range	T_A	-40	-	+85	$^{\circ}\text{C}$
Dynamic Performance					
Dynamic Range (Note 1) LPWR = 0 MCLK = 2.048 MHz	SNR	-	109	-	dB
0 Hz to 1720 Hz		-	121	-	dB
0 Hz to 860 Hz		121	124	-	dB
0 Hz to 430 Hz		-	127	-	dB
0 Hz to 215 Hz		-	130	-	dB
0 Hz to 107.5 Hz		-	133	-	dB
0 Hz to 53.75 Hz		-	136	-	dB
0 Hz to 26.875 Hz		-		-	dB
Dynamic Range (Note 1) LPWR = 1 MCLK = 1.024 MHz	SNR_{LP}	-	106	-	dB
0 Hz to 1720 Hz		-	118	-	dB
0 Hz to 860 Hz		118	121	-	dB
0 Hz to 430 Hz		-	124	-	dB
0 Hz to 215 Hz		-	127	-	dB
0 Hz to 107.5 Hz		-	130	-	dB
0 Hz to 53.75 Hz		-	133	-	dB
0 Hz to 26.875 Hz		-		-	dB
Total Harmonic Distortion (Note 2) LPWR = 0; MCLK = 2.048 MHz	THD	-	-118	-112	dB
Total Harmonic Distortion (Note 2) LPWR = 1; MCLK = 1.024 MHz	THD_{LP}	-	-114	-108	dB
DC Accuracy					
Channel to Channel Gain Variation (Note 3)	CGV	-	1	-	%
Full-scale Drift (Notes 3 and 4)	TC_{FS}	-	5	-	ppm/ $^{\circ}\text{C}$
Offset (Note 3)	V_{ZSE}	-	1	-	mV
Offset after Calibration (Note 5)		-	± 1	-	μV
Offset Calibration Range (Note 6)		-	100	-	%F.S.
Offset Drift (Notes 3 and 4)	TC_{ZSE}	-	1	-	$\mu\text{V}/^{\circ}\text{C}$

- Notes:
1. Dynamic Range defined as $20 \log [(\text{RMS full scale}) / (\text{RMS idle noise})]$
 2. Tested with full-scale input signal of 31.25 Hz; OWR = 1000 SPS; OFST = 1.
 3. Specification is for the parameter over the specified temperature range for the CS5371/72 devices only and does not include the effects of external components.
 4. Specifications are guaranteed by design and/or characterization.
 5. The offset after calibration specification applies to the effective offset voltage for a full-scale input to the CS5371/72 modulator, but is measured from the output digital codes from the digital filter.
 6. The CS5371/72 offset calibration is performed digitally and includes the full-scale range.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Specified Temperature Range	T_A	-40	-	+85	C
Input Characteristics					
Input Signal Frequencies (Note 7)	BW	DC	-	1720	Hz
Input Voltage Range (Note 8)	VIN	-	-	5	V _{p-p}
Input Over-range Voltage Tolerance (Note 8)	I _{OV} R	5	-	-	%F.S.
Input Signal plus Common Mode		(VA-) + 0.7V	-	(VA+) - 1.7V	V
Common Mode Rejection Ratio	CMRR	-	90	-	dB
Channel Crosstalk (CS5372 only)	CXT	-	-120	-	dB
Voltage Reference Input					
VREF (VREF+) - (VREF-)		-	2.5	-	V
VREF Current		-	-	120	μA
Power Supplies					
DC Power Supply Currents (Note 9 and 10)					
LPWR = 0; MCLK = 2.048 MHz	Analog	VA	-	5.0	7.0 mA
	Digital	VD	-	0.2	0.3 mA
LPWR = 1; MCLK = 1.024 MHz	Analog	VA	-	3.0	4.5 mA
	Digital	VD	-	0.2	0.3 mA
Power Down Modes	P _D				
CS5371 PWDN = 1		-	1	-	mW
PWDN = 1, MCLK = 0		-	10	-	μW
CS5372 PWDN1 or PWDN2 = 1		-	25	-	mW
PWDN1 = PWDN2 = 1		-	1	-	mW
PWDN1 = PWDN2 = 1, MCLK = 0		-	10	-	μW
Power Supply Rejection (Note 11)	PSRR	-	90	-	dB

- Notes:
- The upper bandwidth limit is determined by the digital filter. A simple single pole anti-alias filter with a -3 dB frequency at (MCLK / 256) should be placed in front of each channel.
 - The input voltage range is for the configuration depicted in Figure 3, the System Connection Diagram, and applies to signal frequencies from DC to the stop-band frequency selected in the digital filter.
 - Per channel. All outputs unloaded. All digital inputs forced to VD or GND respectively.
 - In Low Power Mode LPWR = 1, the Master Clock MCLK is reduced to 1.024 MHz. This reduces the oversampled signal bandwidth by a factor of 2.
 - Tested with a 50 Hz 100 mVpp sine wave applied separately to each supply.

DIGITAL CHARACTERISTICS Notes: $T_A = 25\text{ }^{\circ}\text{C}$; $V_{A+} = 5\text{V}$ or $2.5\text{V} \pm 5\%$; $V_{A-} = 0\text{V}$ or $-2.5\text{V} \pm 5\%$; $V_D = 5\text{V}$ or $3.3\text{V} \pm 5\%$; $DGND = 0\text{V}$; All voltages with respect to $DGND$.

Parameter	Symbol	Min	Typ	Max	Unit
High-level Input Voltage	V_{IH}	$0.6 * V_D$	-	V_D	V
Low-level Input Voltage	V_{IL}	0.0	-	0.8	V
High-level Output Voltage $I_{out} = -5.0\text{ mA}$	V_{OH}	$(V_D) - 1.0$	-	-	V
Low-level Output Voltage $I_{out} = 5.0\text{ mA}$	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	± 1	± 10	μA
3-state Leakage Current	I_{OZ}	-	-	± 10	μA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

ABSOLUTE MAXIMUM RATINGS Notes: $DGND = 0\text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supplies (Notes 12 and 13)					
Positive Digital	V_D	-0.3	-	+6.0	V
Positive Analog	V_{A+}	-0.3	-	+6.0	V
Negative Analog	V_{A-}	-3.3	-	+0.3	V
Input Current, Any Pin Except Supplies (Note 14 and 15)	I_{IN}	-	-	± 10	mA
Input Current, Supplies (Note 15)	I_{IN}	-	-	± 50	mA
Output Current	I_{OUT}	-	-	± 25	mA
Power Dissipation (Note 16)	PDN	-	-	500	mW
Analog Input Voltage All Analog Pins	V_{INA}	$(V_{A-}) - 0.5$	-	$(V_{A+}) + 0.5$	V
Digital Input Voltage All Digital Pins	V_{IND}	-0.5	-	$(V_D) + 0.5$	V
Ambient Operating Temperature	T_A	-40	-	85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-65	-	150	$^{\circ}\text{C}$

- Notes: 12. V_{A+} and V_{A-} must satisfy $\{(V_{A+}) - (V_{A-})\} < +6.8\text{ V}$.
13. V_D and V_{A-} must satisfy $\{(V_D) - (V_{A-})\} < +7.6\text{ V}$.
14. Includes continuous over-voltage conditions at the analog input (AIN) pins.
15. Transient current of up to 100 mA can be safely tolerated without SCR latch-up.
16. Total power dissipation, including all input and output currents.

SWITCHING CHARACTERISTICS

Notes: $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{A+} = +5\text{V}$ or $+2.5\text{V} \pm 5\%$; $V_{A-} = 0\text{V}$ or $-2.5\text{V} \pm 5\%$; $V_D = +5\text{V}$ or $+3.3\text{V} \pm 5\%$; Digital Inputs: Logic 0 = 0V, Logic 1 = V_D ; $C_L = 50\text{ pF}$

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Frequency (Note 17)	f_c	0.1	2.048	2.2	MHz
MCLK Duty Cycle		40	-	60	%
MCLK Jitter (In-band or aliased in-band)		-	-	300	ps
MCLK Jitter (Out-of-band)		-	-	1	ns
Rise Times: Any Digital Input (Note 18)	t_{risein}	-	-	50	ns
Any Digital Output	t_{riseout}	-	50	100	ns
Fall Times: Any Digital Input (Note 18)	t_{fallin}	-	-	50	ns
Any Digital Output	t_{fallout}	-	50	100	ns
MSYNC Setup Time to MCLK falling (Note 19)	t_{mss}	20	-	-	ns
MSYNC Hold Time after MCLK falling	t_{msh}	20	-	-	ns
MCLK rising to Valid MFLAG	t_{mfh}	-	35	65	ns
MCLK rising to Valid MDATA	t_{mdv}	-	60	90	ns

Notes: 17. If MCLK is removed, the CS5372 enters a micro power state.

18. Excludes MCLK input, MCLK should be driven with a signal having rise/fall times of 25 ns or faster.

19. MSYNC latched on MCLK falling edge, data output on next MCLK rising edge.



Figure 1. Rise and Fall Times

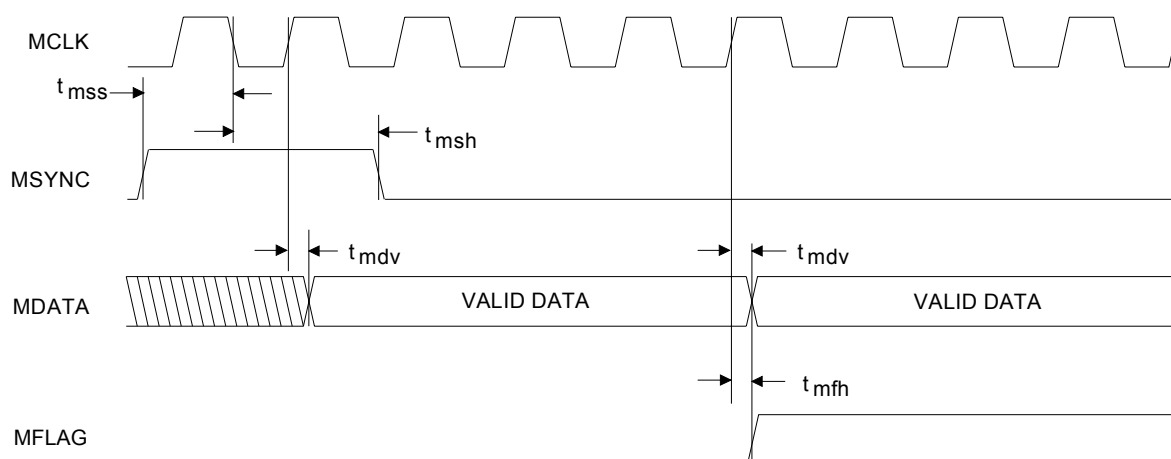


Figure 2. CS5372 Interface Timing

2. GENERAL DESCRIPTION.

The CS5371 and CS5372 are one- and two- channel fourth-order $\Delta\Sigma$ modulators, optimized for extremely high-resolution measurement of signals between DC and 1600 Hz. They are designed to be used with the CS5376A and CS5378 low-power digital filters. Figure 3 on page 8 shows a four-channel system connection diagram for two CS5372 and one CS5376A.

High Performance

The CS5371/72 modulators have exceptional performance characteristics. Modulator dynamic range (SNR) is 127 dB over a 215 Hz bandwidth (2 ms sampling), with total harmonic distortion (THD) of -118 dB.

Low Power Consumption

The CS5371/72 modulators have very low power consumption. Power consumption is only 25 mW per channel in normal mode (LPWR=0, MCLK=2.048 MHz), and 15 mW per channel in low power mode (LPWR=1, MCLK=1.024 MHz).

An independently selectable power-down mode (PWRDN=1) can be used to disable a modulator and reduces its power consumption to 1 mW. If MCLK is then halted (MCLK=0), the modulator enters a micropower state using only 10 μ W per channel.

Small Package Size

The CS5371/72 modulators are available in a very small 24-pin SSOP package approximately 8 mm x 8 mm in size. The CS5372 has two modulator channels per package to increase board layout density even further.

Multi-channel System Support

Combining the CS5371 and CS5372 modulators with a digital filter permits multiple system configurations:

- 1 Channel - CS5371, CS5378
- 2 Channel - CS5372, CS5376A
- 3 Channel - CS5371, CS5372, CS5376A
- 4 Channel - CS5372, CS5372, CS5376A

Differential Analog Signal Inputs

The CS5371/72 modulators have fully differential analog inputs capable of measuring signals up to 5.0 V peak-to-peak when using a 2.5 V voltage reference. The inputs will tolerate a 5% over-range voltage and continue operating at full specification.

Digital Filter Interface

The CS5371/72 modulators are designed to operate with the CS5376A and CS5378 digital filters. The digital filter generates the modulator clock and synchronization signal inputs (MCLK and MSYNC), while receiving the modulator data and over-range flag outputs (MDATA and MFLAG). The modulators produce an oversampled $\Delta\Sigma$ serial bit stream at 512 kbits per second when operated from a 2.048 MHz modulator clock.

Multiple Power Supply Configurations

The CS5371/72 modulators support flexible power supply configurations. They can run from single or dual supplies in the following configurations:

- VA+ = +5V; VA- = 0V; VD = +3.3V to +5V
- VA+ = +2.5V; VA- = -2.5V; VD = +3.3V

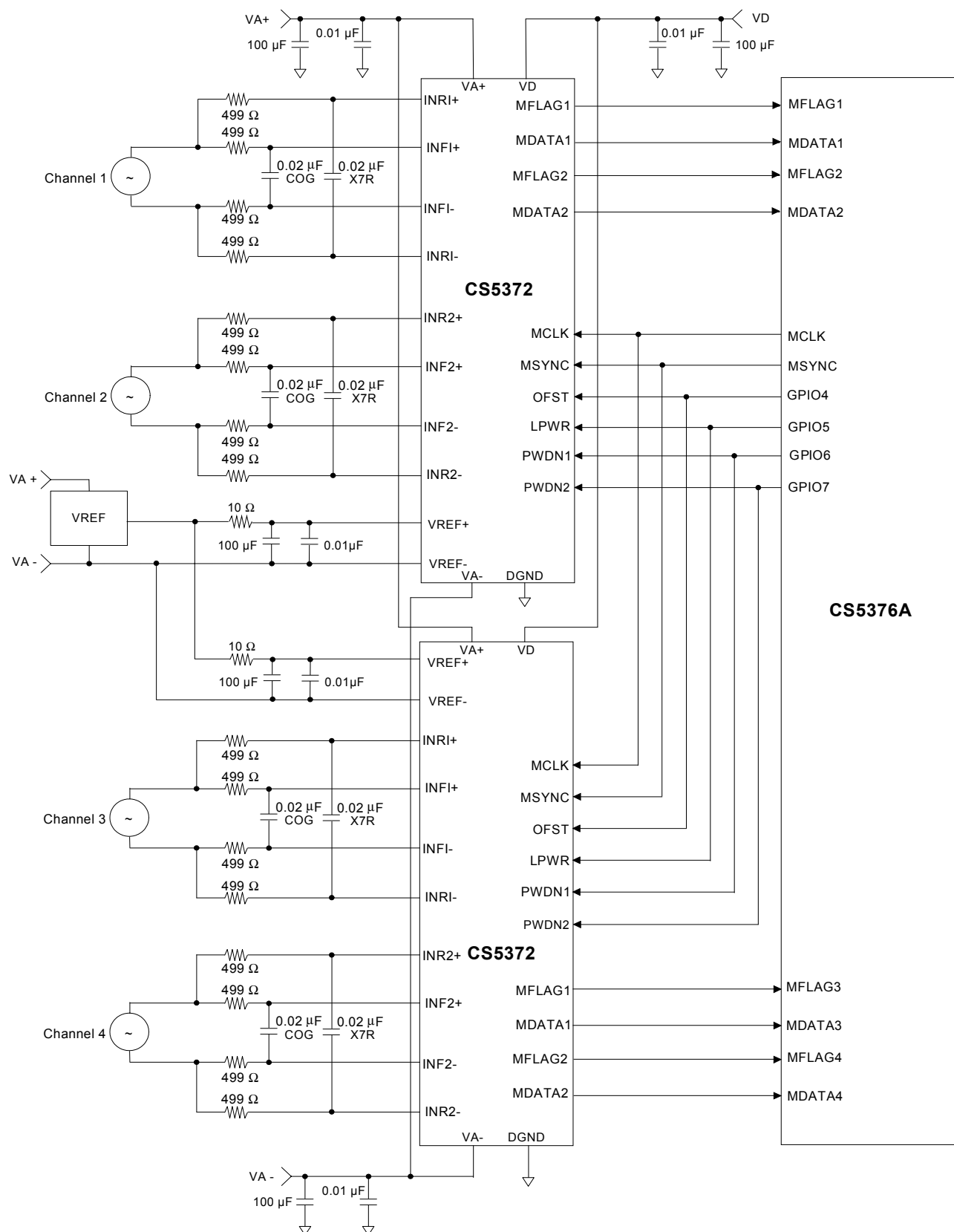


Figure 3. System Connection Diagram

3. MODULATOR PERFORMANCE

Figures 4 and 5 illustrate the spectral performance of the CS5371/72 modulators when combined with the CS5376A or CS5378 digital filter. The plots were created from ten averaged 1024 point FFTs.

3.1. Full-scale Signal Performance

Figure 4 illustrates the full-scale signal performance of the CS5371/72 modulators and digital filter using a 31.25 Hz input signal and a 1000 SPS output word rate. The outstanding full-scale signal characteristics of the CS5371/72 modulators are shown, with no harmonic components exceeding -120 dB. Analysis of this data set yields a signal-to-noise ratio (SNR) of 124.0 dB and a signal-to-distortion ratio (SDR) of 119.0 dB. Note that the full-scale signal peak in Figure 4 shows a slightly reduced amplitude due to spectral smearing associated with the FFT windowing function, and is a purely digital phenomenon.

3.2. Noise Performance

Figure 5 illustrates the noise performance of the CS5371/72 modulators and digital filter using a 31.25 Hz -24 dB input signal at a 1000 SPS output word rate. The outstanding noise characteristics of the CS5371/72 modulators are shown, with the averaged noise components consistently below the -150 dB level. Analysis of this data set yields a dynamic range of 124.7 dB. Note that the 0.7 dB

variation between the signal-to-noise calculation in Figure 4 and the dynamic range calculation in Figure 5 is not modulator dependent and results from jitter in the test signal generator when producing a full-scale output, as evidenced by the skirt surrounding the signal peak below the -140 dB level in Figure 4.

4. SIGNAL INPUTS

The CS5371/72 modulators use a switched capacitor architecture for the analog signal inputs, which has increased jitter tolerance compared with continuous time signal input stages.

4.1. Differential Inputs - INR+/-, INF+/-

The analog signal inputs are differential and use four pins: INR+, INR-, INF+, and INF-. Two inputs, INR+ and INF+, are connected to the positive half of the differential signal, while two inputs, INR- and INF-, are connected to the negative half. The INR+ and INR- pins are switched capacitor 'rough charge' inputs that pre-charge the internal sampling capacitor before it is connected to the INF+ and INF- fine input pins.

The full-scale analog signal span is defined by the voltage applied across the VREF+ and VREF- pins. A 2.5 volt reference input sets full-scale signals as 5 volts peak-to-peak, fully differential. Differential inputs increase the dynamic range of

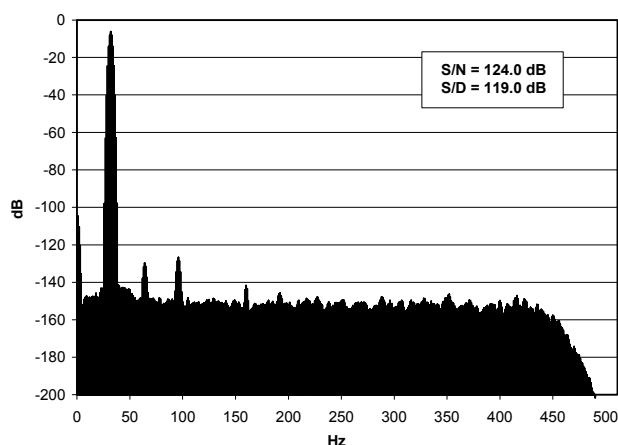


Figure 4. 1024 Point FFT plot with a 31.25 Hz input at Full-scale, ten averages

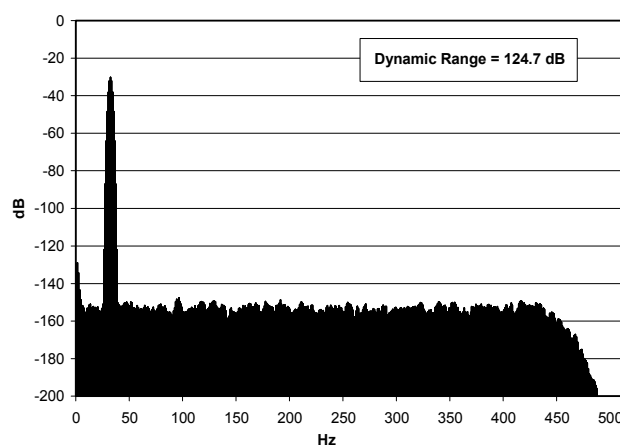


Figure 5. 1024 Point FFT plot with a 31.25 Hz input at -24 dB, ten averages

small signals, reducing the gain requirements for input amplifier stages by a factor of two relative to single ended analog inputs.

4.2. Anti-alias Filters

The CS5371/72 modulator inputs must be bandwidth limited to ensure modulator loop stability and to prevent aliased high-frequency signals. The modulators are 4th order and so are conditionally stable, and can be adversely affected by high amplitude out-of-band signals. Also, aliasing effects degrade modulator performance if the analog inputs are not bandwidth limited since out-of-band signals can appear in the measurement bandwidth. The use of a simple single pole low-pass anti-alias filter on the differential inputs ensures out-of-band signals are eliminated.

Anti-alias filtering may be accomplished actively in an amplifier stage ahead of the CS5371/72 modulator, or passively using an RC filter across the differential rough and fine analog inputs. An RC filter is recommended, even when using an amplifier stage, as it minimizes the 'charge kick' that the driving amplifier sees as switched capacitor sampling is performed.

The -3 dB corner of the input anti-alias filter should be set to the internal modulator sampling clock divided by 64. The modulator sampling clock is a division by 4 of the modulator clock, MCLK. With MCLK=2.048 MHz the modulator sampling clock is 512 kHz, requiring an input filter with a -3 dB corner at 8 kHz.

$$\text{MCLK Frequency} = 2.048 \text{ MHz}$$

$$\text{Sampling Frequency} = \text{MCLK} / 4 = 512 \text{ kHz}$$

$$\text{-3 dB Filter Corner} = \text{Sample Freq} / 64 = 8 \text{ kHz}$$

$$\text{RC filter} = 8 \text{ kHz} = 1 / [2\pi * (2 * R_{\text{diff}}) * C_{\text{diff}}]$$

It should be noted that when using low power mode (LPWR=1 and MCLK=1.024 MHz) the modulator sampling clock is 256 kHz, so the -3 dB filter corner should be scaled down to 4 kHz.

$$\text{MCLK Frequency} = 1.024 \text{ MHz}$$

$$\text{Sampling Frequency} = \text{MCLK} / 4 = 256 \text{ kHz}$$

$$\text{-3 dB Filter Corner} = \text{Sample Freq} / 64 = 4 \text{ kHz}$$

$$\text{RC filter} = 4 \text{ kHz} = 1 / [2\pi * (2 * R_{\text{diff}}) * C_{\text{diff}}]$$

Figure 3 illustrates the CS5372/CS5376A system connections with input anti-alias filter components. Filter components on the rough and fine pins should be identical values for optimum performance, with the capacitor values a minimum of 0.02 μF . The rough input can use either X7R or C0G capacitors, while the fine input requires C0G type capacitors for optimal linearity. Using X7R capacitors on the fine inputs will degrade signal to distortion performance up to 8 dB.

4.3. Input Impedance

Due to the dynamic switched-capacitor input architecture, the input current required from the analog signal source and thus the input impedance of the analog input pins changes any time MCLK is changed. The input impedance of the rough charge inputs, INR+ and INR-, is $[1 / (f * C)]$ where f is the modulator clock frequency, MCLK, and C is the internal sampling capacitor. A 2.048 MHz modulator clock yields a rough input impedance of approximately $[1 / (2.048 \text{ MHz}) * (20 \text{ pF})]$, or about 24 k Ω .

Internal to the modulator the rough charge inputs pre-charge the sampling capacitor used by the fine inputs, therefore the input current to the fine inputs is very low and the effective input impedance is orders of magnitude above the impedance of the rough inputs.

4.4. Maximum Signal Levels

The CS5371/72 modulators are 4th order and are therefore conditionally stable, and may go into an oscillatory condition if the analog inputs over-range beyond full scale by more than 5%. If an unstable condition is detected, the modulators collapse to a 1st order system until loop stability is achieved. During this time, the MFLAG pin transitions from low to high signaling the digital filter to set an error bit in the digital output status word. The analog input signal must be reduced to within the full-scale range of the converter for at least 32 MCLK cycles for the modulators to recover from an unstable condition.

5. INPUT OFFSET

The CS5371/72 modulators are $\Delta\Sigma$ type and so can produce 'idle tones' in the passband when the

input signal is a steady state DC signal within ± 50 mV of the common mode input voltage. Idle tones result from patterns in the output bitstream and appear in the measurement spectrum about -135 dB down from full scale.

Idle tones can be eliminated by adding differential DC offset to the modulator inputs. The added offset should be applied differentially to the inputs, common mode offsets do not affect idle tones.

5.1. Offset Enable - OFST

If the analog inputs are near the common mode voltage when no signal is present, the OFST pin can be used to eliminate idle tones. When OFST=1, -50 mV of differential offset is added to the modulator analog inputs to push the idle tones out of the measurement bandwidth. Care should be taken that when OFST is active, offset voltages generated by external circuitry do not negate the internally added offset.

5.2. Offset Drift

Offset drift characteristics vary from part to part and with changes in the power supply voltages. If the CS5371/72 is used in precision DC measurement applications where offset drift is to be minimized, the power supplies should be well regulated.

For the lowest offset drift, the CS5371/72 modulators should operate with an MCLK of 2.048 MHz. The offset drift rate is inversely proportional to clock frequency, with slower modulator clock rates exhibiting more offset drift. Operating from an MCLK of 1.024 MHz results in twice the offset drift rate compared to an MCLK of 2.048 MHz.

Because offset drift is not linear with temperature, an exact drift rate per $^{\circ}\text{C}$ cannot be specified. The CS5371/72 modulators will exhibit approximately 5 ppm/ $^{\circ}\text{C}$ of offset drift operating with an MCLK of 2.048 MHz.

6. VOLTAGE REFERENCE INPUTS

The CS5371/72 modulators are designed to operate with a 2.5 V voltage reference applied across the VREF+ and VREF- pins to set the full-scale signal range of the analog inputs. A 2.5 V voltage reference results in the highest dynamic range and best signal-to-noise performance, though smaller reference voltages may be used. When the CS5371/72 modulators are operated with a 2.5 V reference, the analog inputs measure full-scale signals of 5 volts peak-to-peak fully differential.

In a single supply power configuration the voltage reference output should be connected to the VREF+ pin with the VREF- pin connected to ground. In a dual supply power configuration the voltage reference should be powered from the VA+ and VA- supplies, with the modulator VREF+ pin connected to the voltage reference output and the VREF- pin connected to VA-. Because most 2.5 V voltage references require a power supply voltage greater than 3 V to operate, when powering the voltage reference from dual supplies the reference voltage into the VREF+ pin should be defined relative to the VA- supply.

The selected voltage reference should produce less than 1 μV_{rms} of noise in the measurement bandwidth on the VREF+ pin. The digital filter output word rate selection determines the bandwidth

over which voltage reference noise affects the CS5371/72 modulator dynamic range.

6.1. Voltage Reference Configurations

For a 2.5 V reference, the Linear Technology LT1019-2.5 voltage reference yields low enough noise if the output is filtered with a low pass RC filter as shown in Figure 6. The filtered version in Figure 6 is acceptable for most spectral measurement applications, but a buffered version with lower source impedance may be preferred for DC measurement applications.

6.2. VREF Input Impedance

The switched-capacitor input architecture of the VREF+ pin causes the input current required from the voltage reference to change any time MCLK is changed. The input impedance of the voltage reference input is calculated similar to the analog signal input impedance as $[1 / (f * C)]$ where f is the modulator clock frequency, MCLK, and C is the internal sampling capacitor. A 2.048 MHz MCLK yields a voltage reference input impedance of approximately $[1 / (2.048 \text{ MHz}) * (20 \text{ pF})]$, or about 24 k Ω .

6.3. Gain Accuracy

Gain accuracy of the CS5371/72 modulators is affected by variations of the voltage reference input. A change in the voltage reference input impedance due to a change in MCLK could affect gain accuracy

when using the higher source impedance configuration of Figure 6. The VREF+ pin input impedance and the external low-pass filter resistor create a voltage divider for the output reference voltage, reducing the effective voltage reference input. If gain error is to be minimized, especially when MCLK is to be changed, the voltage reference should have a low output impedance to minimize the effect of the resistive voltage divider. A buffered voltage reference configuration offers lower output impedance and more stable gain characteristics.

6.4. Gain Drift

Gain drift of the CS5371/72 modulators due to temperature is around 5 ppm/ $^{\circ}\text{C}$, and does not include the temperature drift characteristics of the external voltage reference. Gain drift is not affected by the modulator sample rate or by power supply variations.

7. DIGITAL FILTER INTERFACE

The CS5371/72 modulators are designed to operate with the CS5376A and CS5378 digital filters. The digital filter generates the modulator clock and synchronization signal inputs (MCLK and MSYNC), while receiving the modulator data and over-range flag outputs (MDATA and MFLAG). The modulators produce an oversampled $\Delta\Sigma$ serial

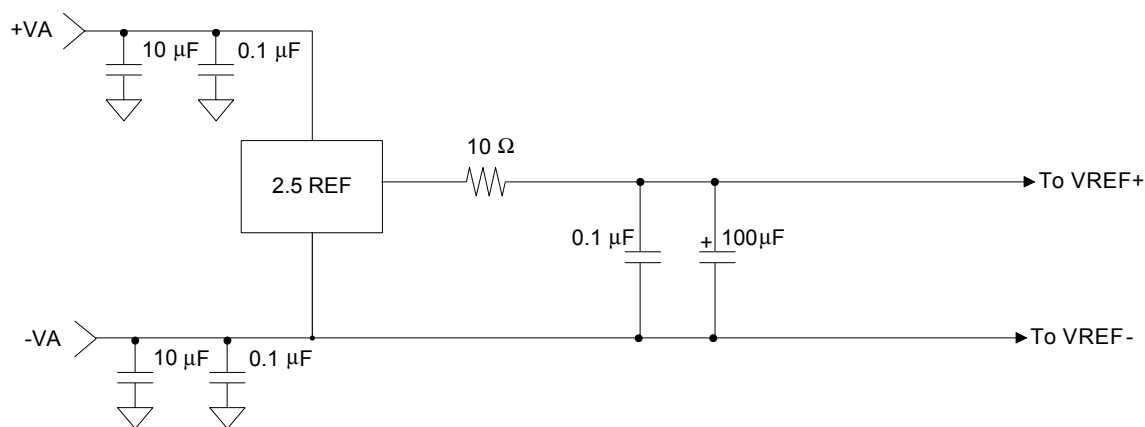


Figure 6. 2.5 Voltage Reference

bit stream at 512 kbits per second when operated from a 2.048 MHz modulator clock.

7.1. Modulator Clock - MCLK

For proper operation, the CS5371/72 modulators must be provided with a CMOS compatible clock on the MCLK pin. MCLK is internally divided by four to generate the modulator sampling clock. MCLK must have less than 300 ps of in-band jitter to maintain full performance specifications.

When used with the CS5376A or CS5378 digital filter, MCLK is automatically generated and is typically 2.048 MHz or 1.024 MHz. MCLK can be generated by other means, using a crystal oscillator for example, and can run any rate between 100 kHz and 2.2 MHz. If MCLK is disabled, the modulators are automatically placed into a micro-power state. They are equipped with loss of clock detection circuitry to force power down if MCLK is removed.

The choice of MCLK frequency affects the performance of the CS5371/72 modulators. They exhibit the best dynamic range (SNR) performance with faster MCLK rates because of increased oversampling of the analog input signal. The modulators exhibit the best total harmonic distortion (THD) performance with slower MCLK rates because slower sampling allows more time to settle the analog input signal.

7.2. Modulator Data - MDATA

The CS5371/72 modulators output a $\Delta\Sigma$ serial bitstream to the MDATA pin, with a one's density proportional to the amplitude of the analog input signal and a bit rate determined by the modulator sampling clock. The modulator sampling clock is a divide by four of MCLK, so for a 2.048 MHz MCLK the modulator sampling clock and MDATA output bit rate will be 512 kHz.

The MDATA output has a one's density defined as nominal 50% for no signal input, 86% for positive full scale, and 14% for negative full scale. It has a maximum positive over-range capability to 93% and a maximum negative over-range capability to 7%. The one's density of the MDATA output is defined as the ratio of '1' bits to total bits in the serial bitstream output, i.e. an 86% one's density has, on

average, a '1' value in 86 of every 100 output data bits.

When operated with the CS5376A or CS5378 digital filter, the full-scale 24-bit output codes range from 0x5D1C41 to 0xA2EAAE with the internal OFST disabled.

Modulator Input Signal	Digital Filter Output Code	
	OFST=0	OFST=1
> + (VREF + 5%)	Error Flag Possible	
+VREF	5D1C41	5B3A71
0V	000000	FE21D8
-VREF	A2EAAE	A108DE
> - (VREF + 5%)	Error Flag Possible	

Table 1. Output coding for the CS5371/72 and digital filter combination

Note that for a full-scale input signal, 5 V_{pp} with VREF=2.5 V, the CS5371/72 and CS5376A/78 chipset does not output a maximum 24-bit 2's complement digital code of 0x7FFFFFFF, but instead a lower scaled value to allow over-range capability.

7.3. Modulator Sync - MSYNC

To synchronize the analog sampling instant and timing of the digital output bitstream, the CS5371/72 modulators use an MSYNC signal. When using the CS5376A or CS5378 digital filter, MSYNC is automatically generated from a SYNC signal input from the external system.

The MSYNC input is rising edge triggered and resets the internal MCLK counter-divider so the analog sampling instant occurs during a consistent MCLK phase. It also sets the MDATA output timing so the bitstream can be properly sampled by the digital filter input.

7.4. Modulator Flag - MFLAG

The CS5371/72 modulators are 4th order $\Delta\Sigma$ and are therefore conditionally stable. The modulators may go into an oscillatory condition if the analog inputs are over-ranged more than 5% past either positive or negative fullscale.

If an unstable condition is detected, the modulators collapse to a 1st order system until loop stability is

achieved. During this time, the MFLAG pin transitions from low to high to signal an error condition. The analog input signal must be reduced to within the full-scale range for at least 32 MCLK cycles for the modulator to recover from an unstable condition.

The MFLAG output connects to a dedicated input on the digital filter, causing an error bit to be set in the status portion of the digital output data word when detected.

8. POWER MODES

Four power modes are available when using the CS5371/72 modulators. Normal power and low power modes are operational modes, power down and micro-power modes are non-operational standby modes.

8.1. Normal Power Mode

The normal operational mode for the modulators, LPWR=0 and MCLK=2.048 MHz, provides the best performance with power consumption of 25 mW per channel. This power mode is recommended when maximum conversion accuracy is required.

8.2. Low Power Mode - LPWR

The modulators have a low-power operational mode, LPWR=1 and MCLK=1.024 MHz, that reduces power consumption to 15 mW per channel at the expense of 3 dB of dynamic range. This operational mode is recommended when minimizing power is more important than maximizing dynamic range.

When operated with LPWR=1, the modulator sampling clock (MCLK / 4) must be restricted to rates of 256 kHz or less, which requires MCLK to run at 1.024 MHz or less. Operating in low power mode with modulator sample rates greater than 256 kHz will significantly degrade total harmonic distortion performance.

8.3. Power Down Mode - PWDN

The modulators have a power down mode, PWDN=1 and MCLK=Active, that disables the operation of the selected modulator channel and reduces its power consumption to 1 mW. Each modulator has an independent power down pin,

PWDN on the CS5371 and PWDN1, PWDN2 on the CS5372. Note that when the modulators are powered down and MCLK is active, the internal clock generator is still drawing minimal currents.

8.4. Micro-power Mode

Standby power consumption of the modulators can be minimized by placing them into a micro-power mode, PWDN=1 and MCLK=0. Micro-power mode requires setting the PWDN pin and halting MCLK to remove the clock generator input current. Micro-power mode consumes only 10 μ W of power.

9. POWER SUPPLY

The CS5371/72 modulators have one positive analog power supply pin, VA+, one negative analog power supply pin, VA-, one digital power supply pin, VD, and one digital ground pin, DGND. The analog and digital circuitry is separated internally to enhance performance, therefore power must be supplied to all three supply pins and the digital ground pin must be connected to system ground.

9.1. Power Supply Configurations

The CS5371/72 analog supplies can be powered by a single +5 V supply and analog ground, or by dual supplies of ± 2.5 V. When using dual supplies, the positive and negative analog power supplies must satisfy the following conditions:

$$(VA+) - (VA-) < 6.8 \text{ volts}$$

$$(VD) - (VA-) < 7.6 \text{ volts}$$

These conditions permit several power supply configurations.

- ♦ VA+ = +5V; VA- = 0V; VD+ = +3.3V to +5V
- ♦ VA+ = +2.5V; VA- = -2.5V; VD+ = +3.3V

When used with the CS5376A or CS5378 digital filter the maximum voltage differential between the modulator digital supply, VD, and the CS5376A/78 I/O supply, VDD2 or VDDPAD, must be 0.3V or less.

9.2. Power Supply Bypassing

The analog and digital supply pins, VA+, VA-, and VD, should be decoupled to system ground with 0.01 μ F and 10 μ F capacitors, or with a single 0.1 μ F capacitor. Bypass capacitors can be X7R, tantalum, or any other dielectric types.

9.3. SCR Latch-up Considerations

The VA- pin is tied to the CS5371/72 substrate and should always be connected to the most negative supply voltage to ensure SCR latch-up does not occur. In general, latch-up may occur when any pin voltage (including the analog inputs) is 0.7V or more below VA-, or 7.6V or more above VA-.

Analog inputs INR+/- and INF+/- should be voltage limited to ensure signals don't exceed the (VA-)-0.7V or (VA+)+7.6V requirement. Either the inputs should be clamped to the VA+ and VA- rails using reversed biased Schottky diodes (BAT85 or similar), or the current into the analog inputs should be limited to less than 10mA. By current limiting the analog inputs, the internal ESD diodes on the analog input pads will clamp the input signal to the proper level. Input currents greater than 10mA will overdrive the internal diodes, so external components are required.

When using dual analog power supplies, it is recommended to connect the VA- power supply pin to system ground (DGND) using a reversed biased Schottky diode. This configuration clamps the VA-

voltage a maximum of 0.3V above ground to ensure SCR latch-up does not occur during power up. If the VA+ power supply ramps before the VA- supply, the VA- voltage could be pulled above ground through the CS5371/72. If the VA- supply is unintentionally pulled 0.7 V above the DGND pin, SCR latch-up can occur.

9.4. DC-DC Converter Considerations

Many measurement systems are battery powered and utilize DC-DC converters to generate the necessary supply voltages for the system. To minimize the effects of interference, it is desirable to operate the DC-DC converter at a frequency which is rejected by the digital filter.

9.5. Power Supply Rejection

Power supply rejection of the CS5371/72 modulators is frequency dependent. The digital filter rejects power supply noise for frequencies above the filter corner frequency at 130 dB or greater. For frequencies between DC and the digital filter corner frequency, power supply rejection is nearly constant at 90 dB.

10. PIN DESCRIPTION - CS5371

Rough Non-Inverting Input	INR+	1 •	24	PWDN	Power-down Enable
Fine Non-Inverting Input	INF+	2	23	LPWR	Low Power Mode Select
Fine Inverting Input	INF-	3	22	MFLAG	Modulator Flag Output
Rough Inverting Input	INR-	4	21	MDATA	Modulator Data Output
Positive Voltage Reference Input	VREF+	5	20	MSYNC	Modulator Sync Input
Negative Voltage Reference Input	VREF-	6	19	MCLK	Modulator Clock Input
Negative Analog Power Supply	VA-	7	18	VD	Positive Digital Power Supply
Positive Analog Power Supply	VA+	8	17	DGND	Digital Ground
No Internal Connection	NC	9	16	NC	No Internal Connection
No Internal Connection	NC	10	15	NC	No Internal Connection
No Internal Connection	NC	11	14	OFST	Offset Mode Select
No Internal Connection	NC	12	13	VD	Positive Digital Power Supply

Power Supplies

VA+ – Positive Analog Power Supply, pin 8

Positive supply voltage.

VA- – Negative Analog Power Supply, pin 7

Negative supply voltage.

VD – Positive Digital Power Supply, pin 13, 18

Positive supply voltage.

DGND – Digital Ground, pin 17

Analog Inputs

INR+ – Rough Non-Inverting Input, pin 1

Rough non-inverting analog input. The rough input settles non-linear currents to improve linearity on the fine input and reduce harmonic distortion.

INR- – Rough Inverting Input, pin 4

Rough inverting analog input. The rough input settles non-linear currents to improve linearity on the fine input and reduce harmonic distortion.

INF+ – Fine Non-Inverting Input, pin 2

Fine non-inverting analog input.

INF- – Fine Inverting Input, pin 3

Fine inverting analog input.

VREF+ – Positive Voltage Reference Input, pin 5

Input for an external +2.5 V voltage reference relative to VREF-.

VREF- – Negative Voltage Reference Input, pin 6

This pin should be tied to VA-.

Digital Inputs**MCLK – Modulator Clock Input, pin 19**

A CMOS compatible clock input for the modulator internal master clock, nominally 2.048 MHz with an amplitude equal to the VD digital power supply.

MSYNC – Modulator Sync Input, pin 20

A low to high transition resets the internal clock phasing of the modulator. This assures the sampling instant and modulator data output are synchronous to the external system.

OFST – Offset Mode Select, pin 14

When high, adds approximately -50 mV of offset to the analog inputs to guarantee any $\Delta\Sigma$ idle tones are removed. When low, no offset is added.

LPWR – Low Power Mode Select, pin 23

When set high with MCLK operating at 1.024 MHz, modulator power dissipation is reduced to 15 mW per channel.

PWDN – Power-down Mode, pin 24

When high, the modulator is in power-down mode and consumes 1 mW. Halting MCLK while in power down mode reduces modulator power dissipation to 10 μ W.

Digital Outputs**MDATA – Modulator Data Output, pin 21**

Modulator data is output as a 1-bit serial data stream at 512 kHz with an MCLK input of 2.048 MHz. Modulator data is output at 256 kHz with an MCLK input of 1.024 MHz.

MFLAG – Modulator Flag Output, pin 22

A high level output indicates the modulator is unstable due to an over-range on the analog inputs.

11. PIN DESCRIPTION - CS5372

Ch. 1 Rough Non-Inverting Input	INR1+	1 •	24	PWDN1	Ch. 1 Power-down Enable
Ch. 1 Fine Non-Inverting Input	INF1+	2	23	LPWR	Low Power Mode Select
Ch. 1 Fine Inverting Input	INF1-	3	22	MFLAG1	Ch. 1 Modulator Flag Output
Ch. 1 Rough Inverting Input	INR1-	4	21	MDATA1	Ch. 1 Modulator Data Output
Positive Voltage Reference Input	VREF+	5	20	MSYNC	Modulator Sync Input
Negative Voltage Reference Input	VREF-	6	19	MCLK	Modulator Clock Input
Negative Analog Power Supply	VA-	7	18	VD	Positive Digital Power Supply
Positive Analog Power Supply	VA+	8	17	DGND	Digital Ground
Ch. 2 Rough Inverting Input	INR2-	9	16	MDATA2	Ch. 2 Modulator Data Output
Ch. 2 Fine Inverting Input	INF2-	10	15	MFLAG2	Ch. 2 Modulator Flag Output
Ch. 2 Fine Non-Inverting Input	INF2+	11	14	OFST	Offset Mode Select
Ch. 2 Rough Non-Inverting Input	INR2+	12	13	PWDN2	Ch. 2 Power-down Enable

Power Supplies

VA+ – Positive Analog Power Supply, pin 8

Positive supply voltage.

VA- – Negative Analog Power Supply, pin 7

Negative supply voltage.

VD – Positive Digital Power Supply, pin 18

Positive supply voltage.

DGND – Digital Ground, pin 17

Analog Inputs

INR1+, INR2+ – Channel 1 & 2 Rough Non-Inverting Inputs, pin 1, 12

Rough non-inverting analog inputs. The rough inputs settle non-linear currents to improve linearity on the fine inputs and reduce harmonic distortion.

INR1-, INR2- – Channel 1 & 2 Rough Inverting Inputs, pin 4, 9

Rough inverting analog inputs. The rough inputs settle non-linear currents to improve linearity on the fine inputs and reduce harmonic distortion.

INF1+, INF2+ – Channel 1 & 2 Fine Non-Inverting Input, pin 2, 11

Fine non-inverting analog inputs.

INF1-, INF2- – Channel 1 & 2 Fine Inverting Input, pin 3, 10

Fine inverting analog inputs.

VREF+ – Positive Voltage Reference Input, pin 5

Input for an external +2.5 V voltage reference relative to VREF-.

VREF- – Negative Voltage Reference Input, pin 6

This pin should be tied to VA-.

Digital Inputs**MCLK – Modulator Clock Input, pin 19**

A CMOS compatible clock input for the modulator internal master clock, nominally 2.048 MHz with an amplitude equal to the VD digital power supply.

MSYNC – Modulator Sync Input, pin 20

A low to high transition resets the internal clock phasing of the modulator. This assures the sampling instant and modulator data output are synchronous to the external system.

OFST – Offset Mode Select, pin 14

When high, adds approximately -50 mV of offset to the analog inputs to guarantee any $\Delta\Sigma$ idle tones are removed. When low, no offset is added.

LPWR – Low Power Mode Select, pin 23

When set high with MCLK operating at 1.024 MHz, modulator power dissipation is reduced to 15 mW per channel.

PWDN1, PWDN2 – Channel 1 & 2 Power-down Mode, pin 24, 13

When high, the modulator is in power down mode and consumes 1 mW. Halting MCLK while in power down mode reduces modulator power dissipation to 10 μ W.

Digital Outputs**MDATA1, MDATA2 – Modulator Data Output, pin 21, 16**

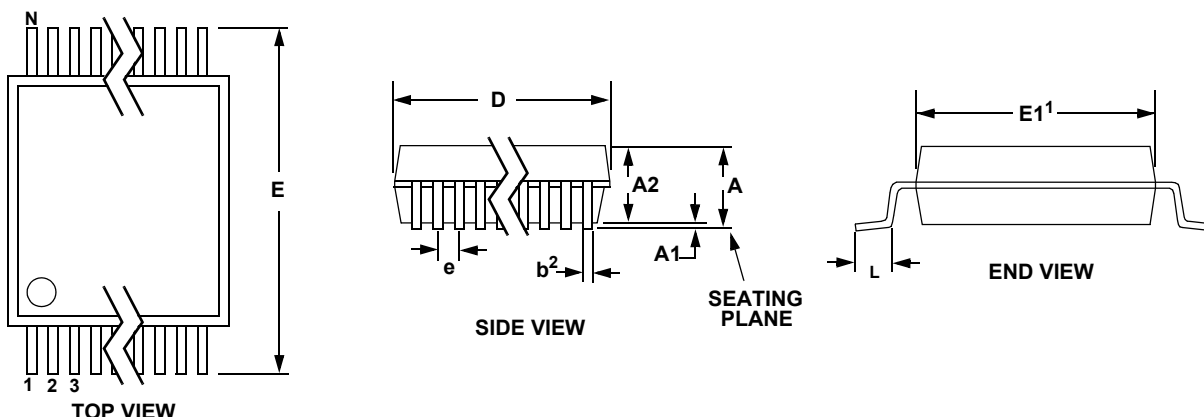
Modulator data is output as a 1-bit serial data stream at 512 kHz with an MCLK input of 2.048 MHz. Modulator data is output at 256 kHz with an MCLK input of 1.024 MHz.

MFLAG1, MFLAG2 – Modulator Flag, pin 22, 15

A high level output indicates the modulator is unstable due to an over-range on the analog inputs.

12. PACKAGE DIMENSIONS

24 PIN SSOP PACKAGE DRAWING



DIM	INCHES		MILLIMETERS		NOTE
	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	2,3
D	0.311	0.335	7.90	8.50	1
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	1
e	0.024	0.027	0.61	0.69	
L	0.025	0.040	0.63	1.03	
α	0°	8°	0°	8°	

- Notes:
1. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
 2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
 3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

13.ORDERING INFORMATION

Model	Temperature	Package
CS5371-BS	-40 to +85 °C	24-pin SSOP
CS5371-BSZ (lead free)		
CS5372-BS		
CS5372-BSZ (lead free)		

14.ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5371-BS	240 °C	2	365 Days
CS5371-BSZ (lead free)	260 °C	3	7 Days
CS5372-BS	240 °C	2	365 Days
CS5372-BSZ (lead free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

15. REVISION HISTORY

Revision	Date	Changes
PP2	AUG 2001	Preliminary release, updated with most-current characterization data.
F1	SEP 2005	Fix data sheet errata.
F2	SEP 2005	Corrected Table 1 on Page 13: When OFST=0 the 0V input is 0x000000, when OFST=1 the 0V input is 0xFE21D8.
F3	OCT 2005	Corrected typical and maximum low-power THD on Page 3. Corrected maximum input signal frequency on Page 4.

Contacting Cirrus Logic Support

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