8-bit AVR Microcontroller

ATtiny102/ATtiny104

DATASHEET SUMMARY

Introduction

The Atmel® ATtiny102/ATtiny104 is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny102/ATtiny104 achieves throughputs close to 1 MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

Feature

High Performance, Low Power Atmel® AVR® 8-Bit Microcontroller Family

- Advanced RISC Architecture
  - 54 Powerful Instructions
  - Mostly Single Clock Cycle Execution
  - 16 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 12 MIPS Throughput at 12MHz
- Non-volatile Program and Data Memories
  - 1024 Bytes of In-system Programmable Flash Program Memory
  - 32 Bytes Internal SRAM
  - Flash Write/Erase Cycles: 10,000
  - Data Retention: 20 Years at 85°C / 100 Years at 25°C
  - Self-programming Flash on Full Operating Voltage Range (1.8 – 5.5V)
- Peripheral Features
  - One 16-bit Timer/Counter (TC) with Prescaler, Input Capture, Two Output Capture and Two PWM Channels
  - Programmable Watchdog Timer (WDT) with Separate On-chip Oscillator
  - Selectable Internal Voltage References: 1.1V, 2.2V and 4.3V
  - 10-bit ADC with 8-channels/14-pin and 5-channel/8-pin Package Options
  - On-chip Analog Comparator (AC)
  - Serial Communication Module: USART

- Special Microcontroller Features
  - In-system Programmable
    - External Programming (2.7 – 5.5V)
    - Self Programming (1.8 – 5.5V)
  - External and Internal Interrupt Sources
  - Low Power Idle, ADC Noise Reduction, and Power-pown Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Supply Voltage Level Monitor with Interrupt and Reset
  - Accurate Internal Calibrated Oscillator
  - Fast and Normal Start-up Time Options Available
  - Individual Serial Number to Represent a Unique ID.
- I/O and Packages
  - 12 Programmable I/O Lines for ATtiny104 and 6 Programmable I/O Lines for ATtiny102
  - 8-pin UDFN (ATtiny102)
  - 8-pin SOIC150 (ATtiny102)
  - 14-pin SOIC150 (ATtiny104)
- Operating Voltage
  - 1.8 - 5.5V
- Temperature Range
  - -40 to +125°C
- Speed Grades
  - 0 – 4MHz at 1.8 – 5.5V
  - 0 – 8MHz at 2.7 – 5.5V
  - 0 – 12MHz at 4.5 – 5.5V

Table of Contents

1. Description

The Atmel®AVR® core combines a rich instruction set with 16 general purpose working registers. All the 16 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The device provides the following features: 1024 Bytes of In-System Programmable Flash with Read-While-Write capabilities, 32 Bytes SRAM, 6/12 general purpose I/O lines for ATtiny102/ATtiny104, 16 general purpose working registers, a 16-bit Timer/Counters (TC) with compare modes, internal and external interrupts, one serial programmable USART, a programmable Watchdog Timer with internal Oscillator and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, TC, USART, ADC, Analog Comparator (AC), and interrupt system to continue functioning. ADC Noise Reduction mode minimizes switching noise during ADC conversions by stopping the CPU and all I/O modules except the ADC. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The device is manufactured using Atmel's high density Non-Volatile Memory (NVM) technology. The on-chip, in-system programmable Flash allows program memory to be re-programmed in-system by a conventional, NVM programmer.

The device is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kit.

2. Configuration Summary

	ATtiny102	ATtiny104
Pin Count	8	14
Flash (Bytes)	1024	1024
SRAM (Bytes)	32	32
EEPROM (Bytes)	-	-
General Purpose I/O-pins (GPIOs)	6	12
USART	1	1
Analog-to-Digital Converter (ADC) / Channels	10-bit ADC with 5-channel	10-bit ADC with 8-channels
Analog Comparators (AC) Channels	1	1
AC Propagation Delay	75-750ns	75-750ns
16-bit Timer Counter (TC) Instances	1	1
PWM Channels	2	2
RC Oscillator	+/-2 %	+/-2 %
Internal Voltage Reference	1.1V/2.2V/4.3V	1.1V/2.2V/4.3V
Operating Voltage	1.8 - 5.5V	
Max Operating Frequency (MHz)	12	
Temperature Range	-40°C to +125°C	
Packages	8-pin UDFN 8-pin SOIC150	14-pin SOIC150

3. Ordering Information

Speed [MHz]	Power Supply [V]	Ordering Code	Package	Operational Range
12	1.8 -5.5	ATtiny102-M7R	8 pad UDFN	Industrial (-40°C to +105°C)
		ATtiny102F-M7R(1)	8 pad UDFN	
		ATtiny102-SSNR	8 pin SOIC150	
		ATtiny102F-SSNR(1)	8 pin SOIC150	
		ATtiny104-SSNR	14 pin SOIC150	
		ATtiny104F-SSNR(1)	14 pin SOIC150	
		ATtiny102-M8R	8 pad UDFN	Industrial (-40°C to +125°C)
		ATtiny102F-M8R(1)	8 pad UDFN	
		ATtiny102-SSFR	8 pin SOIC150	
		ATtiny102F-SSFR(1)	8 pin SOIC150	
		ATtiny104-SSFR	14 pin SOIC150	
		ATtiny104F-SSFR(1)	14 pin SOIC150	

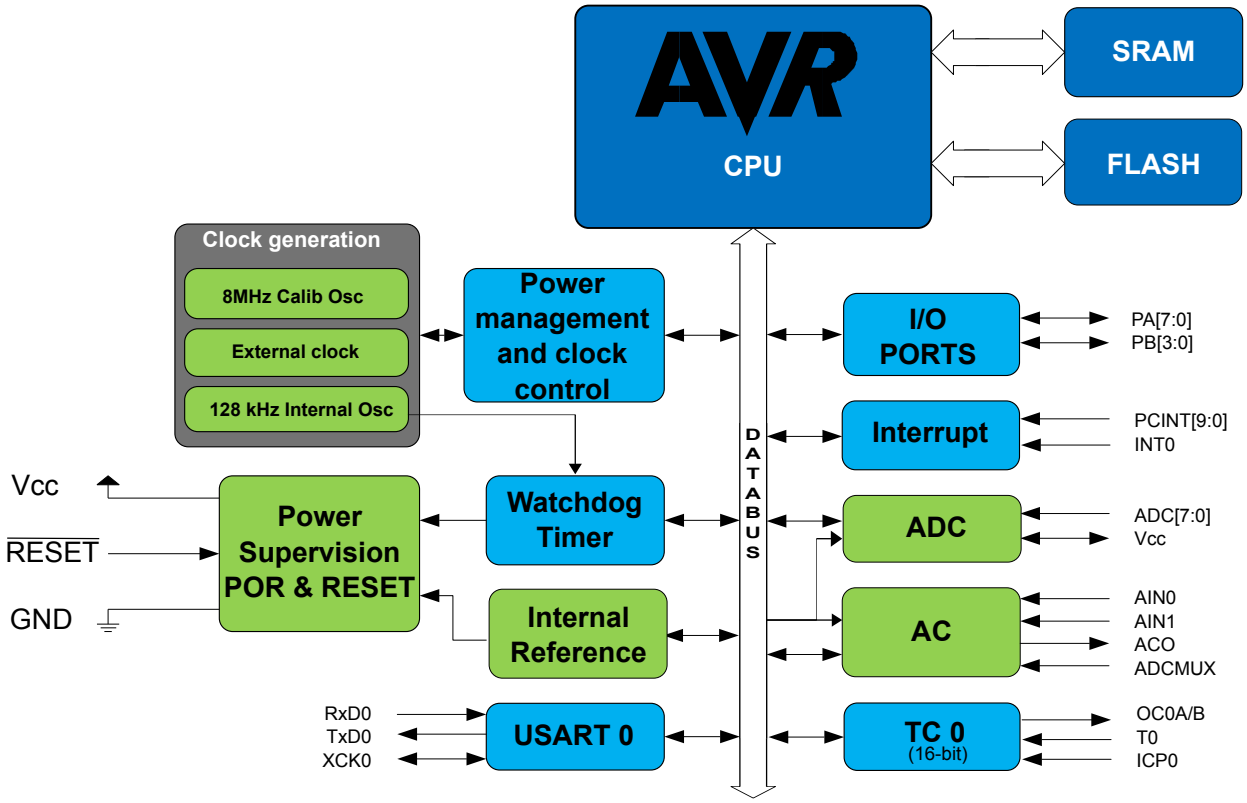
Note:

1. ATtiny104F-xxx and ATtiny102F-xxx have the fast start-up time option.

Package Type	
8 pad UDFN	8-pad, 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)
8 pin SOIC150	8-lead, 0.150” Wide Body, Plastic Gull Wing Small Outline (JEDEC SOIC)
14 pin SOIC150	14-lead, 1.27mm Pitch, 8.65 x 3.90 x 1.60mm Body Size, Plastic Small Outline Package (SOIC)

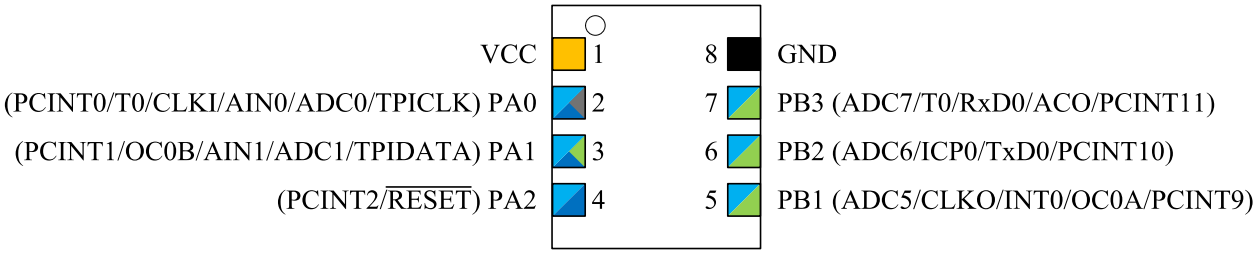
4. Block Diagram

Figure 4-1. Block Diagram



5. Pin Configurations

Figure 5-1. Pin-Out of 8-Pin UDFN



Caution: The thermal pad on the rear of the package should not be connected.

Figure 5-2. Pin-Out of 8-Pin SOIC150

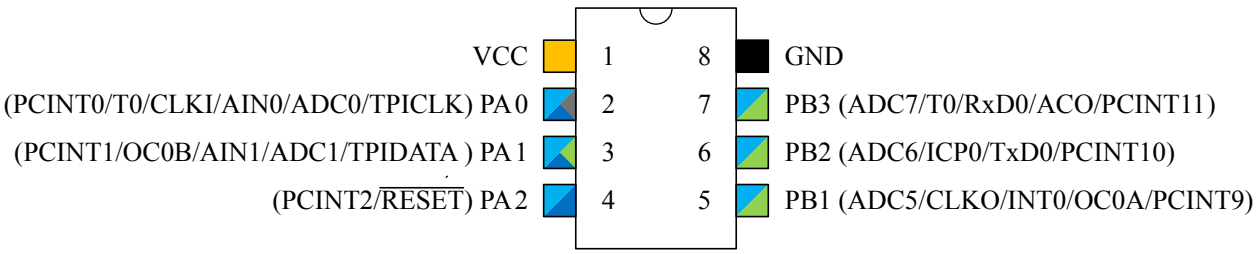
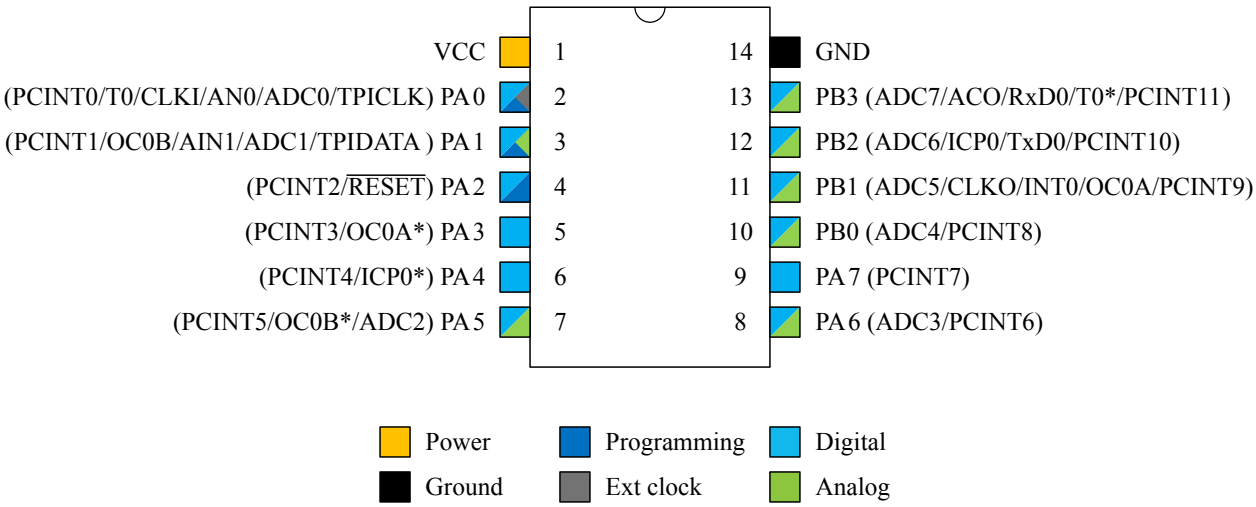


Figure 5-3. Pin-Out of 14-Pin SOIC150



5.1. Pin Descriptions

5.1.1. VCC

Digital supply voltage.

5.1.2. GND

Ground.

5.1.3. Port A (PA[7:0])

This is a 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

5.1.4. Port B (PB[3:0])

This is a 4-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

5.1.5. $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in *System and Reset Characteristics of Electrical Characteristics*. Shorter pulses are not guaranteed to generate a reset.

The reset pin can also be used as a (weak) I/O pin.

6. I/O Multiplexing

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions. The following table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 6-1. PORT Function Multiplexing

14-pin	8-pin	Pin name	Special	INT(3)	ADC(3)	AC	USART	Timer	Programming(8)
1	1(1)	V_{CC}							
2	2	PA[0](2)	CLKI	PCINT0	ADC0	AIN0		T0	TPICLK
3	3	PA[1](5)		PCINT1	ADC1	AIN1		OC0B	TPIDATA
4	4	PA[2]	RESET	PCINT2					RESET
5	-	PA[3](9)		PCINT3				OC0A	
6	-	PA[4](9)		PCINT4				ICP0	
7	-	PA[5](5)(9)		PCINT5	ADC2			OC0B	
8	-	PA[6]		PCINT6	ADC3				
9	-	PA[7]		PCINT7					
10	-	PB[0]		PCINT8	ADC4				
11	5	PB[1](6)	CLKO	PCINT9/INT0	ADC5		XCK0	OC0A	
12	6	PB[2](7)		PCINT10	ADC6		TxD0	ICP0	
13	7	PB[3](4)(9)		PCINT11	ADC7	ACO	RxD0	T0	
14	8	GND							

Note:

1. On the 8-pin UDFN package, the thermal pad should not be connected as well.
2. Priority of CLKI is higher than ADC0. When EXT_CLK is enabled, ADC channel will not work and DIDR0 will not disable the digital input buffer.
3. When both PCINT and the corresponding ADC channel are enabled, the digital input buffer will not be disabled.
4. When ACO is enabled, ADC, TC and USART RX inputs are not disabled.
5. When OC0B is enabled, ADC and AC will continue to receive inputs on that channel if enabled.
6. When CLKO is enable in PB[1], OCA will get lower priority.
7. When USART is enabled, the users must ensure that ADC channel corresponding to the TxD0 pin is not used. Because DIDR0 register will only control the input buffer, not the output part.
8. During reset/external programming, all pins are treated as inputs and outputs are disabled.
9. Alternative location when enabling T/C Remap

7. General Information

7.1. Resources

A comprehensive set of development tools, application notes, and datasheets are available for download on http://www.atmel.com/avr.

7.2. Data Retention

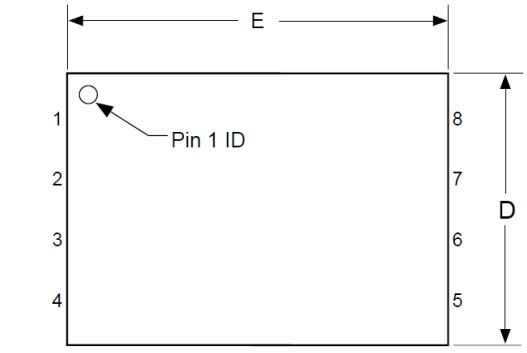
Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C.

7.3. About Code Examples

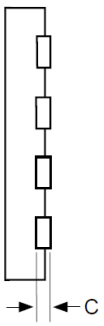
This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

8. Packaging Information

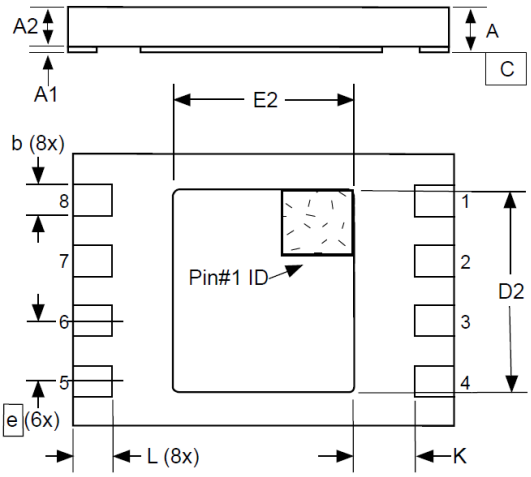
8.1. 8-pin UDFN



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Notes:
1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

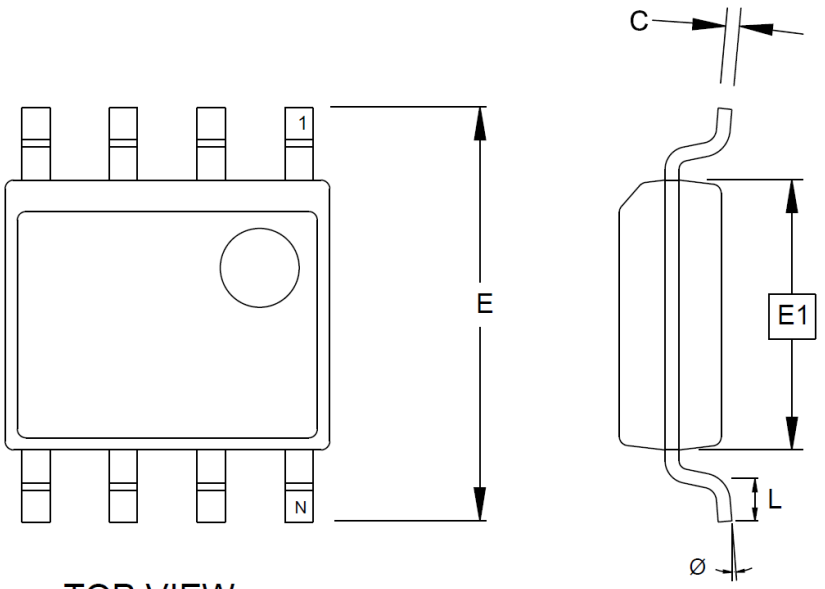
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.40	1.50	1.60	
E	2.90	3.00	3.10	
E2	1.20	1.30	1.40	
b	0.18	0.25	0.30	3
C	0.152 REF			
L	0.35	0.40	0.45	
e	0.50 BSC			
K	0.20	-	-	

11/2/15

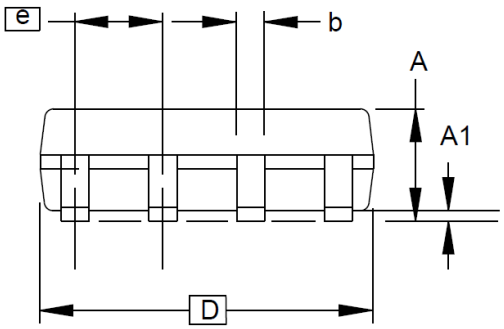
Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)	GPC YNZ	DRAWING NO. 8MA2	REV. H

8.2. 8-pin SOIC150



TOP VIEW

END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

COMMON DIMENSIONS
(Unit of Measure = mm)

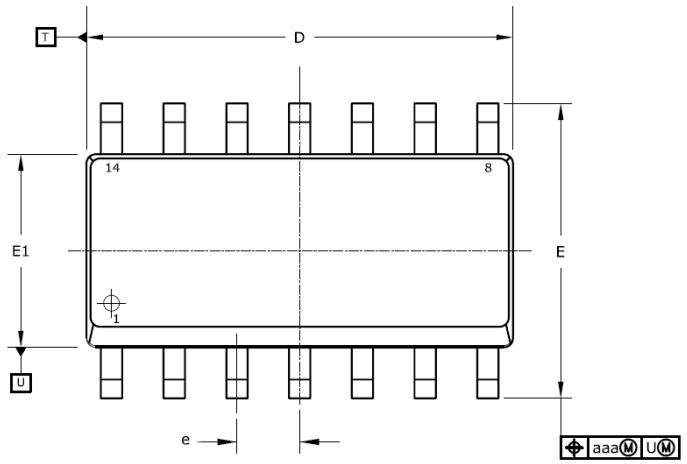
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

6/22/11

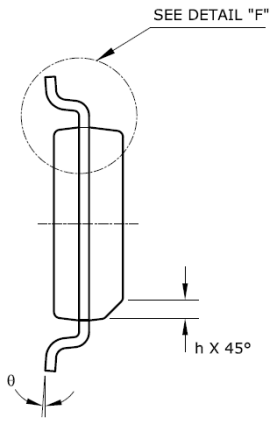
Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

8.3. 14-pin SOIC150

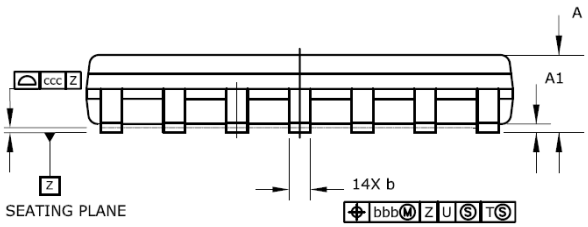
DRAWINGS NOT SCALED



TOP VIEW

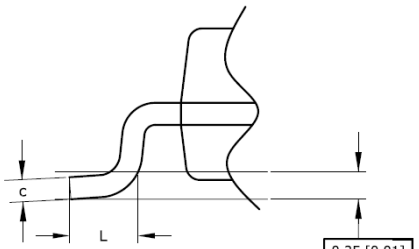


END VIEW



SEATING PLANE

SIDE VIEW



GAUGE PLANE

DETAIL 'F'

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	1.60	1.75	
A1	0.10	----	0.25	
D	8.55	8.65	8.75	2
E	5.80	6.00	6.20	
E1	3.80	3.90	4.00	3
L	0.40	----	1.27	
b	0.33	----	0.51	4
c	0.19	-----	0.25	
e	1.27 BSC			
h	0.25	-----	0.50	
θ	0°	-----	8°	
TOLERANCES OF FORM AND POSITION				
aaa	0.25			
bbb	0.25			
ccc	0.10			
n	14			

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-012, Variation AB.
2. Dimensions D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shal not exceed 0.15mm (0.006 in) per side.
3. Dimensions E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010 in) per side.
4. Dimensions b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.10mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

01/31/2014

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	TU, 14 Lds - 1.27mm Pitch, 8.65X3.90x1.60mm Body Size Plastic Small Outline Package (SOIC)	SVQ	TU	D

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**