Edge4717D
Quad Channel, Per Pin Precision Measurement Unit

SEMTECH

TEST AND MEASUREMENT PRODUCTS

Description

The Edge4717D is a precision measurement unit designed for automated test equipment and instrumentation. Manufactured in a wide voltage CMOS process, it is a monolithic solution for a quad channel per pin PMU.

Each channel of the Edge4717D features a PMU that can force or measure voltage over a typical 15V I/O range, and supports 4 current ranges: ± 3.2 µA, ± 80 µA, ± 2 mA, ± 30 mA.

The Edge4717D has an on-board window comparator per channel that provides two bits of information — DUT too high and DUT too low. There is also a monitor pin which provides a real time analog signal proportional to either the voltage or current measured at the DUT.

The Edge4717D is designed to be a low power, low cost, small footprint solution to allow high pin count testers to support a PMU per pin.

On-board voltage clamps, with over-current detection, provide protection to the DUT and 4717D.

The Edge4717D also has a sample-and-hold feature available for capturing DUT current or voltage measurements.

The Edge4717D is a design improvement to the Edge4717 that features:

- Increased FV/MV range
- Improved over-current detection circuit functionality
- LVTTL comparator outputs (pull-up resistors no longer required)
- Improved HiZ switching characteristics
- Improved Force Voltage Linearity

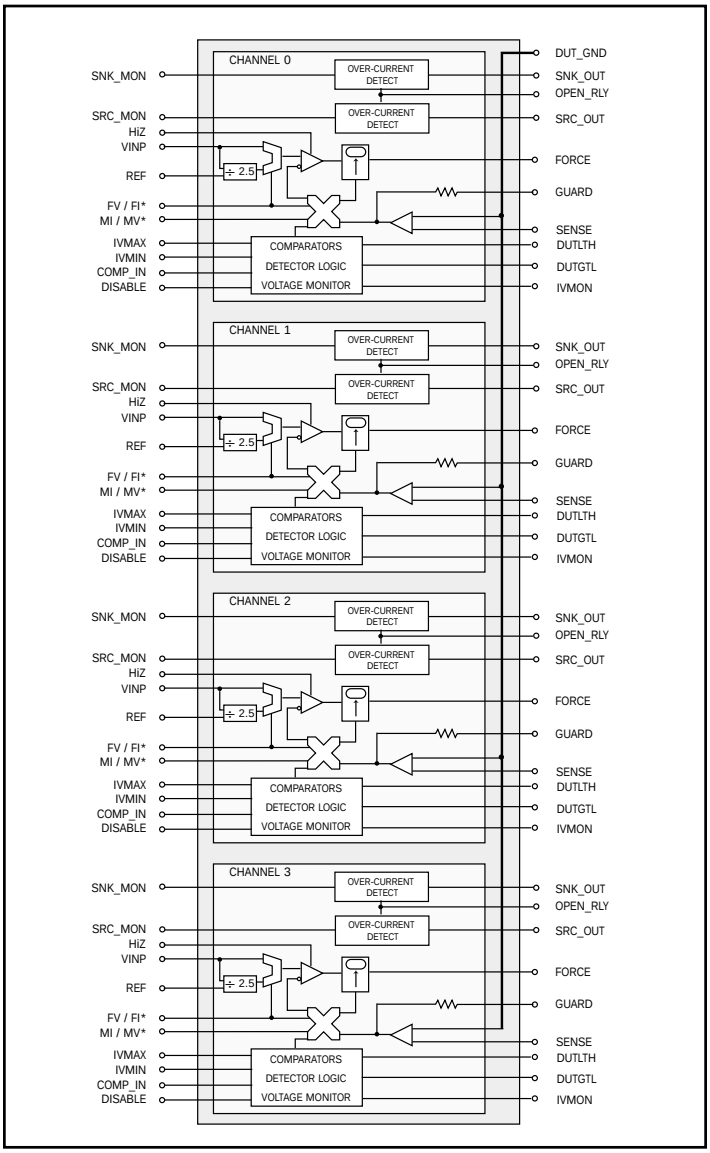
Applications

- Automated Test Equipment
  - Memory Testers
  - VLSI Testers
  - Mixed Signal Tester

Features

- FV / MI Capability
- FI / MV Capability
- FV / MV Capability
- FI / MI Capability
- 4 Current Ranges (± 3.2 µA, ± 80 µA, ± 2 mA, ± 30 mA)
- –5.5V to 9.5V Nominal Output Range (Zero Current)
- –3.5 to 7.5V Nominal Output Range (Full Scale Current)
- On-board Voltage Clamps
- Internal Sample and Hold
- 228 Pin 23 mm x 23 mm TBGA Package

Functional Block Diagram



PIN Description

Pin Name	Pin #	Description
VINP[0:3]	B19, H22, N21, V22	Analog voltage input which forces the output voltage (FV mode) and the output current (FI mode) (one per channel).
REF[0:3]	A19, G22, M21, U22	Reference pin for divide by 2.5 circuit for force current mode; this reference is typically set to 2.25V.
FORCE[0:3]	E2, J2, N2, U2	Analog output pin which forces current or voltage.
SENSE[0:3]	E3, J3, N3, U3	Analog input pin which senses voltage.
FV_FI*[0:3]	A7, C11, A14, B17	TTL compatible input which determines whether the PMU is forcing current or forcing voltage.
MI_MV*[0:3]	C9, B11, B14, C16	TTL compatible input which determines whether the PMU is measuring current or measuring voltage.
RS0[0:3]	C7, B9, C12, B15	TTL compatible current range select inputs.
RS1[0:3]	C6, A8, B12, A15	TTL compatible current range select inputs.
IVMIN[0:3]	C17, H20, M20, U21	Analog input voltages which establish the lower threshold level for the measurement comparator.
IVMAX[0:3]	C18, H21, N22, U20	Analog input voltages which establish the upper threshold level for the measurement comparator.
COMP_IN[0:3]	D2, H2, M2, T2	Analog voltage input to measurement comparator.
DUT_LTH[0:3]	AA13, Y12, AA10, Y9	Digital comparator output that indicates the DUT measurement is less than the upper threshold.
DUT_GTL[0:3]	AA14, AA12, Y11, AA9	Digital comparator output that indicates the DUT measurement is greater than the lower threshold.
DISABLE[0:3]	A6, B10, B13, B16	TTL compatible input which places IVMON output in high impedance.
HIZ[0:3]	B7, A10, C13, A17	TTL compatible input that places the FORCE output into high impedance.
RA[0:3]	F3, K3, P3, V3	External resistor input corresponding to Range A.
RB[0:3]	F2, K2, P2, V2	External resistor input corresponding to Range B.
RC[0:3]	F1, K1, P1, V1	External resistor input corresponding to Range C.
RD[0:3]	G3, L3, R3, W3	External resistor input corresponding to Range D.
SNK_MON[0:3]	F21, K22, R22, AA17	Analog voltage input to sink current clamp.
SRC_MON[0:3]	F22, L22, T22, Y16	Analog voltage input to source current clamp.
SNK_OUT[0:3]	C1, G1, L1, R1	Clamp output.
SRC_OUT[0:3]	E1, J1, N1, U1	Clamp output.

PIN Description *(continued)*

Pin Name	Pin #	Description
OPEN_RLY[0:3]	Y14, Y13, AA11, Y10	Open drain output that is used for opening relays between tester and DUT in case of an over-current condition.
IVMON[0:3]	B18, G21, M22, T21	Analog voltage output that provides a real time monitor of either the measured voltage or measured current level.
LTCH_MODE[0:3]	B6, C10, A12, A16	Controls a mux for determination of whether IVMONITOR is from sample-and-hold or not sampled.
SAMPLE[0:3]	C8, A9, A13, C15	Used for sampling the voltage on the SENSE[0:3] voltage monitor pins.
GUARD[0:3]	D1, H1, M1, T1	Driven guard pin used for guard traces.
TEST[0:3]	B8, A11, C14, A18	Digital input control pin for mux for testing sample-and-hold.
TEST_IN[0:3]	C19, J22, N20, V21	Analog input for testing the sample-and-hold.
COMP1[0:3] COMP2[0:3]	D20, J20, P21, V20 D21, J21, P20, Y19	Internal compensation pins that require an external capacitor connection between the two pins.
COMP3[0:3]	E21, K21, R21, Y18	Internal compensation pin that requires an external capacitor connection between the pin and ground.
COMP4[0:3]	F20, K20, R20, Y17	Internal compensation pin that requires an external capacitor connection between the pin and FORCE output.
DUT_GND	Y6	Input reference pin that should be connected to DUT ground line.
Power Pins		
VCC	A1, A2, A21, A22, B1, B2, B21, B22, C3, C20, Y3, Y20, AA1, AA2, AA21, AA22, AB1, AB2, AB21, AB22	Positive analog power supply.
VDD	Y15	Positive digital supply (comparator).
VEE	A20, B20, C21, C22, D22, E22, G2, L2, R2, W2, W21, W22, Y21, Y22, AA15, AA18, AA19, AA20, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20	Negative analog power supply.
GND	A3, A4, A5, B3, B4, B5, C2, C4, C5, W1, Y1, Y2, Y4, Y5, Y7, Y8, AA3, AA4, AA5, AA6, AA7, AA8, AB3, AB4, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AB12	Ground.
NC	D3, E20, H3, G20, L20, L21, M3, P22, T3, T20, W20, AA16	No Connection. (Unused pins; leave unconnected).

PIN Description *(continued)*

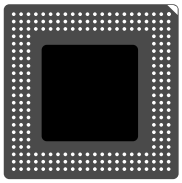
A1 Ball Pad Indicator

Top View

23mm x 23mm 228 Pin TBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	A1 VCC	A2 VCC	A3 GND	A4 GND	A5 GND	A6 DISABLE0	A7 FV_FIN0	A8 RS11	A9 SAMPLE1	A10 HIZ1	A11 TEST1	A12 LTCH_MODE2	A13 SAMPLE2	A14 FV_FIN2	A15 RS13	A16 LTCH_MODE3	A17 HIZ3	A18 TEST3	A19 IREF0	A20 VEE	A21 VCC	A22 VCC
B	B1 VCC	B2 VCC	B3 GND	B4 GND	B5 GND	B6 LTCH_MODE0	B7 HIZ0	B8 TEST0	B9 RS01	B10 DISABLE1	B11 MI_MVN1	B12 RS12	B13 DISABLE2	B14 MI_MVN2	B15 RS03	B16 DISABLE3	B17 FV_FIN3	B18 IVMON0	B19 VINP0	B20 VEE	B21 VCC	B22 VCC
C	C1 SNK_OUT0	C2 GND	C3 VCC	C4 GND	C5 GND	C6 RS10	C7 RS00	C8 SAMPLE0	C9 MI_MVN0	C10 LTCH_MODE1	C11 FV_FIN1	C12 RS02	C13 HIZ2	C14 TEST2	C15 SAMPLE3	C16 MI_MVN3	C17 IV_MIN0	C18 IV_MAX0	C19 TEST_IN0	C20 VCC	C21 VEE	C22 VEE
D	D1 GUARD0	D2 COMP_IN0	D3 NC	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20 COMP10	D21 COMP20	D22 VEE
E	E1 SRC_OUT0	E2 FORCE0	E3 SENSE0	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	E16	E17	E18	E19	E20 NC	E21 COMP30	E22 VEE
F	F1 RC0	F2 RB0	F3 RA0	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20 COMP4D	F21 SNK_MON0	F22 SRC_MON0
G	G1 SNK_OUT1	G2 VEE	G3 RD0	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16	G17	G18	G19	G20 HLD_CAP0 (NC)	G21 IVMON1	G22 IREF1
H	H1 GUARD1	H2 COMP_IN1	H3 NC	H4	H5	H6	H7	H8	H9	H10	H11	H12	H13	H14	H15	H16	H17	H18	H19	H20 IV_MIN1	H21 IV_MAX1	H22 VINP1
J	J1 SRC_OUT1	J2 FORCE1	J3 SENSE1	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20 COMP11	J21 COMP21	J22 TEST_IN1
K	K1 RC1	K2 RB1	K3 RA1	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20 COMP41	K21 COMP31	K22 SNK_MON1
L	L1 SNK_OUT2	L2 VEE	L3 RD1	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16	L17	L18	L19	L20 NC	L21 HLD_CAP1 (NC)	L22 SRC_MON1
M	M1 GUARD2	M2 COMP_IN2	M3 NC	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	M16	M17	M18	M19	M20 IV_MIN2	M21 IREF2	M22 IVMON2
N	N1 SRC_OUT2	N2 FORCE2	N3 SENSE2	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20 TEST_IN2	N21 VINP2	N22 IV_MAX2
P	P1 RC2	P2 RB2	P3 RA2	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	P18	P19	P20 COMP22	P21 COMP12	P22 NC
R	R1 SNK_OUT3	R2 VEE	R3 RD2	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20 COMP42	R21 COMP32	R22 SNK_MON2
T	T1 GUARD3	T2 COMP_IN3	T3 NC	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17	T18	T19	T20 HLD_CAP2 (NC)	T21 IVMON3	T22 SRC_MON2
U	U1 SRC_OUT3	U2 FORCE3	U3 SENSE3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20 IV_MAX3	U21 IV_MIN3	U22 IREF3
V	V1 RC3	V2 RB3	V3 RA3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14	V15	V16	V17	V18	V19	V20 COMP13	V21 TEST_IN3	V22 VINP3
W	W1 GND	W2 VEE	W3 RD3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15	W16	W17	W18	W19	W20 NC	W21 VEE	W22 VEE
Y	Y1 GND	Y2 GND	Y3 VCC	Y4 GND	Y5 GND	Y6 DUT_GND	Y7 GND	Y8 GND	Y9 DUT_LTH3	Y10 OPEN_RLY3	Y11 DUT_GTL2	Y12 DUT_LTH1	Y13 OPEN_RLY1	Y14 OPEN_RLY0	Y15 VDD	Y16 SRC_MON3	Y17 COMP43	Y18 COMP33	Y19 COMP23	Y20 VCC	Y21 VEE	Y22 VEE
AA	AA1 VCC	AA2 VCC	AA3 GND	AA4 GND	AA5 GND	AA6 GND	AA7 GND	AA8 GND	AA9 DUT_GTL3	AA10 DUT_LTH2	AA11 OPEN_RLY2	AA12 DUT_GTL1	AA13 DUT_LTH0	AA14 DUT_GTL0	AA15 VEE	AA16 HLD_CAP3 (NC)	AA17 SNK_MON3	AA18 VEE	AA19 VEE	AA20 VEE	AA21 VCC	AA22 VCC
AB	AB1 VCC	AB2 VCC	AB3 GND	AB4 GND	AB5 GND	AB6 GND	AB7 GND	AB8 GND	AB9 GND	AB10 GND	AB11 GND	AB12 GND	AB13 VEE	AB14 VEE	AB15 VEE	AB16 VEE	AB17 VEE	AB18 VEE	AB19 VEE	AB20 VEE	AB21 VCC	AB22 VCC

PIN Description *(continued)*



A1 Ball Pad Indicator
(see gold triangle located at the corner)

Bottom View

23mm x 23mm 228 Pin TBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	A22 VCC	A21 VCC	A20 VEE	A19 IREF0	A18 TEST3	A17 HIZ3	A16 LTCH_MODE3	A15 RS13	A14 FV_FIN2	A13 SAMPLE2	A12 LTCH_MODE2	A11 TEST1	A10 HIZ1	A9 SAMPLE1	A8 RS11	A7 FV_FIN0	A6 DISABLE0	A5 GND	A4 GND	A3 GND	A2 VCC	A1 VCC	A
B	B22 VCC	B21 VCC	B20 VEE	B19 VINP0	B18 IVMONITOR0	B17 FV_FIN3	B16 DISABLE3	B15 RS03	B14 MI_MVN2	B13 DISABLE2	B12 RS12	B11 MI_MVN1	B10 DISABLE1	B9 RS01	B8 TEST0	B7 HIZ0	B6 LTCH_MODE0	B5 GND	B4 GND	B3 GND	B2 VCC	B1 VCC	B
C	C22 VEE	C21 VEE	C20 VCC	C19 TEST_IN0	C18 IV_MAX0	C17 IV_MIN0	C16 MI_MVN3	C15 SAMPLE3	C14 TEST2	C13 HIZ2	C12 RS02	C11 FV_FIN1	C10 LTCH_MODE1	C9 MI_MVN0	C8 SAMPLE0	C7 RS00	C6 RS10	C5 GND	C4 GND	C3 VCC	C2 GND	C1 SNK_OUT0	C
D	D22 VEE	D21 COMP20	D20 COMP10	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3 NC	D2 COMP_IN0	D1 GUARD0	D
E	E22 VEE	E21 COMP30	E20 NC	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3 SENSE0	E2 FORCE0	E1 SRC_OUT0	E
F	F22 SRC_MON0	F21 SNK_MON0	F20 COMP40	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3 RA0	F2 RB0	F1 RC0	F
G	G22 IREF1	G21 IVMON1	G20 HLD_CAP0 (NC)	G19	G18	G17	G16	G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3 RD0	G2 VEE	G1 SNK_OUT1	G
H	H22 VINP1	H21 IV_MAX1	H20 IV_MIN1	H19	H18	H17	H16	H15	H14	H13	H12	H11	H10	H9	H8	H7	H6	H5	H4	H3 NC	H2 COMP_IN1	H1 GUARD1	H
J	J22 TEST_IN1	J21 COMP21	J20 COMP11	J19	J18	J17	J16	J15	J14	J13	J12	J11	J10	J9	J8	J7	J6	J5	J4	J3 SENSE1	J2 FORCE1	J1 SRC_OUT1	J
K	K22 SNK_MON1	K21 COMP31	K20 COMP41	K19	K18	K17	K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3 RA1	K2 RB1	K1 RC1	K
L	L22 SRC_MON1	L21 HLD_CAP1 (NC)	L20 NC	L19	L18	L17	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3 RD1	L2 VEE	L1 SNK_OUT2	L
M	M22 IVMON2	M21 IREF2	M20 IV_MIN2	M19	M18	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3 NC	M2 COMP_IN2	M1 GUARD2	M
N	N22 IV_MAX2	N21 VINP2	N20 TEST_IN2	N19	N18	N17	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3 SENSE2	N2 FORCE2	N1 SRC_OUT2	N
P	P22 NC	P21 COMP12	P20 COMP22	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3 RA2	P2 RB2	P1 RC2	P
R	R22 SNK_MON2	R21 COMP32	R20 COMP42	R19	R18	R17	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3 RD2	R2 VEE	R1 SNK_OUT3	R
T	T22 SRC_MON2	T21 IVMON3	T20 HLD_CAP2 (NC)	T19	T18	T17	T16	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3 NC	T2 COMP_IN3	T1 GUARD3	T
U	U22 IREF3	U21 IV_MIN3	U20 IV_MAX3	U19	U18	U17	U16	U15	U14	U13	U12	U11	U10	U9	U8	U7	U6	U5	U4	U3 SENSE3	U2 FORCE3	U1 SRC_OUT3	U
V	V22 VINP3	V21 TEST_IN3	V20 COMP13	V19	V18	V17	V16	V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3 RA3	V2 RB3	V1 RC3	V
W	W22 VEE	W21 VEE	W20 NC	W19	W18	W17	W16	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3 RD3	W2 VEE	W1 GND	W
Y	Y22 VEE	Y21 VEE	Y20 VCC	Y19 COMP23	Y18 COMP33	Y17 COMP43	Y16 SRC_MON3	Y15 VDD	Y14 OPEN_RLY0	Y13 OPEN_RLY1	Y12 DUT_LTH1	Y11 DUT_GTL2	Y10 OPEN_RLY3	Y9 DUT_LTH3	Y8 GND	Y7 GND	Y6 DUT_GND	Y5 GND	Y4 GND	Y3 VCC	Y2 GND	Y1 GND	Y
AA	AA22 VCC	AA21 VCC	AA20 VEE	AA19 VEE	AA18 VEE	AA17 SNK_MON3	AA16 HLD_CAP3 (NC)	AA15 VEE	AA14 DUT_GTL0	AA13 DUT_LTH0	AA12 DUT_GTL1	AA11 OPEN_RLY2	AA10 DUT_LTH2	AA9 DUT_GTL3	AA8 GND	AA7 GND	AA6 GND	AA5 GND	AA4 GND	AA3 GND	AA2 VCC	AA1 VCC	AA
AB	AB22 VCC	AB21 VCC	AB20 VEE	AB19 VEE	AB18 VEE	AB17 VEE	AB16 VEE	AB15 VEE	AB14 VEE	AB13 VEE	AB12 GND	AB11 GND	AB10 GND	AB9 GND	AB8 GND	AB7 GND	AB6 GND	AB5 GND	AB4 GND	AB3 GND	AB2 VCC	AB1 VCC	AB

Circuit Description

Circuit Overview

The Edge4717D is a quad channel parametric test and measurement unit that can :

- Force Voltage / Measure Current
- Force Current / Measure Voltage
- Force Voltage / Measure Voltage
- Force Current / Measure Current
- Measure Voltage / Force Disable

The Edge4717D features a PMU (per channel) that can force or measure voltage over a 15V range and force or measure current over four distinct ranges:

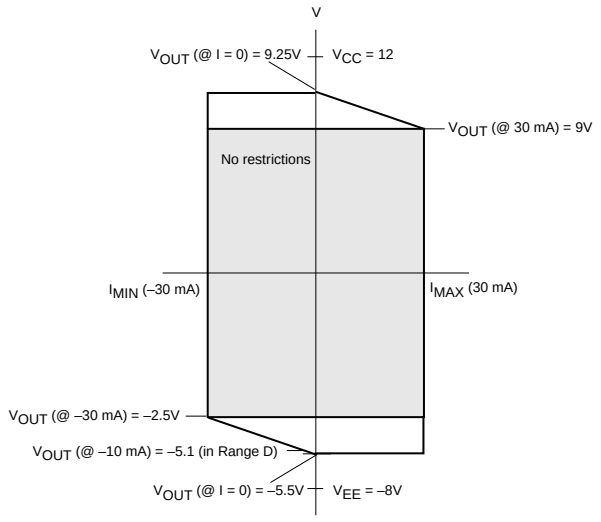
- ± 3.2 µA
- ± 80 µA
- ± 2 mA
- ± 30 mA

The Edge4717D features an on-board window comparator (per channel) that provides two bit measurement range classification.

Also, a monitor pin, IVMON, is capable of outputting either a real time analog voltage signal which tracks the measured parameter, or a sampled value of the measurement parameter captured using the sample and hold circuitry.

PMU Functionality

The trapezoid in Figure 1 describes the current-voltage functionality of the PMU with VCC = 12V and VEE = –8V, in Range D.



NOTE: Negative current is defined as current flowing into PMU from DUT.

Figure 1. PMU Functionality

Control Inputs

FV / FI* is a TTL compatible input which determines whether the PMU forces current or voltage, and MI/MV* is a TTL compatible input which determines whether the PMU measures current or voltage. FV/FI* and MI/MV* are independent for each channel of the Edge4717D. HIZ is a TTL compatible input which can be used to place the PMU's force amp into a high impedance state. Tables 1 and 2 describe the modes of operation related to these three input pins.

HIZ	FV / FI*	MI/MV*	Mode of Operation
1	X	X	High Impedance
0	0	0	Force Current, Measure Voltage
0	0	1	Force Current, Measure Current
0	1	0	Force Voltage, Measure Voltage
0	1	1	Force Voltage, Measure Current

Table 1.

RS0 and RS1 are TTL compatible inputs to an internal analog MUX which selects an external resistor corresponding to a desired current range. The truth table for RS0 and RS1, along with the associated external resistor values and current ranges, is shown in Table 2. RS0 and RS1 are independent for each channel of the Edge4717D.

RS1	RS0	Range	Current Range	"Nominal" Ext. R
0	0	A	3.2 µA	RA = 625KΩ
0	1	B	80 µA	RB = 25KΩ
1	0	C	2 mA	RC = 1KΩ
1	1	D	30 mA	RD = 40Ω

Table 2.

Circuit Description *(continued)*

FORCE/SENSE

FORCE is an analog output which either forces a current or forces a voltage, depending on which operating mode is selected. In FV mode, the voltage forced is equivalent to the voltage applied to the VINP pin. In FI mode, the current forced is mapped to the input as described in the Force Current section. FORCE can be placed in a high-impedance state through the setting of the HIZ input pin.

When the HIZ input pin is set to logical "0", the Edge4717D FORCE output will be controlled by the internal driver amplifier, and the Edge4717D will force a user-defined current or voltage (depending upon the setting of FV/FI*) at the FORCE pin. When HIZ is set to logical "1", the FORCE output is placed into a low-leakage, high impedance state.

SENSE is a high impedance analog input which measures the DUT voltage in the MV operating mode.

(FORCE and SENSE are brought out to separate pins to allow remote sensing.)

IVMON

IVMON is a real time analog voltage output which tracks the sensed parameter.

In the MV mode (MI/MV* = 0), the output voltage displayed at IVMON is a 1:1 mapping of the SENSE voltage. In the MI mode (MI/MV* = 1), IVMON follows the equation:

$$IVMON = I(measured) * REXT$$

Using nominal values for the external resistors (RA, RB, and RC), a voltage at IVMON of +2V corresponds to Imax, and –2V corresponds to Imin of the selected current range. For Range D, +1.2V corresponds to Imax and –1.2V corresponds to Imin.

The IVMON pin can also be placed into a high impedance state by using the DISABLE input (see Table 3).

Disable	MI / MV*	Sensed Parameter
1	X	High Impedance
0	0	Measured Voltage
0	1	Measured Current

Table 3.

Sample and Hold

The Edge4717D features a sample and hold circuit (per channel) which can be used to capture the corresponding voltage value of the sensed parameter (MI or MV) to be displayed at IVMON.

The output of the sample and hold is internally connected to IVMON through a latch controlled by LTCH_MODE. The setting of LTCH_MODE determines whether the data at IVMON comes from the sample and hold circuit or directly from the sensed parameter (see Table 4).

LTCH_MODE	Sample	Sample-and_Hold State
0	X	Transparent
1	↓ (Falling Edge)	Sample Data
1	0	Hold Data
1	1	Transparent

Table 4.

Note: No update is performed on the sample-and-hold.

Sample and Hold Testing

An analog MUX in the 4717D allows for testing of the sample-and-hold circuit.

The MUX control pin, TEST, is a TTL compatible input whose operation is described in Table 5. To test the sample and hold circuitry, an analog signal can be applied to the TEST_IN pin and sampled.

Circuit Description *(continued)*

TEST	Function
0	Normal Operation
1	TEST_IN used for sample-and-hold testing

Table 5.

Test Head Ground Reference

The Edge4717D features a test head ground referencing feature which allows the force voltage function to be referenced to a separate ground reference other than the ground (GND) power used for the device. The test head ground should be connected to the DUT_GND pin of the Edge4717D. The maximum allowed variation between DUT_GND and GND is ± 250 mV.

Force Voltage Mode

In the FV mode (FV/FI* = 1), VINP is a high impedance, analog voltage input that maps directly to the voltage forced at the FORCE pin.

Measure Current Mode

In the MI mode (MI/MV* = 1), a current monitor is connected in series with the PMU forcing amplifier. This monitor generates a voltage that is proportional to the current passing through it, and is brought out to IVMON. This voltage (corresponding to the measured current) can also be tested by the on-board window comparator.

Force Current Mode

In the FI mode (FV/FI* = 0), VINP is a high impedance, analog voltage input that is converted into a current at the FORCE pin (see Figure 1) using the following relationship:

$$\text{Forced Current} = \frac{\text{VINP} - \text{VREF}}{(\text{REXT} * 2.5)}$$

where VREF is the reference voltage input at the REF pin which is nominally set at 2.25V. (Positive current is defined as current flowing out of the PMU.) Table 6 describes the relationship between the voltage applied to VINP and the current at FORCE for Ranges A, B, and C.

VINP	Corresponding Forced Current
VREF + 5.5V	≥ Imax (Full-Scale, Ranges A, B, C)
VREF + 3.5V	≥ Imax (Full-Scale, Range D)
VREF	0
VREF – 3.5V	≤ Imin (Full-Scale, Range D)
VREF – 5.5V	≤ Imin (Full-Scale, Ranges A, B, C)

Table 6.

In the Force Current mode, the voltage at VINP is divided by 2.5 internally on the chip, so that a ± 2V range is used internally for forcing currents on Ranges A, B, and C. Range D uses a ± 1.2V range across REXT for forcing currents.

Measure Voltage Mode

In the MV mode (MI/MV* = 0), DUT voltage is measured via the SENSE input pin. This measured voltage can be displayed on the IVMON pin and tested using the internal window comparator.

Comparator

The Edge4717D features an on-board window comparator which provides two-bit measurement range classification. IVMAX and IVMIN are high impedance analog inputs that establish the upper and lower thresholds for the window comparator. COMP_IN is the window comparator input pin. COMP_IN should be connected to IVMON on each channel if it is desired to use the comparator to indicate PMU measurements.

In the MI mode, an I/V MAX input of +2V will set the upper threshold of the window comparator to a voltage corresponding to +FSC (full-scale current), and an I/V MIN input of –2V will set the lower threshold to a voltage corresponding to –FSC for Ranges A, B, and C. Similarly for Range D, –1.2V corresponds to sinking full-scale current, and +1.2V corresponds to sourcing full-scale current (positive current is defined as current flowing out of the PMU).

DUTGTL the DUTLTH are LVTTL compatible outputs which indicate the range of the measured parameter in relation to IVMIN and IVMAX. Comparator functionality is summarized in Table 7.

Circuit Description *(continued)*

TEST CONDITION	DUT LTH	DUT GTL
COMP_IN > IVMAX COMP_IN < IVMAX	0 1	N/A
COMP_IN > IVMIN COMP_IN < IVMIN	N/A	1 0
COMP_IN < IVMAX and COMP_IN > IVMIN	1	1

Table 7. Comparator Truth Table

Clamp Condition	Clamp Diode Current	OPEN_RLY
SRC_OUT < FORCE–V_{diode}	N/A	1
SRC_OUT > FORCE–V_{diode}	I_{CLAMP} > 55 mA I_{CLAMP} < 55 mA	0 1
SNK_OUT < FORCE+V_{diode}	I_{CLAMP} > 55 mA I_{CLAMP} < 55 mA	0 1
SNK_OUT > FORCE+V_{diode}	N/A	1

Table 8. Over-Current Detection Circuit Functionality (V_{diode} is the forward voltage of the external clamp diode).

REXT Selection

The Edge4717D is designed such that the maximum voltage drop across REXT (RA, RB, RC, or RD depending on range selected using RS0 and RS1 inputs) is ≤ 2V.

Resistor values can be chosen to operate the PMU at any current range up to ± 50 mA in accordance with the following equation:

$$REXT[\Omega] = \frac{2\ [V]}{IMAX[A]}$$

, IMAX ≤ 50 mA for Range D
IMAX ≤ 2 mA for Range C
IMAX ≤ 80 µA for Range B
IMAX ≤ 3.2 mA for Range A

Voltage Clamps/Over-Current Detection

The Edge4717D features four pairs of on-board clamps (one pair per channel), which can be used to clamp the voltage of pins connected to SRC_OUT and SNK_OUT between limits set by the voltages applied to SRC_MON and SNK_MON. SNK_MON is a high impedance input that establishes the upper clamping limit, while SRC_MON is a high impedance analog input that establishes the lower clamping limit. In addition to voltage clamping functionality, the clamp circuitry of the Edge4717D also features over-current detection capability. Over-current detection is only enabled when one of the voltage clamping thresholds is exceeded (FORCE + V_{diode} > SNK_MON or FORCE – V_{diode} < SRC_MON). When enabled, an over-current condition is signaled via the OPEN-RLY pin. OPEN_RLY is an open drain output pin that pulls down when an over-current condition is detected. OPEN_RLY functionality is depicted in Table 8.

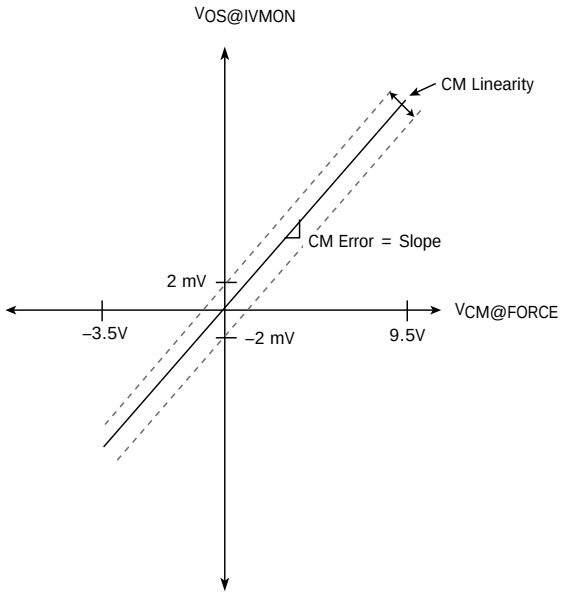
For applications that require the use of external resistors that are much smaller in Ohmic value than those that are outlined in Table 2, one will need to account for the variation in switch resistance vs. common mode voltage of the range selection switches (A-D in Figure 3) when specifying the overall accuracy of the application.

Common Mode Error/Calibration

In order to attain a high degree of accuracy in a typical ATE application, offset and gain errors are accounted for through software calibration. When operating the Edge4717D in the Measure Current (MI) or Force Current (FI) modes, an additional source of error, common mode error, should be accounted for. Common mode error is a measure of how the common mode voltage, V_{CM}, at the input of the current sense amplifier affects the forced or measured current values (see Figure 2). Since this error is created by internal resistors in the current sense amplifier, it is very linear in nature.

Using the common mode error and common mode linearity specifications, one can see that with a small number of calibration steps (see Applications note PMU-A1), the effect of this error can be significantly reduced.

Circuit Description *(continued)*



(Note: Slope may be negative)

Figure 2. Graphical Representation of Common Mode Error

Transient Clamps

The Edge4717D has on-board transient clamps to limit the voltage and current spikes that might result from either changing the current range or changing the operating mode.

Driven Guard Pin

The Edge4717D features a pin (per channel), GUARD, which can be used to drive the guard traces of a FORCE/SENSE pair. By surrounding FORCE and SENSE traces with guard traces which connect to the GUARD pin, an effective method to achieve minimal leakage can be achieved.

Power Supply Sequencing

In order to avoid the possibility of latch-up, the following power-up requirements must be satisified:

1. VEE ≤ GND ≤ VDD ≤ VCC at all times
2. VEE ≤ All inputs ≤ VCC

The following power supply sequencing can be used as a guideline when operating the Edge4717D:

Power Up Sequence

1. VCC (substrate)
2. VEE/VDD
3. Digital Inputs
4. Analog Inputs

Power Down Sequence

1. Analog Inputs
2. Digital Inputs
3. VEE/VDD
4. VCC (substrate)

Circuit Description *(continued)*

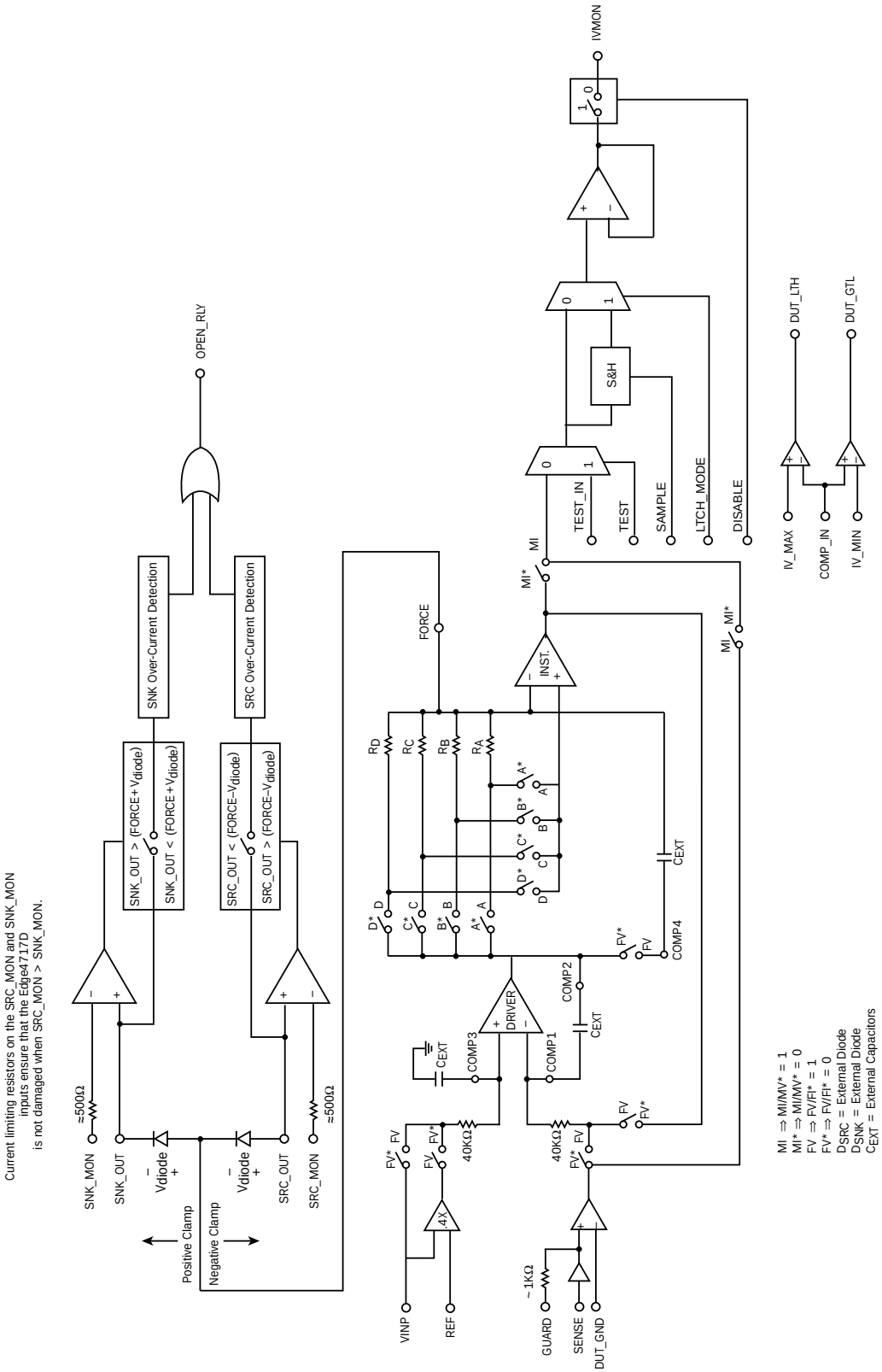
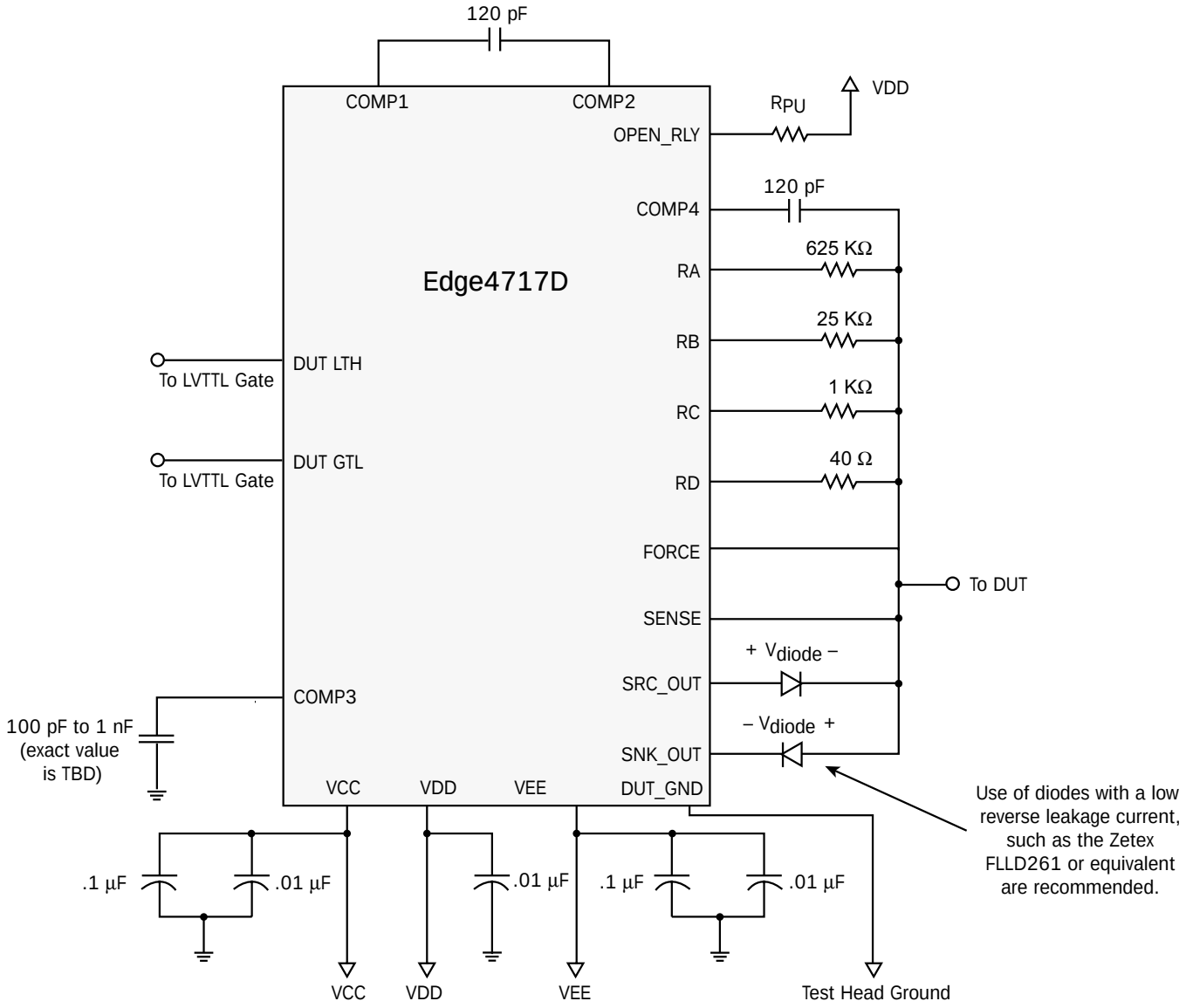


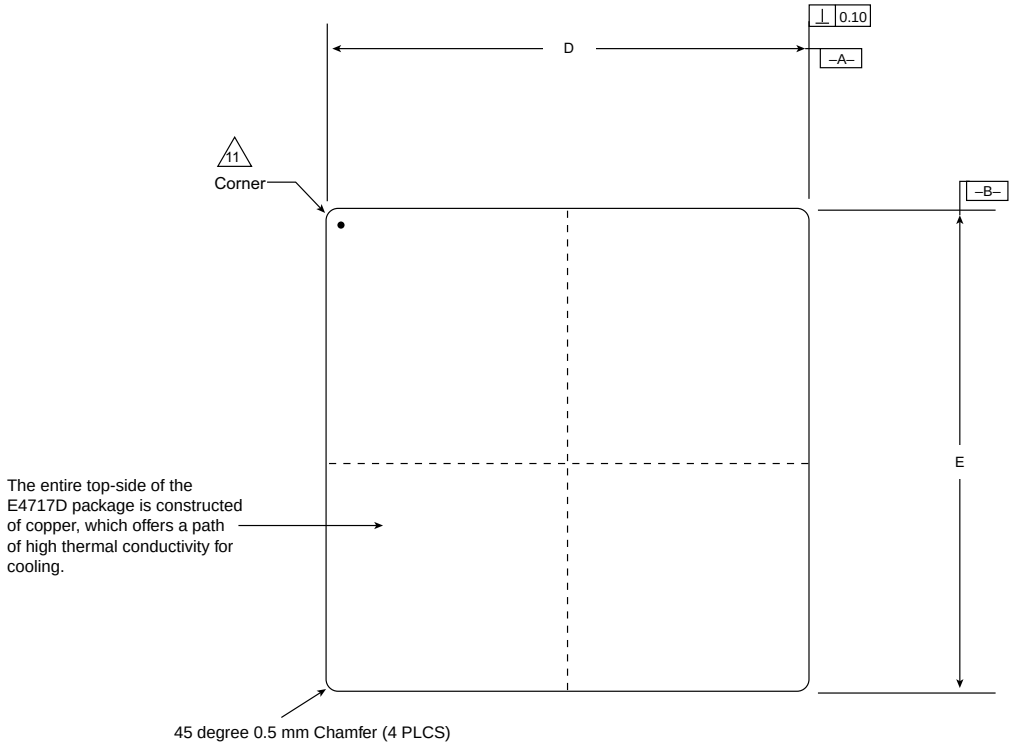
Figure 3. Functional Schematic



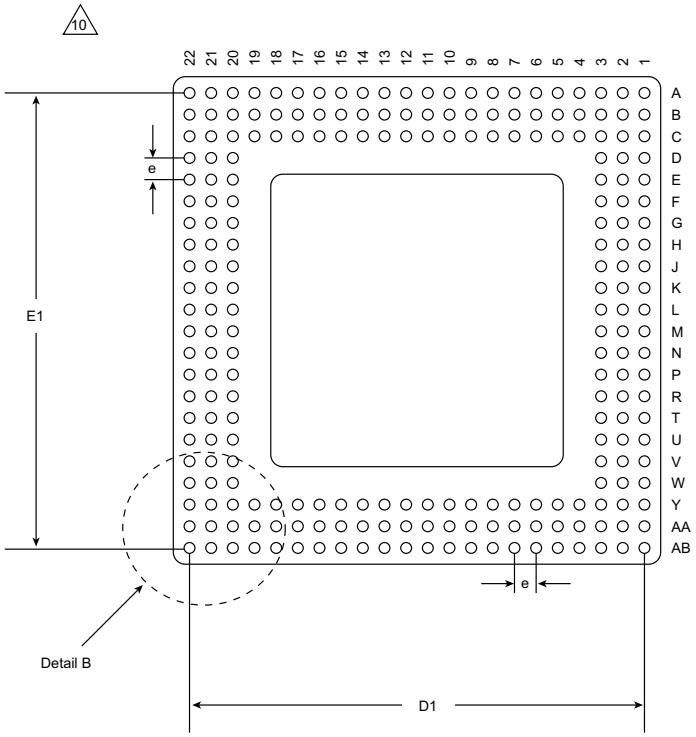
Actual decoupling capacitor values depend on the actual system environment.

Figure 4. Required External Components (Per Channel)

Package Information

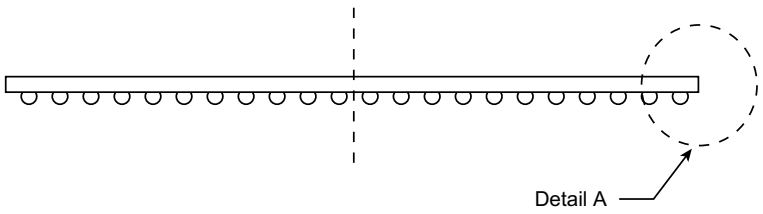


Top View

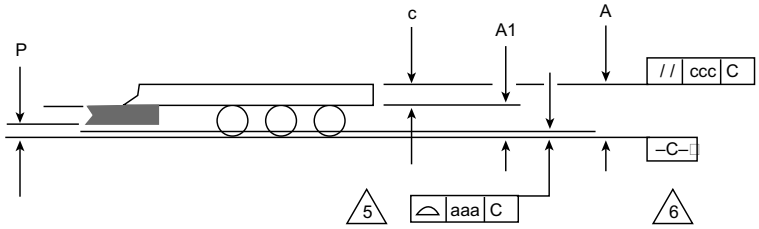


Bottom View

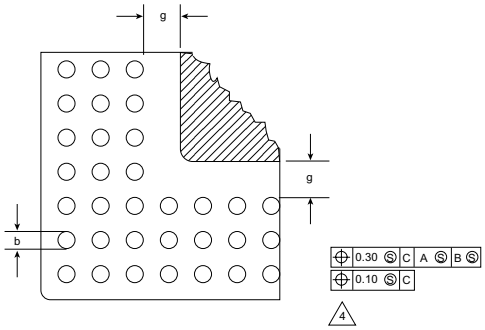
Package Information *(continued)*



Side View



Detail A



Detail B

NOTES:

1. All dimensions are in millimeters.
2. “e” represents the basic solder ball grid pitch.
3. “M” represents the basic solder ball matrix size, and symbol “N” is the maximum allowable number of balls after depopulating.
4. “b” is measured at the maximum solder ball diameter (after reflow) parallel to primary datum –C–.
5. Dimension “aaa” is measured parallel to primary datum –C–.
6. Primary datum –C– and seating plane are defined by the spherical crowns of the solder balls.
7. Package surface shall be black oxide.
8. Cavity depth varies with die thickness.
9. Substrate material base is copper.
10. Bilateral tolerance zone is applied to each side of package body.
11. 45 degree 0.5 mm Chamfer corner and white dot for Pin 1 identification.

Dimensional References			
REF.	**MIN.**	**NOM.**	**MAX.**
A	1.25	1.4	1.55
A1	0.40	0.50	0.60
D	22.80	23.00	23.20
D1		21.00 BSC	
E	22.80	23.00	23.20
E1		21.00 BSC	
b	0.525	0.65	0.775
c	0.85	0.90	0.95
M		22	
N		228	
aaa			0.15
ccc			0.25
e		1.00 TYP	
g	0.35		
P	0.15		

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Power Supply	VCC	11.5	12	12.5	V
Negative Analog Power Supply	VEE	–8.5	–8	–7.5	V
Total Analog Power Supply	VCC – VEE	19	20	21	V
Digital Power Supply	VDD	3.0	3.3	5.25	V
Case Temperature	TC	25		+65	˚C
Thermal Resistance of Package (Junction to Case)	θjc		0.3		˚C/W

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC			+15	V
Negative Power Supply	VEE	–15			V
Total Power Supply	VCC – VEE	0		22	V
Digital Power Supply	VDD	0		+7	V
Digital Inputs		–.5		7.0	V
Analog Inputs		VEE – .5		VCC + .5	V
Storage Temperature		–55		+125	˚C
Case Temperature				100	˚C
Soldering Temperature				260	˚C

Stresses above listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Power Supply Consumption (No-Load)					
Positive Supply	ICC		35	72	mA
Negative Supply	IEE		35	72	mA
"Digital" Supply	IDD			5	mA
Power Supply Rejection Ratio	PSRR				
VCC to any Analog Output (except in Hold mode)					
1 MHz			20		dB
500 kHz			20		dB
100 kHz			25		dB
VEE to any Analog Output (except in Hold mode)					
1 MHz			16		dB
500 kHz			18		dB
100 kHz			25		dB
VDD to any Analog Output (except in Hold mode)					
< 1 MHz			60		dB
VCC to IVMON (Hold Mode)					
1 MHz			0.6		dB
500 kHz			6		dB
100 kHz			20		dB
200 Hz			30		dB
VEE to IVMON (Hold Mode)					
1 MHz			1.7		dB
500 kHz			7		dB
100 kHz			21		dB
200 Hz			30		dB
VDD to IVMON (Hold Mode)					
< 1 MHz			60		dB
Force Voltage Mode					
Input Voltage Range	VINP	VEE + 2.0		VCC – 2.0	V
Input Leakage Current	Ileak	–1	0	1	µA
Output Forcing Voltage (Positive Full-Scale Current through R_{EXT})	VFORCE	VEE + 2.5		VCC – 4.5	V
Output Forcing Voltage (0 Current through R_{EXT})	VFORCE	VEE + 2.5		VCC – 2.5	V
Output Forcing Voltage (Negative Full-Scale Current through R_{EXT})	VFORCE	VEE + 4.5		VCC – 2.5	V
Voltage Accuracy					
Offset	VOS	–200		200	mV
Gain	Gain	.985		1.015	V/V
Linearity	FV INL	–0.025	.01	+0.025	% FSVR

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Measure Current Mode					
Current Measurement Range	$I_{MEASURE}$				
Range A		–3.2		3.2	µA
Range B		–80		80	µA
Range C		–2		2	mA
Range D		–30		30	mA
Current Measurement Accuracy					
Offset (@ IVMON)	VOS	–150		150	mV
Gain (Note 1)	Gain	.985		1.015	V/V
Linearity	MI INL				
Ranges A, B, C		–.08		.08	% FSCR
Range D		–80		+80	µA
Common Mode Error	CM Error	–5.5		5.5	mV/V
Common Mode Linearity					
FORCE = VEE + 4.5V to VCC – 4.75V	CM INL	–.05		.05	%FSCR
IVMON Output Impedance	R_{OUT}		500		Ω
IVMON Leakage Current	I_{LEAK}	–100		100	nA
(IVMON = VEE+2.5V TO VCC–2.5V)					
Force Current Mode					
Input Voltage Range	VINP	VREF – 5.5		VREF + 5.5	V
Input Leakage Current	I_{LEAK}	–1		1	µA
REF Input Voltage Range	VREF	0		2.5	V
REF Leakage Current	I_{LEAK}	–1	0	–1	µA
Output Forcing Current	I_{FORCE}				
Range A		–3.2		3.2	µA
Range B		–80		80	µA
Range C		–2		2	mA
Range D		–30		30	mA
Compliance Voltage Range	VFORCE				
Positive Full-Scale Current		VEE + 2.5		VCC – 3.0	V
0 Current		VEE + 2.5		VCC – 2.5	V
Negative Full-Scale Current		VEE + 3.0		VCC – 2.5	V
Current Accuracy					
Offset	IOS	–3.6		3.6	% FSCR
Gain (Note 2)	Gain	.385	.4	.415	V/V
Linearity	FI INL				
Ranges A, B, C		–.08		.08	% FSCR
Range D		–80		+80	µA
Common Mode Error	CM Error	–5.5		5.5	mV/V
Common Mode Linearity					
FORCE = VEE + 4.5V to VCC – 4.5V	CM INL	–.05		.05	% FSCR

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Measure Voltage Mode					
Voltage Measurement Range	VSENSE	VEE + 2.5		VCC – 2.5	V
Voltage Measurement Accuracy					
Offset	VOS	–200		200	mV
Gain	Gain	.985	±.01	1.015	V/V
Linearity	MV INL	–.025		.025	%FSVR
FORCE/SENSE Combined Leakage Current in HiZ (FV/FI* = 0, FORCE/SENSE = VEE + 2.5V to VCC–2.5V)	I_{LEAK}	–10		10	nA
IVMON Output Impedance	R_{OUT}		500		Ω
IVMON Leakage Current (IVMON = VEE + 2.5V to VCC–2.5V)	I_{LEAK}	–100		100	nA
Digital Inputs (FV/FI*, MI/MV*, RS0, RS1, DISABLE, TEST, HiZ, LTCH_MODE, SAMPLE)					
Input Low Level	VIL			0.8	V
Input High Level	VIH	2.0			V
Input Leakage Current	Ileak	–1	0	1	µA
Voltage Clamps					
Range	SNK_MON – SRC_MON	.5		16.0	V
Effective Output Impedance of Clamps	R_{OUT}			10	Ω
Sink Clamp Voltage Range	SNK_MON	VEE + 2.5		VCC – 2.0	V
Source Clamp Voltage Range	SRC_MON	VEE + 2.0		VCC – 2.5	V
SRC_MON Leakage Current	I_{LEAK}	–1		1	µA
SNK_MON Leakage Current	I_{LEAK}	–1		1	µA
Linearity @ 5 mA Constant Current	CLAMP INL	–.400		+.400	% FSVR
Offset @ 5 mA Constant Current	VOS	–150		+150	mV
PPMU Voltage Clamps Current Interrupt Limit (OPEN_RLY Trigger Current)	I_{CLAMP}	35		95	mA
PPMU Voltage Clamps Current Limiting Range	I_{LIMIT}	35		95	mA
Output Low Voltage for OPEN_RLY Pin @ 1 mA	V_{OL}			500	mV
TEST_IN Leakage Current	I_{LEAK}	–1		1	µA
OPEN_RLY Leakage Current @ 5V	I_{LEAK}	–1		1	µA
Sample and Hold Circuit					
Linearity Error	S&H INL	–.025	.01	.025	% FSVR
Hold Step	V_{HS}		16	20	mV
TempCo of Hold Step (Note 3)	ΔV / Δ°C			50	µV/°C
Output Impedance of IVMON (Note 3)	R_{OUT}		500		Ω

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Short Circuit Protection					
Forcing Op-Amp Current Limit (Note 3)	I_{MAX}	35		75	mA
Driven Guard / Test Head Ground					
GUARD – SENSE @ DUT_GND = 0 SENSE = 5V	V_{DIFF}	–100		+100	mV
DUT_GND to GND Voltage Range	V_{OS}	–250		+250	mV
DUT_GND Leakage Current	I_{LEAK}	–1		1	µA
Comparator					
IVMAX Voltage Range	IVMAX	VEE + 1.75		VCC – 1.75	V
IVMIN Voltage Range	IVMIN	VEE + 1.75		VCC – 1.75	V
Comparator Offset (IVMIN, IVMAX)	V_{OS}	–100		+100	mV
Input Bias Current at (IVMIN, IVMAX, COMP_IN)	I_{bias}	–1		+1	µA
Digital Outputs (DUTLTH, DUTGTL)					
Output Low Level (TBD load)	V_{OL}			400	mV
Output High Level (TBD load)	V_{OH}	2.4		VDD	V

Note 1: Gain = $\frac{IVMON}{V_{EXT}}$, where V_{EXT} is the voltage across R_{EXT}, which corresponds to measured current.

Note 2: Gain = $\frac{V_{EXT}}{VINP - REF}$, REF = 2.25V nominal, V_{EXT} is the voltage across R_{EXT}, which corresponds to forced current.

Note 3: Guaranteed by design and characterization. Not production tested.

Unit Definitions:

FSCR = Full Scale Current Range
- Range A, ± 3.2 µA
- Range B, ± 80 µA
- Range C, ± 2 mA
- Range D, ± 30 mA

FSVR = Full Scale Voltage Range
- FV mode, no current = 14V minimum
- FV mode, current load = 12V minimum
- MV mode = 14V minimum

AC Characteristics

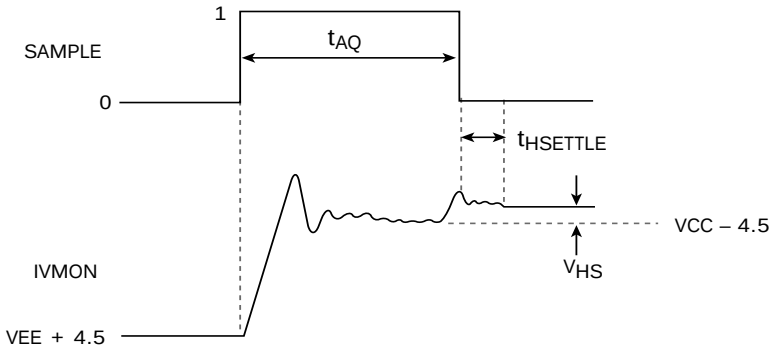
Parameter	Symbol	Min	Typ	Max	Units
Force Voltage / Measure Current					
FORCE Output Voltage Settling Time (Note 1) (To 0.1% of 10V step)	t_{settle}				
RANGE A				2	ms
RANGES B, C, D				300	µs
Measured Current Settling Time (Note 1) (To 0.1% of FSCR step)	t_{settle}				
RANGE A				4	ms
RANGES B, C, D				300	µs
Stability (Note 1)					
Capacitive Loading Range for Stable Operation	C_{LOAD}	0		10	nF
Force Amp					
Saturation Recovery Time	t_{sr}		25		µs
HiZ True to FORCE Disable Time	t_z			1	µs
HiZ False to FORCE Enable Time	t_{oe}			15	µs
Force Current / Measure Voltage					
FORCE Output Current Settling Time (Note 1) (To 0.1% of FSCR step)	t_{settle}				
RANGE A				4	ms
RANGES B, C, D				300	µs
SENSE (Measure) Voltage Settling Time (Note 1) (To 0.1% of 10V step)	t_{settle}				
RANGE A				4	ms
RANGES B, C, D				300	µs
Stability (Note 1)					
Capacitive Loading Range for Stable Operation	C_{LOAD}	0		10	nF
Force Amp					
Saturation Recovery Time	t_{sr}		25		µs
HiZ True to FORCE Disable Time	t_z			1	µs
HiZ False to FORCE Enable Time	t_{oe}			15	µs
I/V Monitor					
Enable Time	t_{oe}			500	ns
Disable Time	t_z			500	ns

AC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Sample and Hold Circuit					
Droop Rate	ΔV/Δt			40	mV/s
Acquisition Time (to 0.025% of Sampled Value)	t_{AQ}		1	10	µs
Hold Mode Settling Time (Notes 1, 2)					
Measure Voltage Mode	$t_{HSETTLE}$				
To 0.1% of 10V Step			0.8	1.5	µs
To 0.025% of 10V Step			1.4	2	µs
Measure Current Mode (Notes 1, 2)	$t_{HSETTLE}$				
To 0.1% of 4V Step			1.3	2	µs
To 0.025% of 4V Step			1.8	3	µsf
Comparators					
Propagation Delay	tpd			25	µs

AC Test Conditions: COMP3 = 120 pF to Ground; COMP4 = 120 pF to FORCE; Capacitor between COMP1 and
COMP2 = 120 pF; Load at FORCE/SENSE combined output = 100 pF.

Note 1: Guaranteed by design and characterization. Not production tested.
Note 2: Sample and Hold Circuit Acquisition Time (t_{AQ}) and Settling Time ($t_{HSETTLE}$) are described below:



CONDITIONS:

LTCH_MODE = 1
IVMON = 100 pF to GND

Ordering Information

Model Number	Package
E4717DBG	228 Pin 23 mm x 23 mm TBGA
EVM4717DBG	Edge4717D Evaluation Board

This device is ESD sensitive. Care should be taken when handling and installing this device to avoid damaging it.

Contact Information

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