

FQD17N08L / FQU17N08L

80V LOGIC N-Channel MOSFET

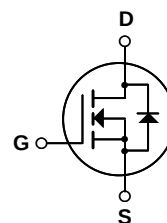
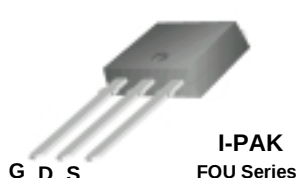
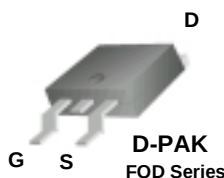
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand a high energy pulse in the avalanche and commutation modes. These devices are well suited for low voltage applications such as automotive, high efficiency switching for DC/DC converters, and DC motor control.

Features

- 12.9A, 80V, $R_{DS(on)} = 0.1\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 8.8 nC)
- Low C_{rss} (typical 29 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Low level gate drive requirements allowing direct operation from logic drives



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQD17N08L / FQU17N08L	Units
V_{DSS}	Drain-Source Voltage	80	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	12.9	A
	- Continuous ($T_C = 100^\circ\text{C}$)	8.2	A
I_{DM}	Drain Current - Pulsed (Note 1)	51.6	A
V_{GSS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	100	mJ
I_{AR}	Avalanche Current (Note 1)	12.9	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	40	W
	- Derate above 25°C	0.32	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	3.13	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.08	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 64\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 6.45\text{ A}$	--	0.076	0.100	Ω
		$V_{GS} = 5\text{ V}, I_D = 6.45\text{ A}$	--	0.090	0.115	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 25\text{ V}, I_D = 6.45\text{ A}$ (Note 4)	--	11.7	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	400	520	pF
C_{oss}	Output Capacitance		--	120	155	pF
C_{rss}	Reverse Transfer Capacitance		--	29	37	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}, I_D = 16.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	7	25	ns
t_r	Turn-On Rise Time		--	290	590	ns
$t_{d(off)}$	Turn-Off Delay Time		--	20	50	ns
t_f	Turn-Off Fall Time		--	75	160	ns
Q_g	Total Gate Charge	$V_{DS} = 64\text{ V}, I_D = 16.5\text{ A},$ $V_{GS} = 5\text{ V}$ (Note 4, 5)	--	8.8	11.5	nC
Q_{gs}	Gate-Source Charge		--	2.0	--	nC
Q_{gd}	Gate-Drain Charge		--	5.4	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	12.9	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	51.6	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 12.9 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 16.5 A, dI _F / dt = 100 A/μs (Note 4)	--	55	--	ns
Q _{rr}	Reverse Recovery Charge		--	85	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 0.83\text{ mH}, I_{AS} = 12.9\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 16.5\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

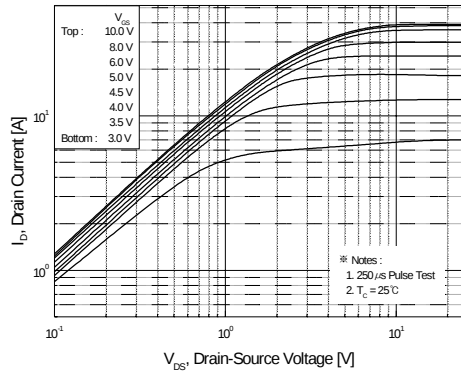


Figure 1. On-Region Characteristics

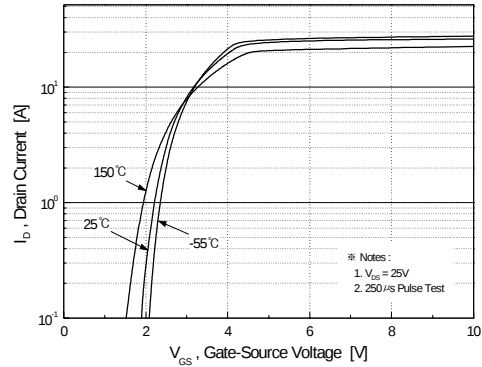


Figure 2. Transfer Characteristics

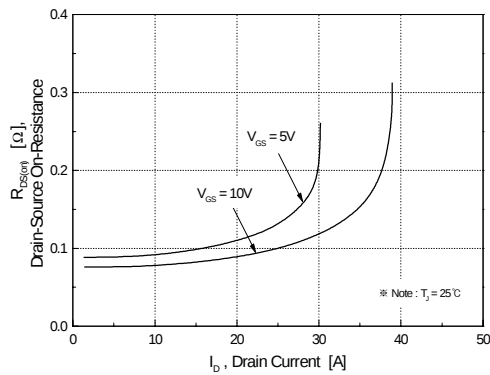


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

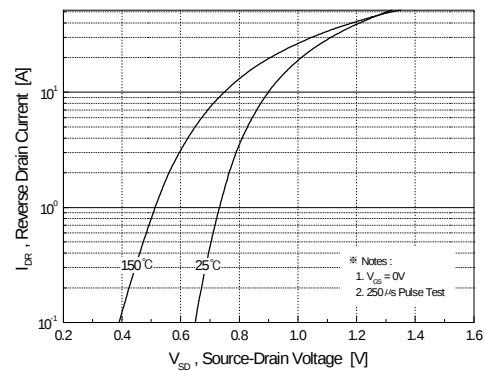


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

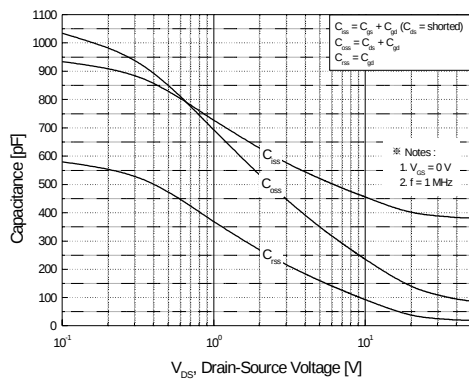


Figure 5. Capacitance Characteristics

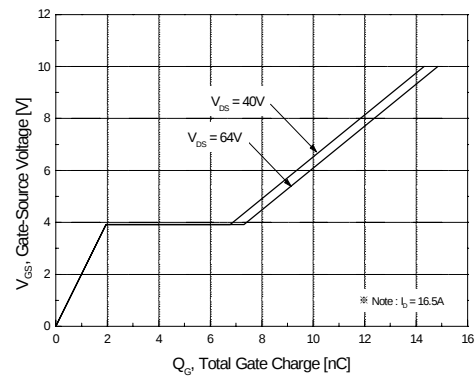


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

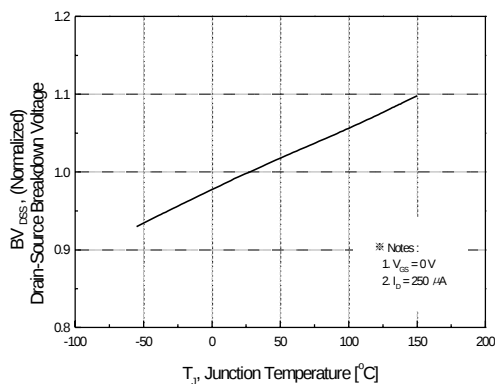


Figure 7. Breakdown Voltage Variation vs. Temperature

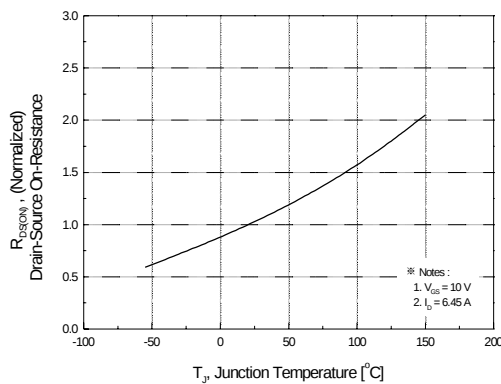


Figure 8. On-Resistance Variation vs. Temperature

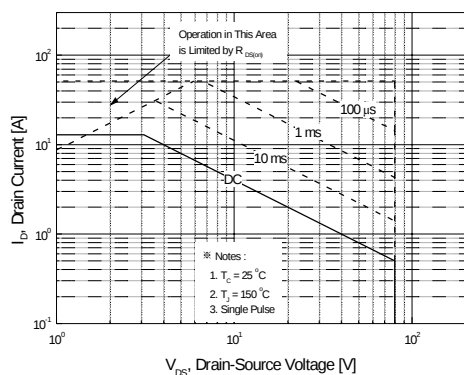


Figure 9. Maximum Safe Operating Area

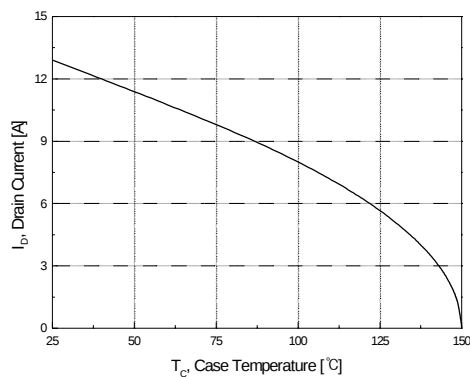


Figure 10. Maximum Drain Current vs. Case Temperature

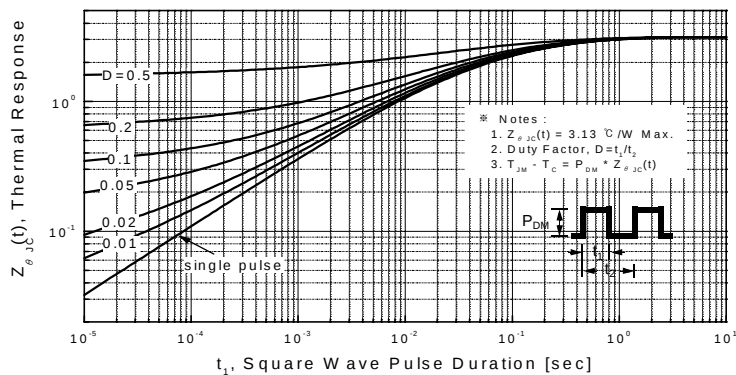
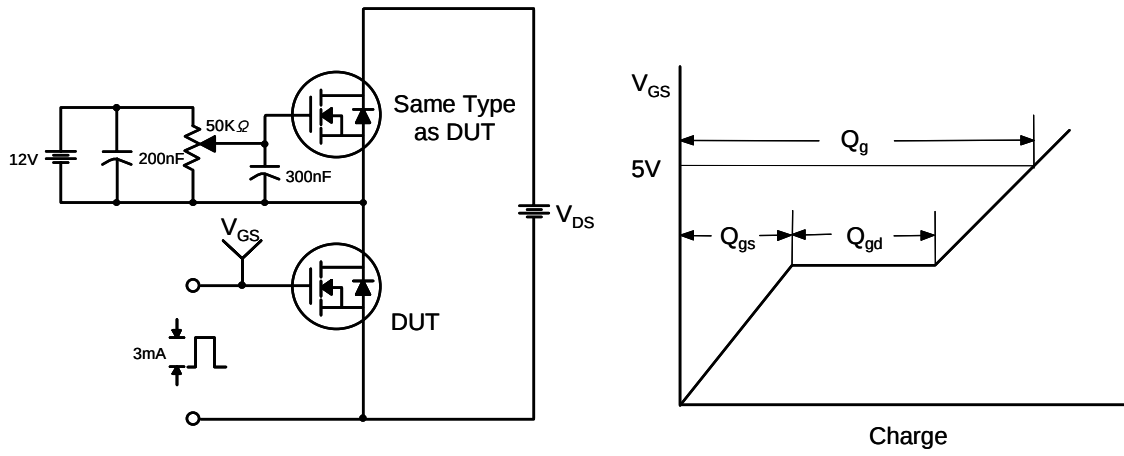
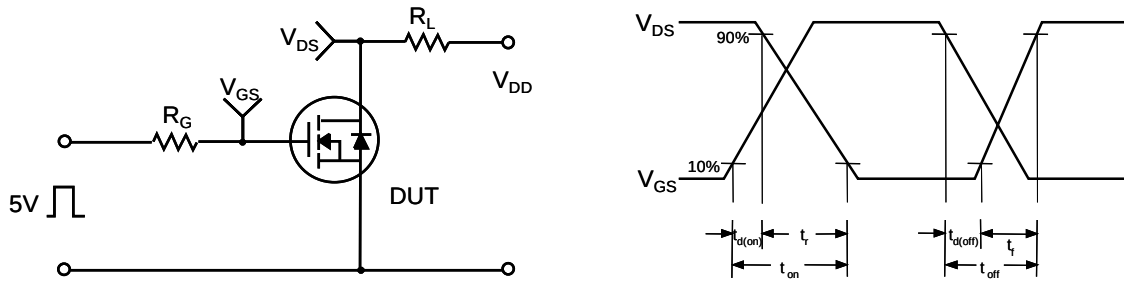


Figure 11. Transient Thermal Response Curve

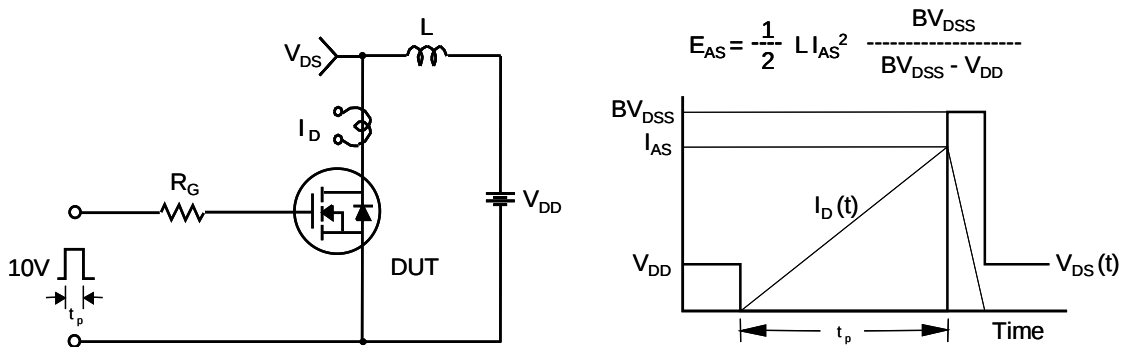
Gate Charge Test Circuit & Waveform



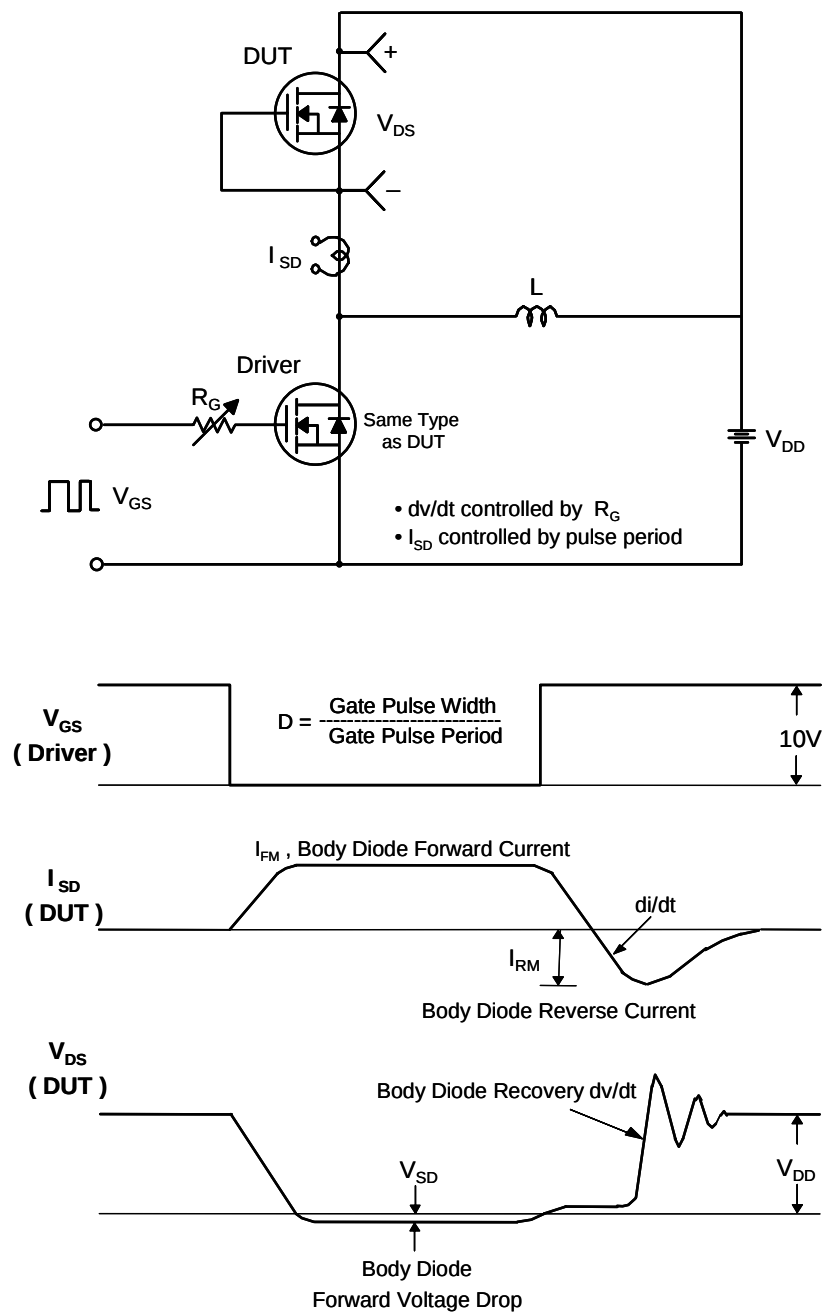
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

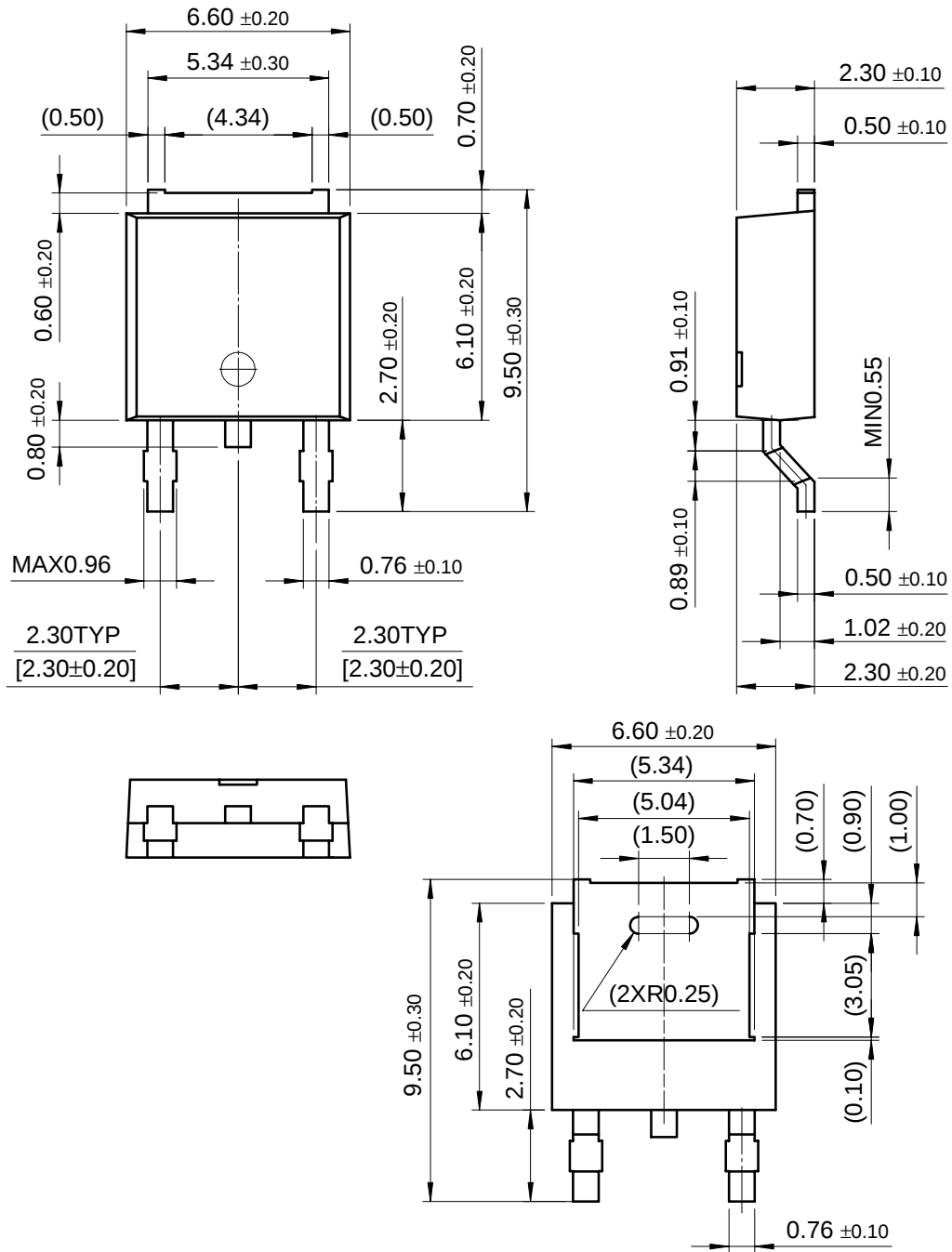


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

DPAK



Technical drawing of a 3-pin connector. The drawing includes a top view, a side view, and a cross-sectional view. Dimensions are provided in millimeters with tolerances.

Top View Dimensions:

- Overall width: 6.60 ± 0.20
- Distance between pins: 5.34 ± 0.20
- Pin width: 0.76 ± 0.10
- Pin spacing from center: 2.30 TYP (range $[2.30 \pm 0.20]$)
- Pin length: 1.80 ± 0.20
- Pin thickness: 0.80 ± 0.10
- Maximum pin width: $\text{MAX} 0.96$

Side View Dimensions:

- Overall height: 16.10 ± 0.30
- Top flange width: 2.30 ± 0.20
- Top flange thickness: 0.50 ± 0.10
- Pin diameter: 0.50 ± 0.10

Cross-sectional View:

- Shows the internal structure of the connector, including the pins and the housing.

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