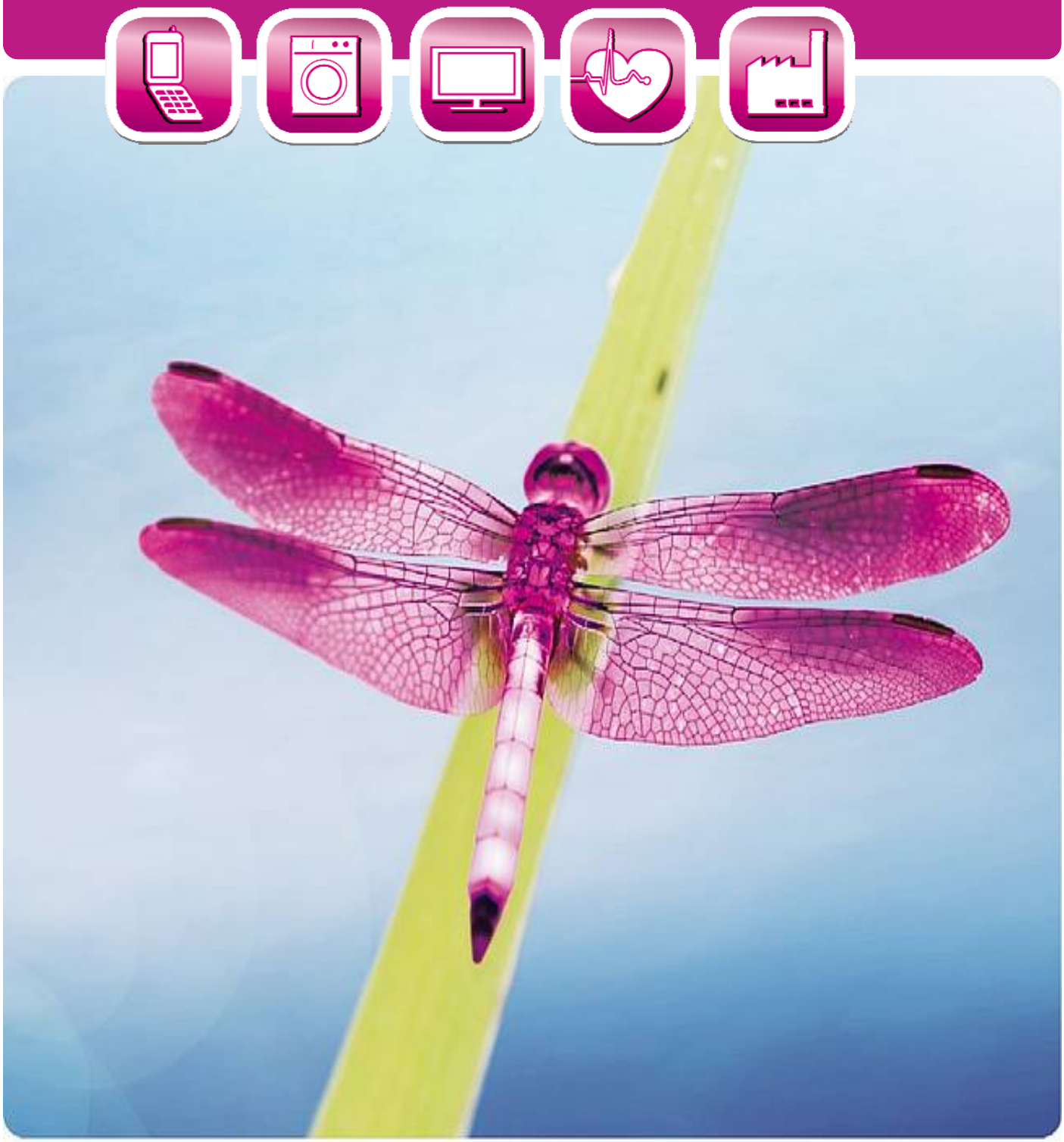
The Analog Mixed Signal Company

Data Sheet

Rev. **2.0** / **October 2011**

ZADCS1282/1242/1222

12-Bit, 200ksps, ADC Family



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Brief Description

The ZMDI ZADCS1282/ZADCS1242/ZADCS1222 are 12-Bit low power analog-to-digital (A/D) converters with up to 250ksps conversion rate. The converter is based on successive-approximation-register architecture.
All converters have an 8-channel input multiplexer and a high-bandwidth a track/hold circuit. All analog inputs are software configurable as eight / four/two single ended or four/two/one differential analog input channels as well as for unipolar or bipolar output coding.
The ZADCS1282/ ZADCS1242/ ZADCS1222 operate from a single +2.7V to +5.25V supply.
The synchronous four wire serial interface connects directly to a microcontroller using one of the standards like SPI™, QSPI™, and Microwire™ without external components.
The ZADCS1282/ZADCS1242/ZADCS1222 use either the external serial-interface clock or an internally generated clock to perform successive-approximation analog-to-digital conversions. The internal clock mode can be used to run synchronous conversions on several ZMDI ADCs in parallel.
The "V" versions ZADCS1282V/ZADCS1242V/ ZADCS1222V are equipped with a high accurate internal 2.5V reference with an additional external ±1.5% voltage adjustment range.
The device provides a hard-wired shut-down pin (nSHDN) and software-selectable power-down modes to automatically shut down the IC at the end of a conversion. Accessing the serial interface automatically powers up the ZADCS1282/ ZADCS1242/ZADCS1222. A quick turn-on time allows the device to be shut down between measurements.

Features

- 12-Bit resolution SAR ADC
- 2/4/8 channel single or 1/2/4 channel diff. inputs
- Software configurable uni- or bipolar output code
- SPI™/QSPI™, Microwire™ compatible serial interface
- No missing codes
- Low power consumption
- Internal 2.5V reference (only "V" version - ZADCS1282V/ ZADCS1242V/ZADCS1222V)
- Software programmable power down mode
- Single-Supply Operation +2.5V to +5.25V

Benefits

- Scalable system solutions possible due to upward/downward compatibility within the family (8, 10, 12 bit resolution, 2, 4, 8 channels)
- Accurate measurements
- Long battery life cycles due to low power consumption
- Synchronous sampling with several ZADCS parts in parallel

Available Support

- ZADCS1282 Kit
  - Evaluation Kit for ZMDI ZADCS12x2 Family based on ZADCS1282 device
  - Standalone and PC based operation modus
  - USB 2.0 (1.1) compatible
  - User Interface for PC operated modus
  - Graphical oscilloscope appl. and FFT analyzer

Physical Characteristics

- ADC resolution ..... 12 Bit
- Conversion rate..... 200 ksps
- Power supply rate ..... 2.7V to 5.25V
- INL..... ±1 LSB max.
- DNL ..... ±1 LSB max.
- SINAD ..... >70 dB
- Standby (idle) current..... <0.5 µA
- Current consumption @ 200 ksps, 3V supply
  - with internal reference ..... < 1.2 mA
  - without internal reference ..... < 0.9 mA
- Temperature range ..... -25°C to +85°C
- 14 / 16 / 20-Pin SSOP package

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12-Bit, 200ksps, ADC Family

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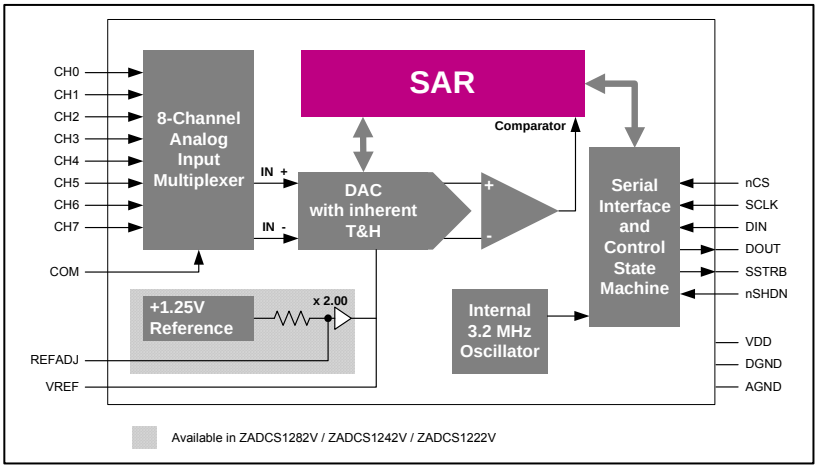
Typical Applications

- Embedded control & real time appl.
- Industrial control & process control applications
- Motion control applications
- Three phase motor control
- Power generation (Solar, Windmills, etc.)
- Data Acquisition
- Portable Data Logging
- Battery-Powered Systems
- Automotive

ZADCS1282 Block Diagram



Ordering Information

Order Code	Resolution [Bit]	Channels [number]	Sample Rate [ksps]	Temperature range [°C]	Internal Vref	INL	DNL	Pins [number]	Package [Type]	Packing
ZADCS1282VIS20T	12	8	200	-25°C to +85°C	✓	± 1 LSB	± 1 LSB	20	SSOP	Tube
ZADCS1282IS20T	12	8	200	-25°C to +85°C	--	± 1 LSB	± 1 LSB	20	SSOP	Tube
ZADCS1242VIS16T	12	4	200	-25°C to +85°C	✓	± 1 LSB	± 1 LSB	16	SSOP	Tube
ZADCS1242IS16T	12	4	200	-25°C to +85°C	--	± 1 LSB	± 1 LSB	16	SSOP	Tube
ZADCS1222VIS14T	12	2	200	-25°C to +85°C	✓	± 1 LSB	± 1 LSB	14	SSOP	Tube
ZADCS1222IS14T	12	2	200	-25°C to +85°C	--	± 1 LSB	± 1 LSB	14	SSOP	Tube

Sales and Further Information

www.zmdi.com adc@zmdi.com

Zentrum Mikroelektronik Dresden AG
Grenzstrasse 28
01109 Dresden
Germany

Phone +49 (0)351.8822.7232
Fax +49 (0)351.8822.87232

ZMD America, Inc.
8413 Excelsior Drive
Suite 200
Madison, WI 53717
USA

Phone +1 (608) 829-1987
Fax +1 (631) 549-2882

Zentrum Mikroelektronik Dresden AG, Japan Office
2nd Floor, Shinbashi Tokyu Bldg.
4-21-3, Shinbashi, Minato-ku
Tokyo, 105-0004
Japan

Phone +81.3.6895.7410
Fax +81.3.6895.7301

ZMD FAR EAST, Ltd.
3F, No. 51, Sec. 2,
Keelung Road
11052 Taipei
Taiwan

Phone +886 2 2377 8189
Fax +886 2 2377 8199

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1 General Device Specification

1.1. Absolute Maximum Ratings (Non Operating)

Symbol	Parameter	Min	Max	Unit	Note
V_{DD-GND}	VDD to AGND, DGND	-0.3	6	V	
$V_{AGND-DGND}$	AGND to DGND	-0.3	0.3	V	
	CH0 – CH7, COM to AGND, DGND	-0.3	VDD+0.3	V	
	VREF, VREFADJ to AGND	-0.3	VDD+0.3	V	
	Digital Inputs to DGND	-0.3	6	V	
	Digital Outputs to DGND	-0.3	VDD+0.3	V	
	Digital Output Sink Current		25	mA	
I_{in}	Input current into any pin except supply pins (Latch-Up)	-100	100	mA	
V_{HBM}	Electrostatic discharge – Human Body Model (HBM)	2000		V	1
θ_{JCT}	Maximum Junction Temperature		+150°	°C	
θ_{OP}	Operating Temperature Range	-25	+85		
θ_{STG}	Storage temperature	-65	+150	°C	
θ_{lead}	Lead Temperature 100%Sn	JEDEC-J-STD-20C 260		°C	
H	Humidity non-condensing				2
P_{tot}	Total power dissipation		250	mW	
R_{thj}	Thermal resistance of Package SSOP20 / 5.3mm		100	K/W	

Table 1: Absolute Maximum Ratings

1 HBM: C = 100pF charged to V_{HBM} with resistor R = 1.5kΩ in series, valid for all pins

2 Level 4 according to JEDEC-020A is guaranteed

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1.2. Package Pin Assignment ZADCS1282 / ZADCS1282V

Package pin number	Name	Direction	Type	Description
1	nCS	IN	CMOS Digital	Active Low Chip Select
2	DIN	IN	CMOS Digital	Serial Data Input
3	DGND		SUPPLY	Digital Ground
4	AGND		SUPPLY	Analog Ground
5	VREF	I/O	Analog	Reference Buffer Output / External Reference Input
6	COM	IN	Analog	Ground reference for analog inputs in single ended mode
7	CH0	IN	Analog	Analog Input Channel 0
8	CH1	IN	Analog	Analog Input Channel 1
9	CH4	IN	Analog	Analog Input Channel 4
10	CH5	IN	Analog	Analog Input Channel 5
11	CH7	IN	Analog	Analog Input Channel 7
12	CH6	IN	Analog	Analog Input Channel 6
13	CH3	IN	Analog	Analog Input Channel 3
14	CH2	IN	Analog	Analog Input Channel 2
15	REFADJ	I/O	Analog	Input to Reference Buffer Amplifier
16	VDD		SUPPLY	Positive Supply
17	nSHDN	IN	CMOS Digital	Active Low Shutdown
18	DOUT	OUT	CMOS Digital	Serial Data Output
19	SSTRB	OUT	CMOS Digital	Serial Strobe Output
20	SCLK	IN	CMOS Digital	Serial Clock Input

Table 2: Pin list ZADCS1282 / ZADCS1282V

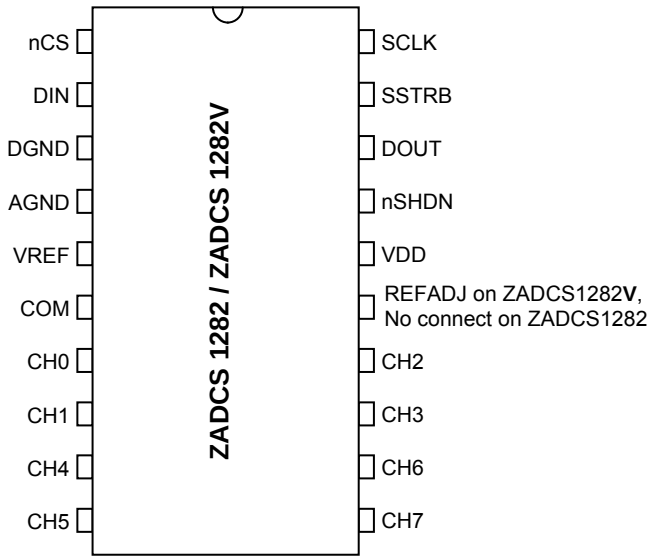

Figure 1 Package Pin Assignment for ZADCS1282 & ZADCS1282V

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1.3. Package Pin Assignment ZADCS1242 / ZADCS1242V

Package pin number	Name	Direction	Type	Description
1	nCS	IN	CMOS Digital	Active Low Chip Select
2	DIN	IN	CMOS Digital	Serial Data Input
3	DGND		SUPPLY	Digital Ground
4	AGND		SUPPLY	Analog Ground
5	VREF	I/O	Analog	Reference Buffer Output / External Reference Input
6	COM	IN	Analog	Ground reference for analog inputs in single ended mode
7	CH0	IN	Analog	Analog Input Channel 0
8	CH1	IN	Analog	Analog Input Channel 1
9	CH3	IN	Analog	Analog Input Channel 3
10	CH2	IN	Analog	Analog Input Channel 2
11	REFADJ	I/O	Analog	Input to Reference Buffer Amplifier
12	VDD		SUPPLY	Positive Supply
13	nSHDN	IN	CMOS Digital	Active Low Shutdown
14	DOUT	OUT	CMOS Digital	Serial Data Output
15	SSTRB	OUT	CMOS Digital	Serial Strobe Output
16	SCLK	IN	CMOS Digital	Serial Clock Input

Table 3: Pin list ZADCS1242 / ZADCS1242V

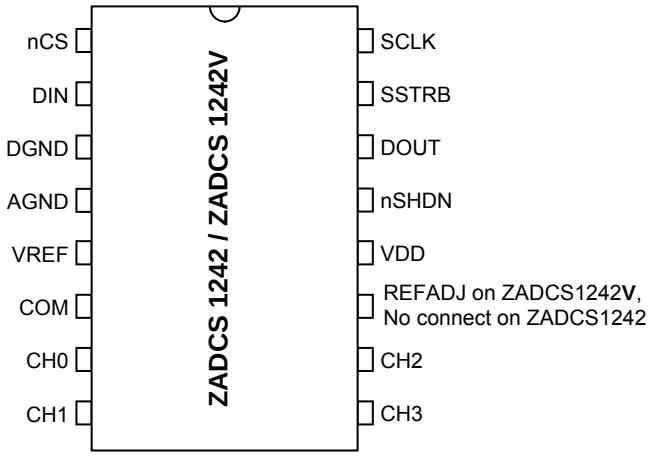

Figure 2 Package Pin Assignment for ZADCS1242 & ZADCS1242V

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1.4. Package Pin Assignment ZADCS1222 / ZADCS1222V

Package pin number	Name	Direction	Type	Description
1	nCS	IN	CMOS Digital	Active Low Chip Select
2	DIN	IN	CMOS Digital	Serial Data Input
3	DGND		SUPPLY	Digital Ground
4	AGND		SUPPLY	Analog Ground
5	VREF	I/O	Analog	Reference Buffer Output / External Reference Input
6	COM	IN	Analog	Ground reference for analog inputs in single ended mode
7	CH0	IN	Analog	Analog Input Channel 0
8	CH1	IN	Analog	Analog Input Channel 1
9	REFADJ	I/O	Analog	Input to Reference Buffer Amplifier
10	VDD		SUPPLY	Positive Supply
11	nSHDN	IN	CMOS Digital	Active Low Shutdown
12	DOUT	OUT	CMOS Digital	Serial Data Output
13	SSTRB	OUT	CMOS Digital	Serial Strobe Output
14	SCLK	IN	CMOS Digital	Serial Clock Input

Table 4: Pin list ZADCS1222 / ZADCS1222V

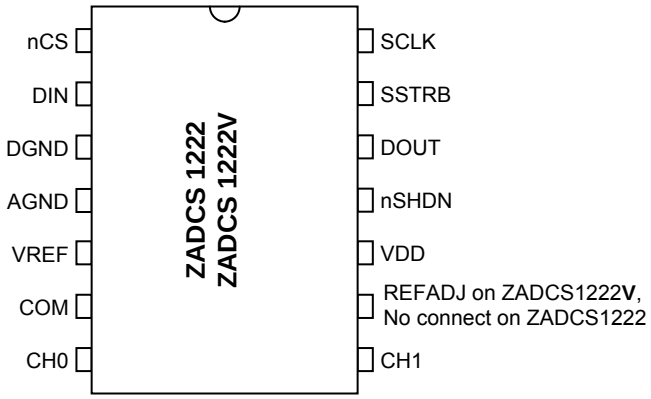

Figure 3 Package Pin Assignment for ZADCS1222 & ZADCS1222V

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1.5. Electrical Characteristics

1.5.1. General Parameters

(VDD = +2.7V to + 5.25V; f_{SCLK} = 3.2MHz (50% duty cycle); 16 clocks/conversion cycle (200 ksps); V_{REF} = 2.500V applied to VREF pin; $\theta_{OP} = \theta_{OPmin} \ldots \theta_{OPmax}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC Accuracy						
Resolution				12		Bits
Relative Accuracy	INL	ZADCS1282 / ZADCS1282**V** ZADCS1242 / ZADCS1242**V** ZADCS1222 / ZADCS1222**V**			± 1.0	LSB
No Missing Codes	NMC		12			Bits
Differential Nonlinearity	DNL	ZADCS1282 / ZADCS1282**V** ZADCS1242 / ZADCS1242**V** ZADCS1222 / ZADCS1222**V**			± 1.0	LSB
Offset Error				± 0.5	± 3.0	LSB
Gain Error				± 0.5	± 4.0	LSB
Gain Temperature Coefficient				± 0.25		ppm/°C
Dynamic Specifications (10kHz sine-wave input, 0V to 2.500Vpp, 200ksps, 3.2MHz external clock)						
Signal-to-Noise + Distortion Ratio	SINAD		70	73		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-88	-80	dB
Spurious-Free Dynamic Range	SFDR		76	80		dB
Small-Signal Bandwidth		-3dB roll off		3.8		MHz
Conversion Rate						
Sampling Time (= Track/Hold Acquisition Time)	t_{ACQ}	Ext. Clock = 3.2MHz, 2.5 clocks/ acquisition	0.758			µs
Conversion Time	t_{CONV}	Ext. Clock = 3.2MHz, 12 clocks/ conversion			3.75	µs
		Int. Clock = 3.2MHz +/- 12% tolerance	3.30		4.20	µs
Aperture Delay				30		ns
Aperture Jitter				< 50		ps
External Clock Frequency			0.1		3.2	MHz
Internal Clock Frequency			2.81	3.2	3.58	MHz
Analog Inputs						
Input Voltage Range, Single-Ended and Differential		Unipolar, COM = 0V	0 to VREF			V
		Bipolar, COM = VREF/2	± VREF / 2			
Input Capacitance				16		pF

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1.5.2. Specific Parameters of ZADCS12x2V versions (with Internal Reference)

(VDD = +2.7V to + 5.25V; f_{SCLK} = 3.2MHz (50% duty cycle); 16 clocks/conversion cycle (200 ksps); $\theta_{OP} = \theta_{OPmin} \ldots \theta_{OPmax}$)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Internal Reference at VREF							
VREF Output Voltage		T_A = + 25°C		2.480	2.500	2.520	V
VREF Short-Circuit Current						30	mA
VREF Temperature Coefficient					± 30	± 50	ppm/°C
Load Regulation		0 to 0.2mA output load			0.35		mV
Capacitive Bypass at VREF				4.7			µF
Capacitive Bypass at REFADJ				0.047			µF
REFADJ Adjustment Range					± 1.5		%
External Reference at VREF (internal buffer disabled by V(REFADJ) = VDD)							
VREF Input Voltage Range				1.0		VDD + 50mV	V
VREF Input Current		VREF = 2.5V			180	215	µA
VREF Input Resistance				11.5	14		kΩ
Shutdown VREF Input Current						0.1	µA
REFADJ Buffer Disable Threshold				VDD-0.5			V
External Reference at VREF_ADJ							
Reference Buffer Gain					2.00		
VREF_ADJ Input Current						±80	µA
Full Power Down VREFADJ Input Current		Full Power-Down mode				0.1	µA
Power Requirements							
Positive Supply Voltage	VDD			2.7		5.25	V
Positive Supply Current ZADCS1282**VI** ZADCS1242**VI** ZADCS1222**VI**	IDD	VDD=3.6V	Operating Mode ext. VREF		0.85	1.0	mA
			Operating Mode int. VREF		1.3	1.4	mA
			Fast Power-Down		250	300	µA
			Full Power-Down		0.5	4.0	
Positive Supply Current ZADCS1282**VI** ZADCS1242**VI** ZADCS1222**VI**	IDD	VDD=5.2V	Operating Mode ext. VREF		1.00	1.3	mA
			Operating Mode int. VREF		1.40	1.6	mA
			Fast Power-Down		250	300	µA
			Full Power-Down		0.5	4.0	

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1.5.3. Specific Parameters of basic ZADCS12x2 versions (without Internal Reference)

(VDD = +2.7V to + 5.25V; f_{SCLK} = 3.2MHz (50% duty cycle); 16 clocks/conversion cycle (200 ksps); $\theta_{OP} = \theta_{OPmin} \ldots \theta_{OPmax}$)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
External Reference at VREF							
VREF Input Voltage Range				1.0		VDD + 50mV	V
VREF Input Current		VREF = 2.5V			180	215	µA
VREF Input Resistance				11.5	14		kΩ
Shutdown VREF Input Current						0.1	µA
Capacitive Bypass at VREF				4.7			µF
Power Requirements							
Positive Supply Voltage	VDD			2.7		5.25	V
Positive Supply Current ZADCS1282**I** ZADCS1242**I** ZADCS1222**I**	IDD	VDD = 3.6V	Operating Mode		0.85	1.0	µA
			Full Power-Down		0.5	4.0	
Positive Supply Current ZADCS1282**I** ZADCS1242**I** ZADCS1222**I**	IDD	VDD = 5.25V	Operating Mode		1.00	1.3	µA
			Full Power-Down		0.5	4.0	

1.5.4. Digital Pin Parameters

(VDD = +2.7V to + 5.25V; f_{SCLK} = 3.2MHz (50% duty cycle); 16 clocks/conversion cycle (200 ksps); $\theta_{OP} = \theta_{OPmin} \ldots \theta_{OPmax}$)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Digital Inputs (DIN, SCLK, CS, nSHDN)							
Logic High Level	V_{IH}	VDD = 2.7V		1.9			V
		VDD = 5.25V		3.3			V
Logic Low Level	V_{IL}	VDD = 2.7V				0.7	V
		VDD = 5.25V				1.4	V
Hysteresis	V_{Hyst}			0.7			V
Input Leakage	I_{IN}	VIN = 0V or VDD			± 0.1	± 1.0	µA
Input Capacitance	C_{IN}				5		pF
Digital Outptus (DOUT, SSTRB)							
Output High Current	I_{OH}	V_{OH}= VDD – 0.5V	VDD = 2.7V	3.5		8.5	mA
			VDD = 5.25V	5.5		10.8	mA
Output Low Voltage	I_{OL}	V_{OL}= 0.4V	VDD = 2.7V	4		11.5	mA
			VDD = 5.25V	6.4		15.3	mA
Three-State Leakage Current	I_{Leak}	nCS = VDD			± 0.1	± 1.0	µA
Three-State Output Capacitance	C_{OUT}	nCS = VDD			5		pF

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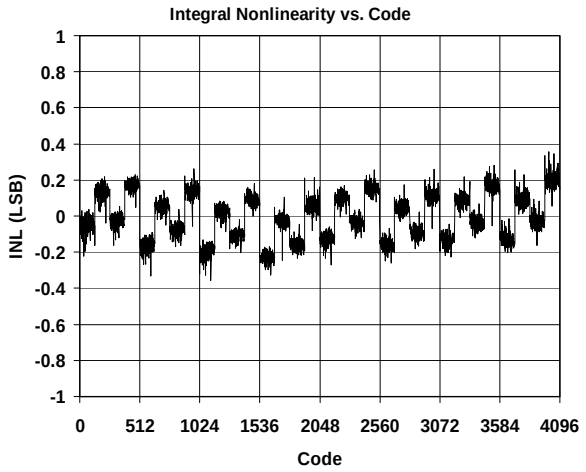
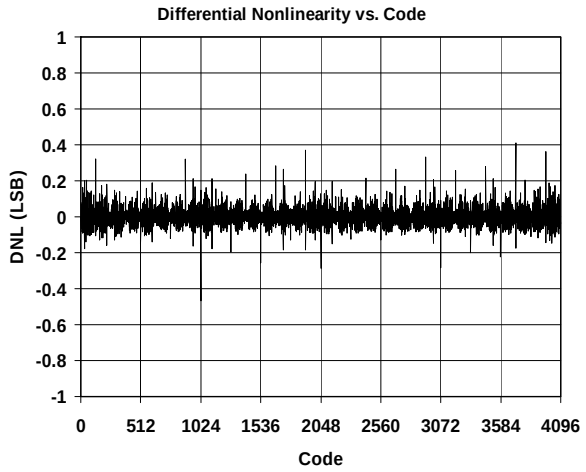
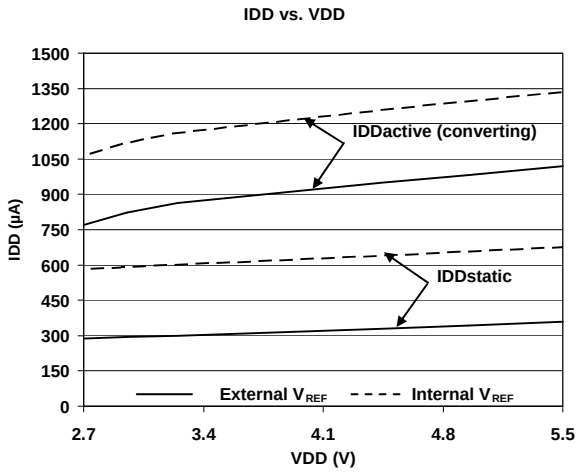
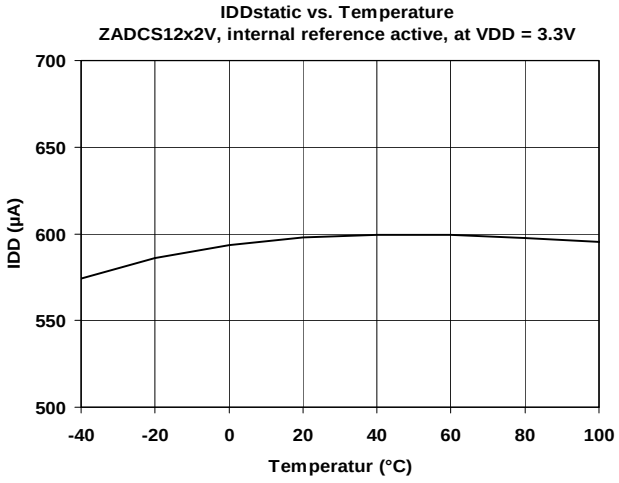
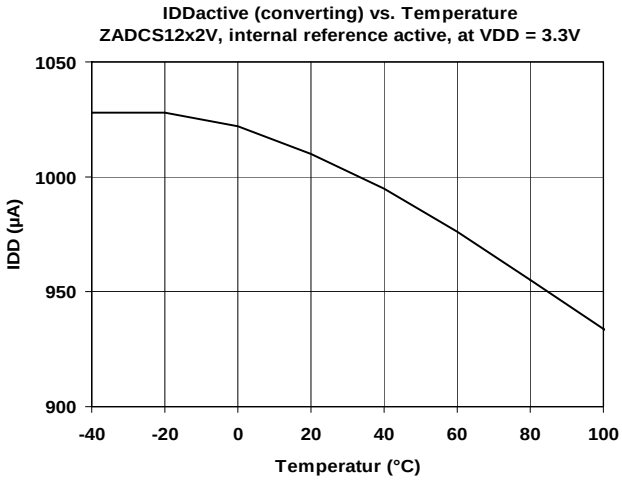
1.6. Typical Operating Characteristics

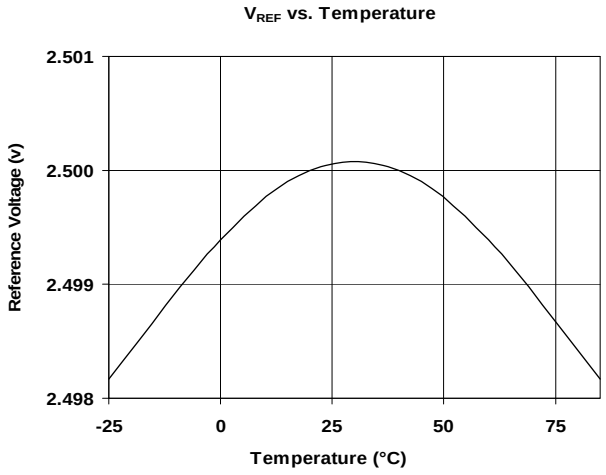












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2 Detailed Description

2.1. General Operation

The ZADCS12x2 family is a set of classic successive approximation register (SAR) type converters. The architecture is based on a capacitive charge redistribution DAC merged with a resistor string DAC building a hybrid converter with excellent monotonicity and DNL properties. The Sample & Hold function is inherent to the capacitive DAC. This avoids additional active components in the signal path that could distort the input signal or introduce errors.

All devices in the ZADCS12x2 family build on the same converter core and differ only in the number of input channels and the availability of an internal reference voltage generator. The ZADCS12x2**V** versions are equipped with a highly accurate internal 1.25V bandgap reference which is available at the VREFADJ pin. The bandgap voltage is further amplified by an internal buffer amplifier to 2.50V that is available at pin VREF. All other versions come without the internal reference and the internal buffer amplifier. They require an external reference supplied at VREF, with the benefit of considerably lower power consumption.

A basic application schematic for ZADC1282**V** is shown in Figure 4, for ZADCS1282 in Figure 5. ZADCS1282**V** can also be operated with an external reference, if VREFADJ is tied to VDD.

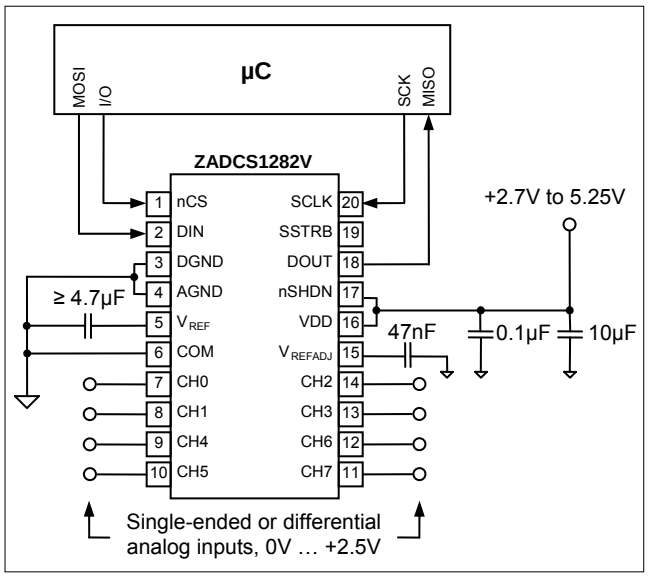

Figure 4: Basic application schematic for ZADCS1282V

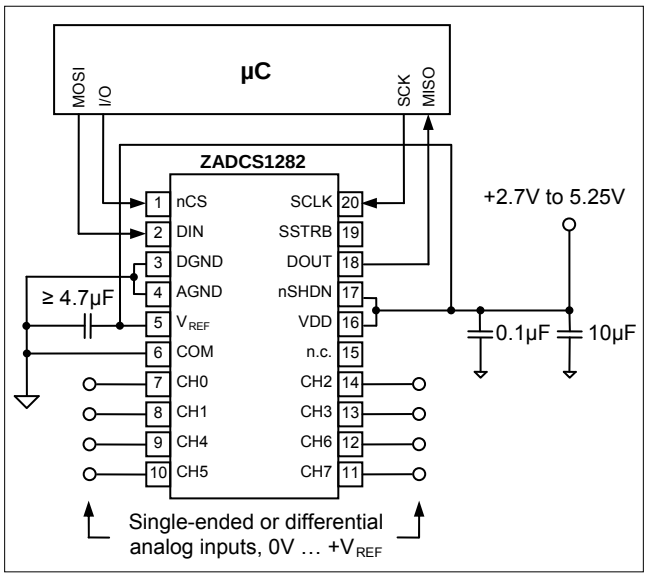

Figure 5: Basic application schematic for ZADCS1282

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	IN+								IN-
1	0	0		IN+							IN-
0	0	1			IN+						IN-
1	0	1				IN+					IN-
0	1	0					IN+				IN-
1	1	0						IN+			IN-
0	1	1							IN+		IN-
1	1	1								IN+	IN-

Table 5: Channel selection in Single Ended Mode

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	IN+	IN-						
0	0	1			IN+	IN-				
0	1	0					IN+	IN-		
0	1	1							IN+	IN-
1	0	0	IN-	IN+						
1	0	1			IN-	IN+				
1	1	0					IN-	IN+		
1	1	1							IN-	IN+

Table 6: Channel selection in Differential Mode

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2.2. Analog Input

The analog input to the converter is fully differential. Both converter input signals IN_+ and IN_- (see Functional Block diagram at front page) get sampled during the acquisition period enabling the converter to be used in fully differential applications where both signals can vary over time.

The ZADCS12x2 family converters do not require that the negative input signal be kept constant within ± 0.5LSB during the entire conversion as is commonly required by converters featuring pseudo differential operation only.

The input signals can be applied single ended, referenced to the COM pin, or differential, using pairs of the input channels. The desired configuration is selectable for every conversion via the Control-Byte received on DIN pin of the digital interface (see further description below)

A block diagram of the input multiplexer is shown in Figure 8. Table 5 and Table 6 show the relationship of the Control-Byte bits A2, A1, A0 and SGL/DIF to the configuration of the analog multiplexer. The entire table applies only to ZADCS1282 devices. For ZADCS1242 devices bit A1 is don't care, for ZADCS1222 devices A1 and A0 are don't care.

Both input signals IN_+ and IN_- are generally allowed to swing between –0.2V and VDD+0.2V. However, depending on the selected conversion mode – uniploar or bipolar – certain input voltage relations can limit the output code range of the converter.

In unipolar mode the voltage at IN_+ must exceed the voltage at IN_- to obtain codes unequal to 0x00. The entire 8 bit transfer characteristic is then covered by IN_+ if IN_+ ranges from IN_- to (IN_-+Vref). Any voltage on IN_+>(IN_-+Vref) results in code 0xFF. Code 0xFF is not reached, if (IN_-+Vref) > VDD + 0.2V because the input voltage is clamped at VDD + 0.2V by ESD protection devices.

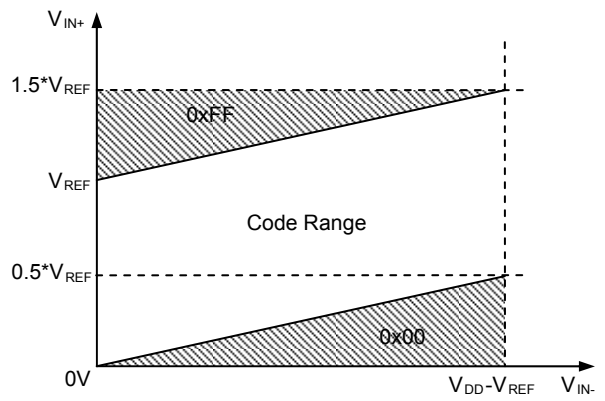

Figure 6: Input voltage range in unipolar mode

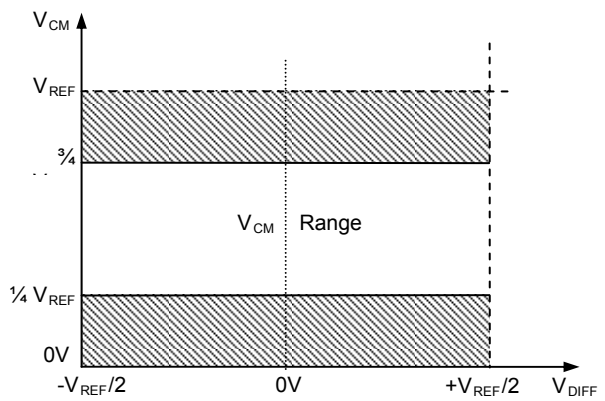

Figure 7: Input voltage range for bipolar mode

The voltage at IN_- can range from -0.2V … ½ V_{REF} without limiting the Code Range, assuming the fore mentioned VDD condition is true. See also Figure 6 for input voltage ranges in unipolar conversion mode.

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In bipolar mode, IN_+ can range from (IN_- - Vref/2) to (IN_-+Vref/2) keeping the converter out of code saturation. For instance, if IN_- is set to a constant DC voltage of Vref/2, then IN_+ can vary from 0V to V_{REF} to cover the entire code range. Lower or higher voltages of IN_+ keep the output code at the minimum or maximum code value.

Figure 7 shows the input voltage ranges in bipolar mode when IN_- is set to a constant DC voltage.

As explained before, converters out of the ZADCS12x2 family can also be used to convert fully differential input signals that change around a common mode input voltage.

The bipolar mode is best used for such purposes since it allows the input signals to be positive or negative in relation to each other.

The common mode level of a differential input signal is calculated $V_{CM} = (V(IN_+) + V(IN_-)) / 2$. To avoid code clipping or over steering of the converter, the common mode level can change from ¼ V_{REF} … ¾ V_{REF}. Within this range the peak to peak amplitude of the differential input signal can be ± $V_{REF}/2$.

The average input current on the analog inputs depends on the conversion rate. The signal source must be capable of charging the internal sampling capacitors (typically 16pF on each input of the converter: IN_+ and IN_-) within the acquisition time t_{ACQ} to the required accuracy. The equivalent input circuit in sampling mode is shown in Figure 9.

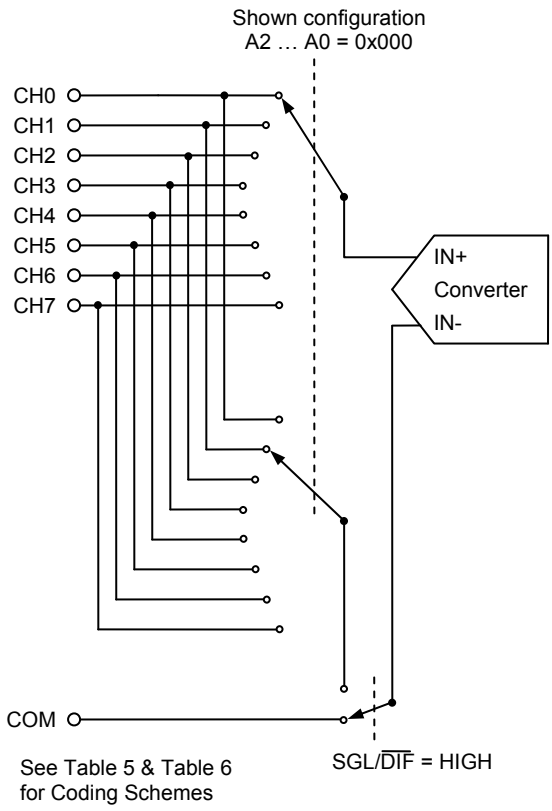

Figure 8: Block diagram of input multiplexer

The following equation provides a rough hand calculation for a source impedance R_S that is required to settle out a DC input signal referenced to AGND with 8 bit accuracy in a given acquisition time

$$R_S \le \frac{t_{ACQ}}{9 \times C_{IN}} - R_{SW}$$

For example, if f_{SCLK} = 3.2MHz, the acquisition time is t_{ACQ} = 781.25ns. Thus the output impedance of the signal source R_S must be less than

$$R_S \le \frac{781.25\text{ns}}{9 \times 20\text{pF}} - 3\text{k}\Omega = 1.34\text{k}\Omega$$

If the output impedance of the source is higher than the calculated maximum R_S the acquisition time must be extended by reducing f_{SCLK} to ensure 8 bit accuracy. Another option is to add a capacitor of > 20nF to the individual input. Although this limits the bandwidth of the input signal because an RC low pass filter is build

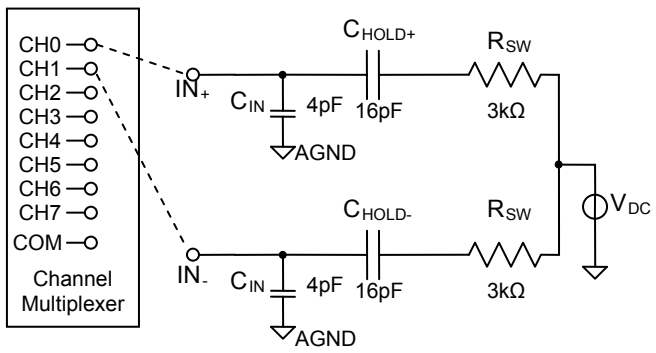

Figure 9: Equivalent input circuit during sampling

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together with the source impedance, it may be useful for certain applications.

The small-signal bandwidth of the input tracking circuitry is 3.8MHz. Hence it is possible to digitize high-speed transient events and periodic signals with frequencies exceeding the ADC's sampling rate. This allows the application of certain under-sampling techniques like down conversion of modulated high frequency signals.

Be aware that under-sampling techniques still require a bandwidth limitation of the input signal to less than the Nyquist frequency of the converter to avoid aliasing effects. Also, the output impedance of the input source must be very low to achieve the mentioned small signal bandwidth in the overall system.

2.3. Internal & External Reference

ZADCS12x2**V** family members are equipped with a highly accurate internal 2.5V reference voltage source. The voltage is generated from a trimmed 1.25V bandgap with an internal buffer that is set to a gain of 2.00. The bandgap voltage is supplied at VREFADJ with an output impedance of 20kΩ. An external capacitor of 47nF at VREFADJ is useful to further decrease noise on the internal reference.
The VREFADJ pin also provides an opportunity to externally adjust the bandgap voltage in a limited range (see Figure 10) as well as the possibility to overdrive the internal bandgap with an external 1.25V reference.
The internal bandgap reference and the VREF buffer can be shut down completely by setting VREFADJ to VDD. This reduces power consumption of the ZADCS12x2**V** devices and allows the supply of an external reference at VREF.

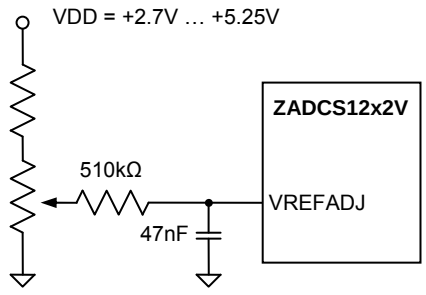

Figure 10: Reference Adjust Circuit

Basic ZADCS12x2 devices do not contain the internal bandgap or the VREF buffer. An external reference must be supplied all the time at VREF.
The value of the reference voltage at VREF sets the input range of the converter and the analog voltage weight of each digital code. The size of the LSB (least significant bit) is equal to the value of VREF (reference to AGND) divided by 4096. For example at a reference voltage of 2.500V, the voltage level of a LSB is equal to 0.610mV.

The average current consumption at VREF depends on the value of VREF and the sampling frequency. Two effects contribute to the current at VREF, a resistive connection from VREF to AGND and charge currents that result from the switching and recharging of the capacitor array (CDAC) during sampling and conversion. For an external reference of 2.5V the input current at VREF is approximately 100µA.

2.4. Digital Interface

All devices out of the ZADCS12x2 family are controlled by a 4-wire serial interface that is compatible to SPI™, QSPI™ and MICROWIRE™ devices without external logic. Any conversion is started by sending a control byte into DIN while nCS is low. A typical sequence is shown in Figure 11.

The control byte defines the input channel(s), unipolar or bipolar operation and output coding, single-ended or differential input configuration, external or internal conversion clock and the kind of power down that is activated after the completion of a conversion. A detailed description of the control bits can be obtained from Figure 11. As it can also be seen in Figure 11 the acquisition of the input signal occurs at the end of the control byte for 2.5 clock cycles. Outside this range, the Track & Hold is in hold mode.

The conversion process is started, with the falling clock edge (SCLK) of the eighth bit in the control byte. It takes twelve clock cycles to complete the conversion and one additional cycle to shift out the last bit of the conversion result. During the remaining seven clock cycles the output is filled with zeros in 24-Clock Conversion Mode. Depending on what clock mode was selected, either the external SPI clock or an internal clock is used to drive the successive approximation. Figure 12 shows the Timing for Internal Clock Mode.

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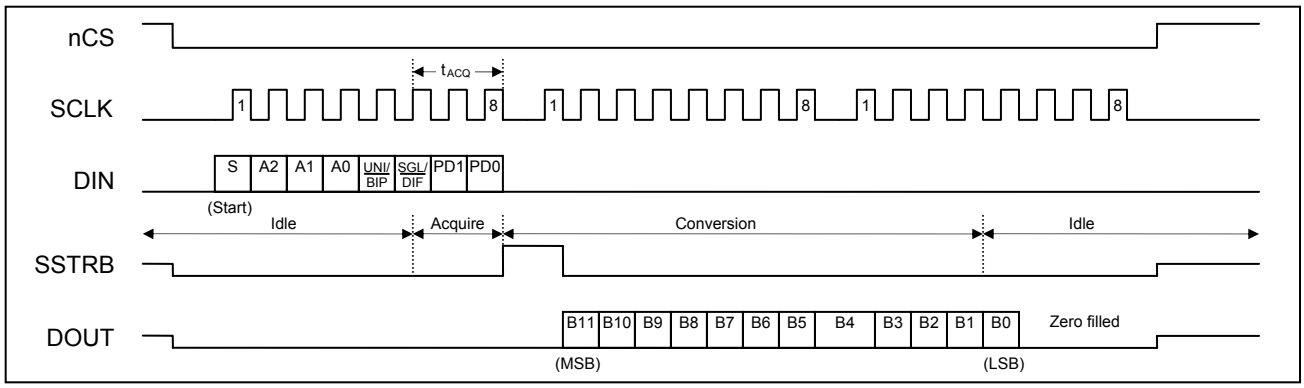

Figure 11: 24-Clock External Clock Mode Timing ($f_{SCLK} \leq 3.2MHz$)

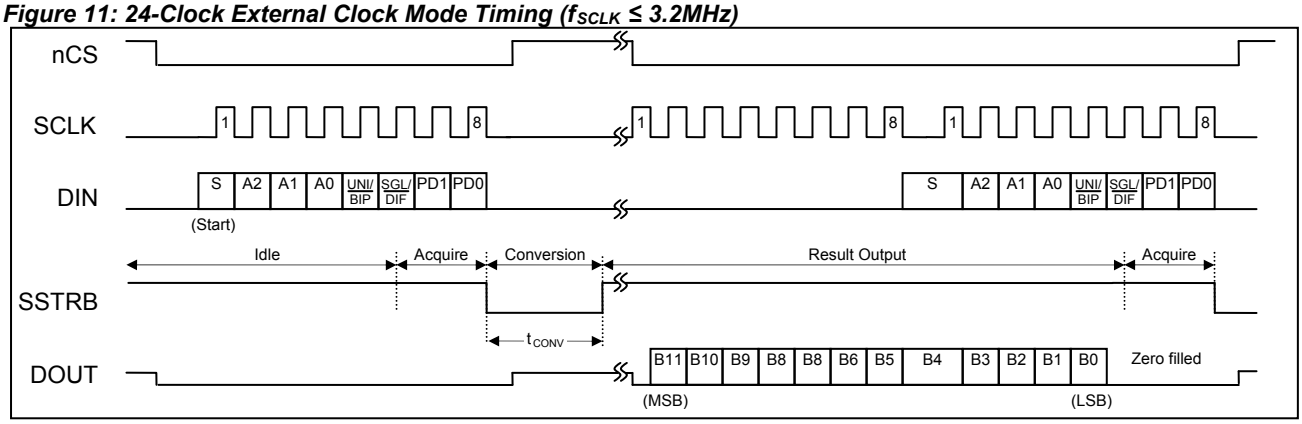

Figure 12: Internal Clock Mode Timing with interleaved Control Byte transmission

BIT	Name	Description
7 (MSB)	START	The Start Bit is defined by the first logic ‘1’ after nCS goes low.
6 5 4	A2 A1 A0	Channel Select Bits. Along with SGL/DIF these bits control the setting of the input multiplexer. For further details on the decoding see also Table 5 and Table 6.
3	UNI/BIP	Output Code Bit. The value of the bit determines conversion mode and output code format. ‘1’ = unipolar - straight binary coding ‘0’ = bipolar - two’s complement coding
2	SGL/DIF	Single-Ended / Differential Select Bit. Along with the Channel Select Bits A2 .. A0 this bit controls the setting of the input multiplexer ‘1’ = single ended - all channels CH0 … CH7 measured referenced to COM ‘0’ = differential - the voltage between two channels is measured
1 0 (LSB)	PD1 PD0	Power Down and Clock Mode Select Bits PD1 PD0 Mode 0 0 Full Power-Down 0 1 Fast Power-Down 1 0 Internal clock mode 1 1 External clock mode

Table 7 Control Byte Format

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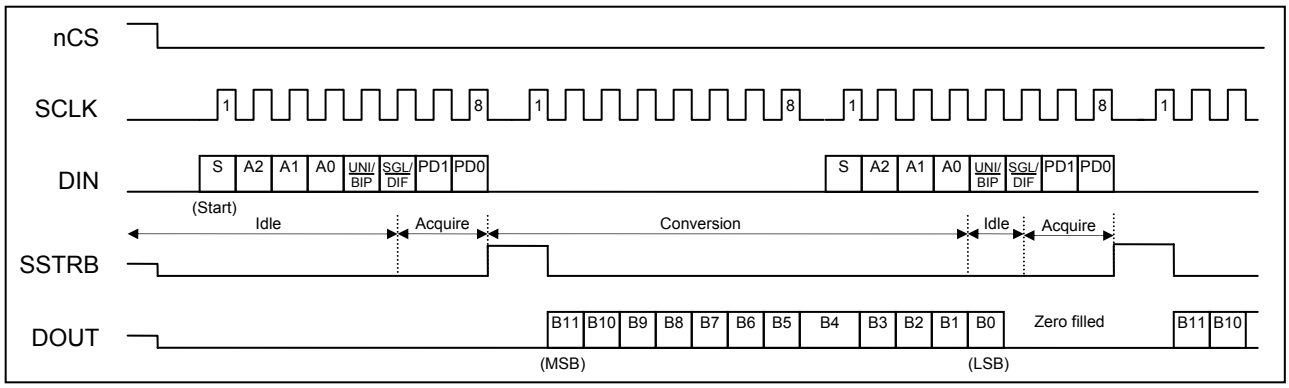

Figure 13: 16-Clock External Clock Mode Conversion

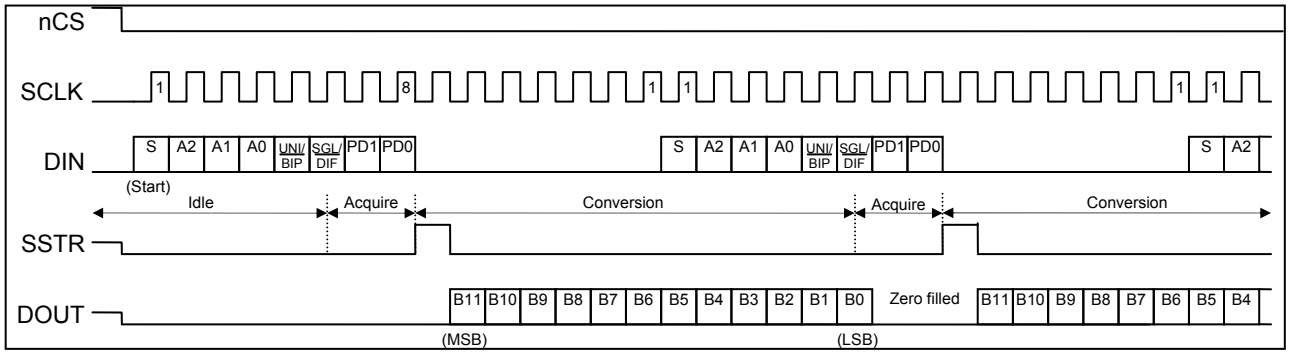

Figure 14: 15-Clock External Clock Mode Conversion

Internal Clock Mode

In Internal Clock Mode, the conversion starts at the falling clock edge of the eighth control bit just as in External Clock Mode. However, there are no further clock pulses required at SCLK to complete the conversion. The conversion clock is generated by an internal oscillator that runs at approximately 3.2MHz. While the conversion is running, the SSTRB signal is driven LOW. As soon as the conversion is complete, SSTRB is switched to HIGH, signalling that the conversion result can be read out on the serial interface. To shorten cycle times ZADCS12x2 family devices allow interleaving of the read out process with the transmission of a new control byte. Thus it is possible to read the conversion result and to start a new conversion with just two consecutive byte transfers, instead of thee bytes that would have to be send without the interleaving function. While the IC is performing a conversion in Internal Clock Mode, the Chip Select signal (nCS) may be tied HIGH allowing other devices to communicate on the bus. The output driver at DOUT is switched into a high impedance state while nCS is HIGH. The conversion time t_{CONV} may vary in the specified limits depending on the actual VDD and temperature values.

16-Clocks per Conversion

Interleaving of the data read out process and transmission of a new Control Byte is also supported for External Clock Mode operation. Figure 13 shows the transmission timing for conversion runs using 16 clock cycles per run.

15-Clocks per Conversion

ZADCS12x2 family devices do also support a 15 clock cycle conversion mode (see Figure 14). This is the fastest conversion mode possible. In fact, the specified converter sampling rate of 200ksps will be reached in this mode, provided the clock frequency is set to 3.2MHz. Usually micro controllers do not support this kind of 15 bit serial communication transfers. However, specifically designed digital state machines implemented in Field Programmable Gate Arrays (FPGA) or Application Specific Integrated Circuits (ASIC) may use this operation mode.

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Digital Timing

In general the clock frequency at SCLK may vary from 0.1MHz to 3.2MHz. Considering all telegram pauses or other interruptions of a continuous clock at SCLK, each conversion must be completed within 1.2ms from the falling clock edge of the eighth bit in the Control Byte. Otherwise the signal that was captured during sample/hold may drop to noticeable affect the conversion result. Further detailed timing information on the digital interface is provided in Table 8 and Figure 15.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCLK Periode	t_{SCLK}		303.0			ns
SCLK Pulse Width High	$t_{SCLKhigh}$		151.5			ns
SCLK Pulse Width Low	$t_{SCLKlow}$		151.5			ns
DIN to SCLK Setup	$t_{DinSetup}$		30			ns
DIN to SCLK Hold	$t_{DinHold}$		10			ns
nCS Fall to SCLK Setup	$t_{nCSSetup}$		30			ns
SCLK Fall to DOUT & SSTRB Hold	$t_{OutHold}$	C_{Load} = 20pF	10			ns
SCLK Fall to DOUT & SSTRB Valid	$t_{OutValid}$	C_{Load} = 20pF			40	ns
nCS Rise to DOUT & SSTRB Disable	$t_{OutDisable}$	C_{Load} = 20pF	10		60	ns
nCS Fall to DOUT & SSTRB Enable	$t_{OutEnable}$	C_{Load} = 20pF			60	ns
nCS Pulse Width High	$t_{nCSHigh}$		100			ns

Table 8: Timing Characterisitics (VDD = +2.7V to + 5.25V; $\theta_{OP} = \theta_{OPmin} \ldots \theta_{OPmax}$)

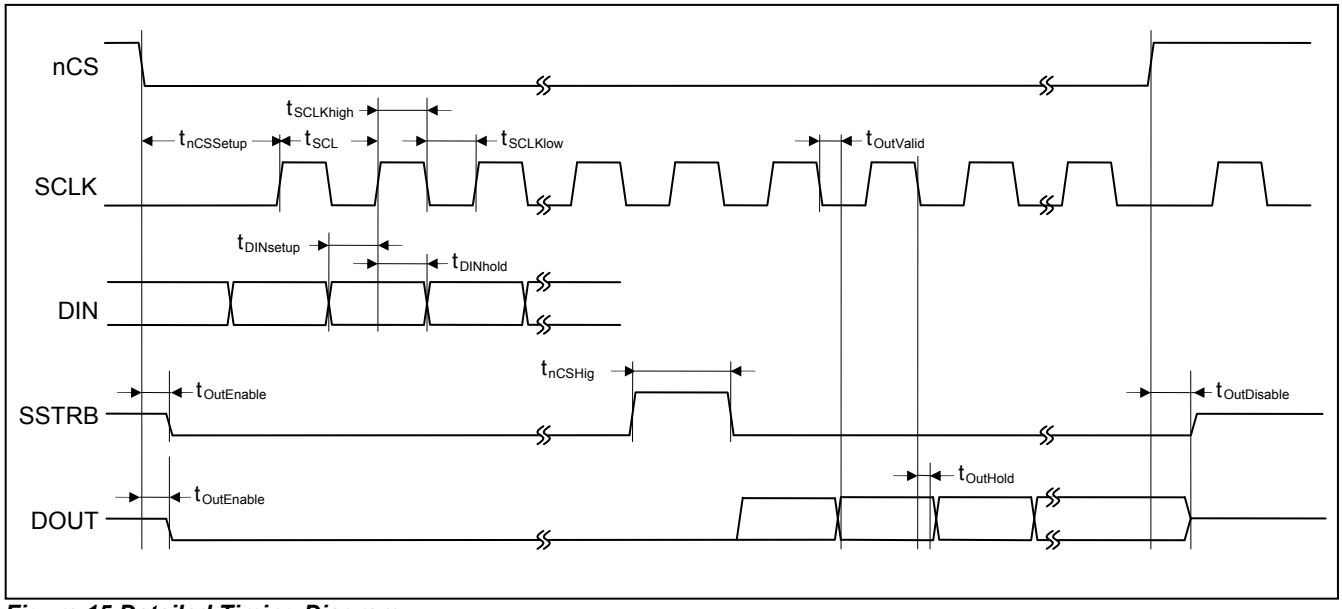

Figure 15 Detailed Timing Diagram

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Output Code Format

ZADCS12x2 family devices do all support unipolar and bipolar operation modes. The digital output code is straight binary in unipolar mode. It ranges from 0x00 for an input voltage difference of 0V to 0xFF for an input voltage difference of VREF (Full Scale = FS). The first code transition (0x00 → 0x01) occurs at a voltage equivalent to ½ LSB, the last (0xFE → 0xFF) at VREF-1.5 LSB. See also Figure 16 for details. In bipolar mode a two's complement coding is applied. Code transitions occur again halfway between successive integer LSB values. The transfer function is shown in Figure 17.

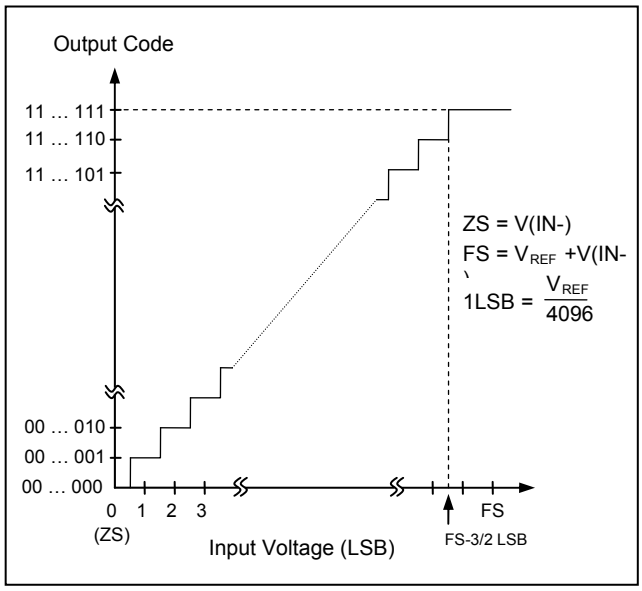

Figure 16: Unipolar Transfer Function

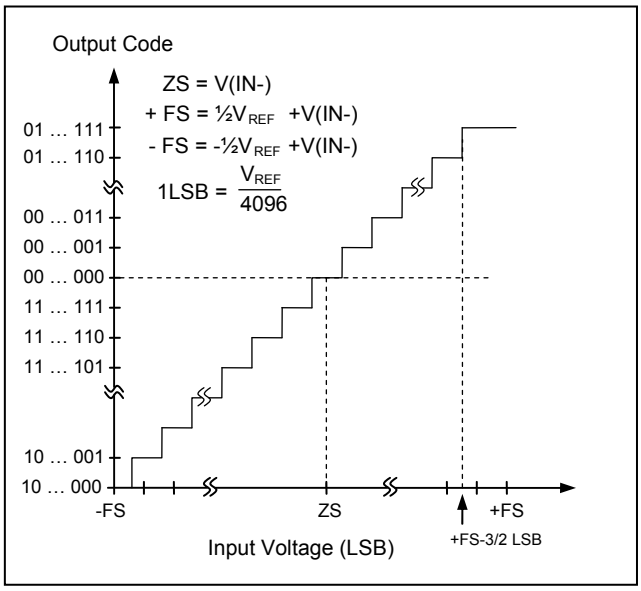

Figure 17: Bipolar Transfer Function

2.5. Power Dissipation

The ZADCS12x2 family offers three different ways to save operating current between conversions. Two different software controlled power down modes can be activated to automatically shut-down the device after completion of a conversion. They differ in the amount of circuitry that is powered down.

Software Power Down

Full Power Down Mode shuts down the entire analog part of the IC, reducing the static IDD of the device to less than 0.5µA if no external clock is provided at SCLK. Fast Power Down mode is only useful with ZADCS12x2V devices if the internal voltage reference is used. During Fast Power-Down the bandgap and the VREFADJ output buffer are kept alive while all other internal analog circuitry is shut down. The benefit of Fast Power Down mode is a shorter turn on time of the reference compared to Full Power-Down Mode. This is basically due to the fact that the low pass which is formed at the VREFADJ output by the internal 20kΩ resistor and the external buffer capacitor of 47nF is not discharged in Fast Power-Down Mode. The settling time of the low pass at VREFADJ is about 9ms to reach 12 bit accuracy. The Fast Power Down mode omits this settling and reduces the turn on time to about 200µs. To wake up the IC out of either software power down mode, it is sufficient to send a Start Bit while nCS is LOW. Since micro controllers can commonly transfer full bytes per transaction only, a dummy conversion is usually carried out to wake the device.

In all application cases where an external reference voltage is supplied (basic ZADCS12x2 and ZADCS12x2**V** with VREFADJ tied to VDD) there is no turn on time to be considered. The first conversion is already valid. Fast Power-Down and Full Power-Down Mode do not show any difference in this configuration.

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Hardware Power Down

The third power down mode is called Hardware Power-Down. It is initiated by pulling the nSHDN pin LOW. If this condition is true, the device will immediately shut down all circuitry just as in Full Power Down-Mode.
The IC wakes up if nSHDN is tied HIGH. There is no internal pull-up that would allow nSHDN to float during normal operation. This ensures the lowest possible power consumption in power down mode.

General Power Considerations

Even without activating any power down mode, the devices out of the ZADCS12x2 family reduce their power consumption between conversions automatically. The comparator, which contributes a considerable amount to the overall current consumption of the device, is shut off as soon as a conversion is ended. It gets turned on at the start of the next acquisition period. This explains the difference between the IDDstatic and IDDactive measurements shown in chapter 1.6 Typical Operating Characteristics.
The average current consumption of the device depends very much on the sampling frequency and the type of protocol used to communicate with the device.
In order to achieve the lowest power consumption at low sampling frequencies, it is suggested to keep the conversion clock frequency at the maximum level of 3.2MHz and to power down the device between consecutive conversions. Figure 18 shows the characteristic current consumption of the ZADCS12x2 family with external reference supply versus Sampling Rate

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3 Layout

To achieve optimum conversion performance care must be taken in design and layout of the application board. It is highly recommended to use printed circuit boards instead of wire wrap designs and to establish a single point star connection ground system towards AGND (see Figure 19).

For optimal noise performance the star point should be located very close to the AGND pin of the converter. The ground return to the power supply should be as short as possible and low impedance.

All other analog ground points of external circuitry that is related to the A/D converter as well as the DGND pin of the device should be connected to this ground point too. Any other digital ground system should be kept apart as far as possible and connect on the power supply point only.

Analog and digital signal domains should also be separated as well as possible and analog input signals should be shielded by AGND ground planes from electromagnetic interferences. Four-layer PCB boards that allow smaller vertical distances between the ground plane and the shielded signals do generally show a better performance than two-layer boards.

The sampling phase is the most critical portion of the overall conversion timing for signal distortion. If possible, the switching of any high power devices or nearby digital logic should be avoided during the sampling phase of the converter.

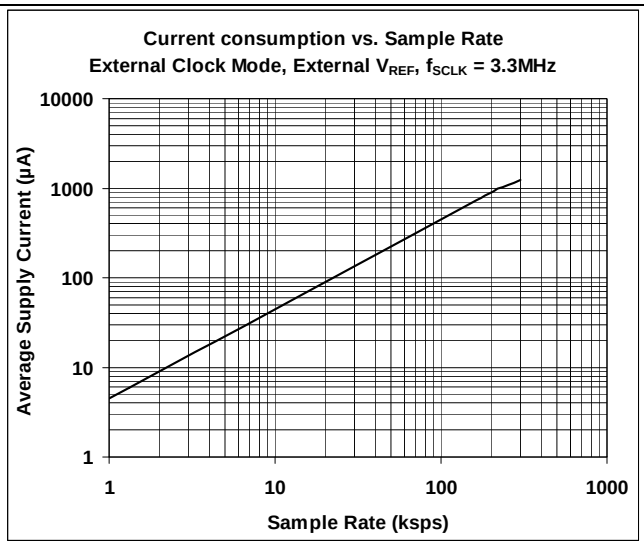

Figure 18: Supply Current versus Sampling Rate

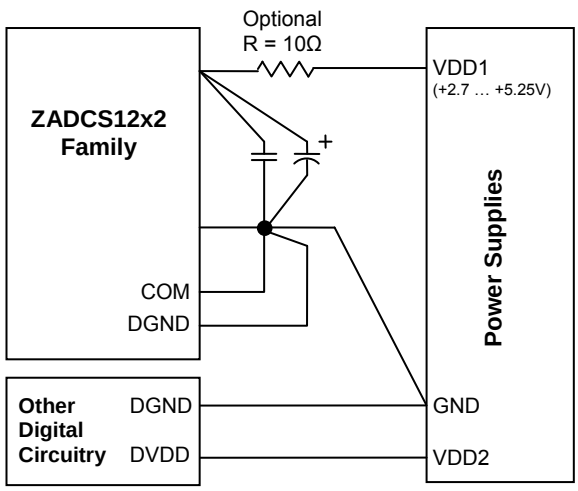

Figure 19: Optimal Power-Supply Grounding System

The fully differential internal architecture of the ZADCS12x2 family ensures very good suppression of power supply noise. Nevertheless, the SAR architecture is generally sensitive to glitches or sudden changes of the power supply that occur shortly before the latching of the comparator output. It is therefore recommended to bypass the power supply connection very close to the device with capacitors of 0.1µF (ceramic) and >1µF (electrolytic). In case of a noisy supply, an additional series resistor of 5 to 10 ohms can be used to low-pass filter the supply voltage. The reference voltage should always be bypassed with capacitors of 0.1µF (ceramic) and ≥ 4.7µF (electrolytic) as close as possible to the VREF pin. If V_{REF} is provided by an external source, any series resistance in the V_{REF} supply path can cause a gain error of the converter. During conversion, a DC current of about 100µA is drawn through the VREF pin that could cause a noticeable voltage drop across the resistance.

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4 Package Drawing

ZADCS1282 devices are delivered in a 20-pin SSOP-package that has the dimensions as shown in Figure 20 and Table 9. ZADCS1242 and ZADCS1222 devices apply respective 16-pin and 14-pin SSOP-packages. Their dimensions are specified in Table 9 and Table 10.

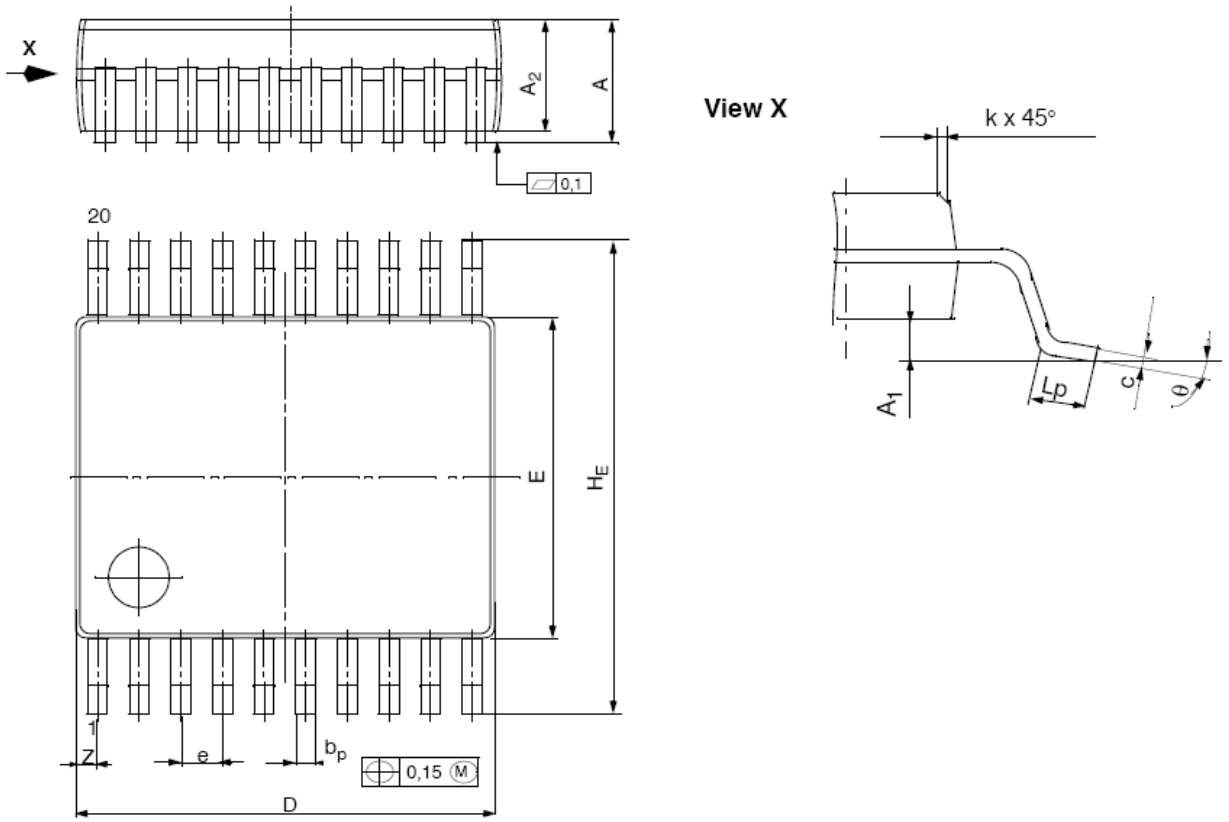

Figure 20: Package Outline Dimensions

Symbol	A	A_1	A_2	b_P	c	D	E	e_{nom}	H_E	L_P	Z	k	Θ
Nominal	1.86	0.13	1.73	0.30	0.15	7.20	5.30		7.80				4°
Maximum	1.99	0.21	1.78	0.38	0.20	7.33	5.38	0.65	7.90		0.74		8°
Minimum	1.73	0.05	1.68	0.25	0.09	7.07	5.20		7.65	0.63		0.25	0°

Table 9: Package Dimensions for ZADC1282 devices (mm)

Symbol	A	A_1	A_2	b_P	c	D	E	e_{nom}	H_E	L_P	Z	k	Θ
Nominal	1.86	0.13	1.73	0.30	0.15	6.20	5.30		7.80				4°
Maximum	1.99	0.21	1.78	0.38	0.20	6.07	5.38	0.65	7.90		0.89		10°
Minimum	1.73	0.05	1.68	0.25	0.09	6.33	5.20		7.65	0.63		0.25	0°

Table 10: Package Dimensions for ZADC1242 devices (mm)

Symbol	A	A_1	A_2	b_P	c	D	E	e_{nom}	H_E	L_P	Z	k	Θ
Nominal	1.86	0.13	1.73	0.30	0.15	6.20	5.30		7.80				4°
Maximum	1.99	0.21	1.78	0.38	0.20	6.33	5.38	0.65	7.90		1.22		10°
Minimum	1.73	0.05	1.68	0.25	0.09	6.07	5.20		7.65	0.63		0.25	0°

Table 11: Package Dimensions for ZADC1222 devices (mm)

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Sales and Further Information

www.zmdi.com adc@zmdi.com

Zentrum Mikroelektronik Dresden AG
Grenzstrasse 28
01109 Dresden
Germany

Phone +49 (0)351.8822.7232
Fax +49 (0)351.8822.87232

ZMD America, Inc.
8413 Excelsior Drive
Suite 200
Madison, WI 53717
USA

Phone +1 (608) 829-1987
Fax +1 (631) 549-2882

Zentrum Mikroelektronik Dresden AG, Japan Office
2nd Floor, Shinbashi Tokyu Bldg.
4-21-3, Shinbashi, Minato-ku
Tokyo, 105-0004
Japan

Phone +81.3.6895.7410
Fax +81.3.6895.7301

ZMD FAR EAST, Ltd.
3F, No. 51, Sec. 2,
Keelung Road
11052 Taipei
Taiwan

Phone +886 2 2377 8189
Fax +886 2 2377 8199

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