18-Channel Gamma Buffer with Regulator

ADD8709

FEATURES

Integrated voltage regulator
Upper/lower buffers swing to V_{DD}/GND
Single-supply operation: 7.5 V to 16.5 V
Continuous current drive: 15 mA
High peak output current: 150 mA
Low offset voltage: 15 mV max
Output voltage stable under transient load conditions

APPLICATIONS

TFT LCD monitor panels
TFT LCD TV panels

GENERAL DESCRIPTION

The ADD8709 is an 18-channel gamma reference for use in high-resolution TFT LCD monitor and TV panels. The output buffers feature low offset voltage and high current drive under transient load conditions to provide a more accurate and stable gamma curve. Two channels swing to V_{DD} and two channels swing to GND, increasing the overall range of the curve. An on-board voltage regulator is available for external applications. Here again, external component costs are reduced and the quality of the gray scale is increased.

The ADD8709 is specified over the temperature range of –40°C to +100°C and comes in a robust, low profile quad flat package.

FUNCTIONAL BLOCK DIAGRAM

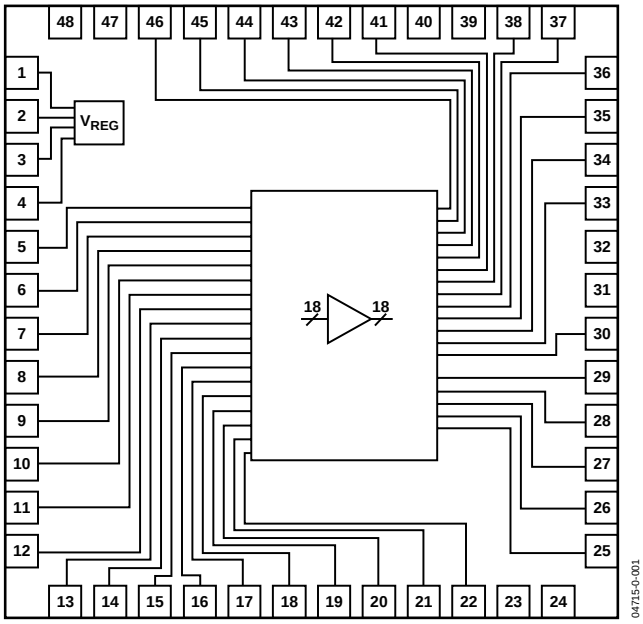

Figure 1. 48-Lead LQFP

Rev. 0
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REVISION HISTORY

7/04—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

7.5 V ≤ V_{DD} ≤ 16 V, T_A @ 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ALL DEVICES						
POWER SUPPLY						
Supply Voltage	V_S		7.5		16	V
Supply Current	I_{SYS}	No load		10.5	15	mA
		−20°C ≤ T_A ≤ +105°C			17	mA
VOLTAGE REGULATOR						
Dropout Voltage	ΔV_{DO}	I_L = 100 µA		100	150	mV
		I_L = 5 mA		310	350	mV
Line Regulation	REG_{LINE}	V_{IN} = 8.5 V to 16.5 V, V_{OUT} = 8 V		0.01	0.20	%/V
Load Regulation	REG_{LOAD}	I_O = 100 µA to 10 mA		0.02	0.10	%/mA
Load Current	I_O			5		mA
Thermal Regulation	$REG_{THERMAL}$			0.005		%/W
GAMMA BUFFERS						
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{DD} = 7 V to 17 V, −20°C ≤ T_A ≤ +105°C	68	90		dB
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			5	15	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−20°C ≤ T_A ≤ +105°C		20		µV/°C
Input Bias Current	I_B			0.5	1.1	µA
		−20°C ≤ T_A ≤ +105°C			1.5	µA
Input Voltage Range			0		V_{DD}	V
Input Impedance	Z_{IN}			400		kΩ
Input Capacitance	C_{IN}			1		pF
OUTPUT CHARACTERISTICS						
Output Performance (V1, V8, V9, V18)	ΔV_{OUT}[1]	I_L = 20 mA, V_{DD} = 16 V		15		mV
Output Performance (V2 to V7, V10 to V17)	ΔV_{OUT}[1]	I_L = 5 mA, V_{DD} = 16 V		5		mV
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 200 pF	4	6		V/µs
Bandwidth	BW	−3 dB, R_L = 10 kΩ, C_L = 200 pF		4.5		MHz
Settling Time to 0.1%	t_S	1 V, R_L = 10 kΩ, C_L = 200 pF		1.1		µs
Phase Margin	φo	R_L = 10 kΩ, C_L = 200 pF		55		Degrees

[1] ΔV_{OUT} is the shift from the desired output voltage under the specified current load.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_{DD})	18 V
Input Voltage	–0.5 V to V_{DD}
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range[1]	–40°C to +100°C
Junction Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
ESD Tolerance (HBM)	±2000 V
ESD Tolerance (MM)	±150 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Package Characteristics

Package Type	θ_{JA}	Unit
LQFP (ST)	74.57	°C/W

[1] See Application Notes section.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

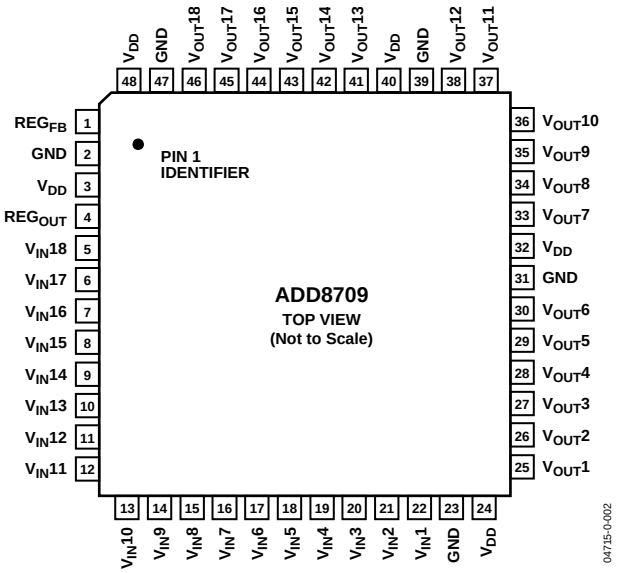

Figure 2. 48-Lead Low Profile Quad Flat Package (ST-48)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Name	Description
1	REG_{FB}	Regulator Feedback	Compares a percentage of the regulator output to the internal voltage reference. Internal resistors are used to program the desired regulator output voltage.
2	GND	Ground	Ground. Nominally 0 V.
3	V_{DD}	Supply	Supply voltage or source voltage. Nominally 16 V.
4	REG_{OUT}	Regulator Output	Provides a regulated output voltage for use as a reference for additional external gamma channels.
5	$V_{IN}18$	Input	Buffer input.
6	$V_{IN}17$		
7	$V_{IN}16$		
8	$V_{IN}15$		
9	$V_{IN}14$		
10	$V_{IN}13$		
11	$V_{IN}12$		
12	$V_{IN}11$		
13	$V_{IN}10$		
14	$V_{IN}9$		
15	$V_{IN}8$		
16	$V_{IN}7$		
17	$V_{IN}6$		
18	$V_{IN}5$		
19	$V_{IN}4$		
20	$V_{IN}3$		
21	$V_{IN}2$		
22	$V_{IN}1$		
23	GND	Ground	Ground. Nominally 0 V.
24	V_{DD}	Supply	Supply voltage. Nominally 16 V.
25	$V_{OUT}1$	Output	Buffer output. Designed to have higher sink than source capability.
26	$V_{OUT}2$		

Pin No.	Mnemonic	Name	Description
27	$V_{OUT}3$	Output	Buffer output.
28	$V_{OUT}4$		
29	$V_{OUT}5$		
30	$V_{OUT}6$		
31	GND	Ground	Ground. Nominally 0 V.
32	V_{DD}	Supply	Supply voltage. Nominally 16 V.
33	$V_{OUT}7$	Output	Buffer output.
34	$V_{OUT}8$		
35	$V_{OUT}9$		
36	$V_{OUT}10$		
37	$V_{OUT}11$		
38	$V_{OUT}12$		
39	GND	Ground	Ground. Nominally 0 V.
40	V_{DD}	Supply	Supply voltage. Nominally 16 V.
41	$V_{OUT}13$	Output	Buffer output.
42	$V_{OUT}14$		
43	$V_{OUT}15$		
44	$V_{OUT}16$		
45	$V_{OUT}17$	Output	Buffer output. Designed to have higher source than sink capability.
46	$V_{OUT}18$		
47	GND	Ground	Ground. Nominally 0 V.
48	V_{DD}	Supply	Supply voltage. Nominally 16 V.

TYPICAL APPLICATIONS CIRCUIT

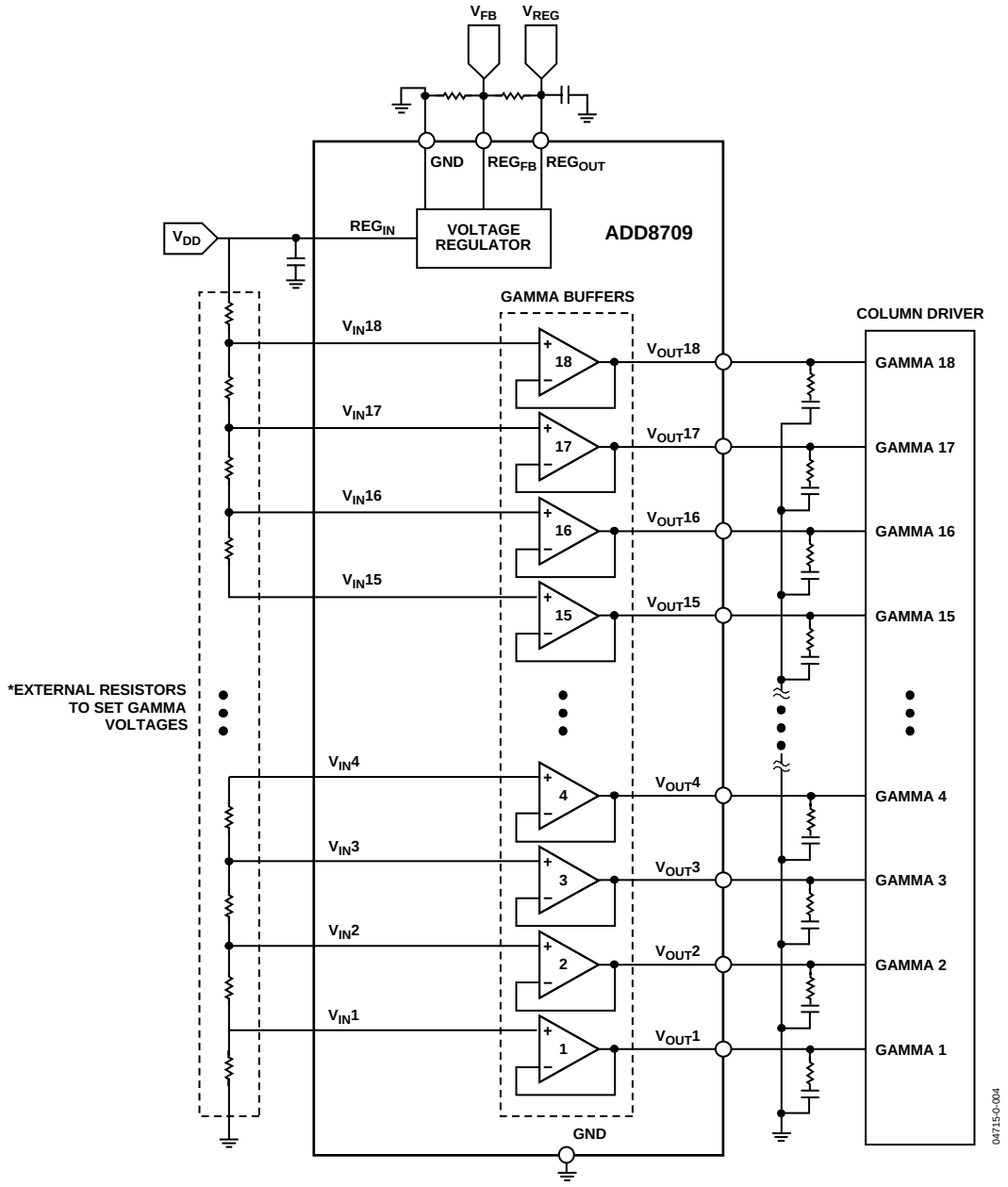

Figure 3.

TYPICAL PERFORMANCE CHARACTERISTICS

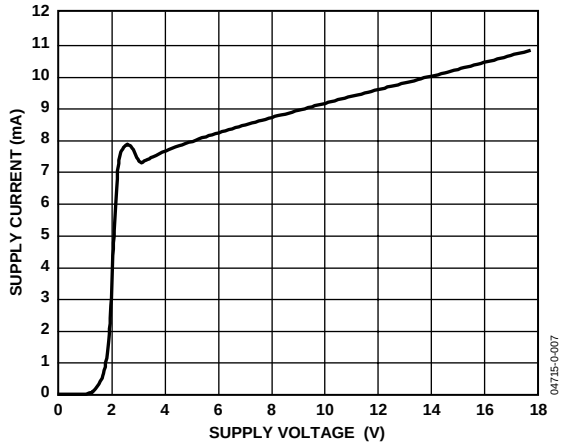

Figure 4. Supply Current vs. Supply Voltage

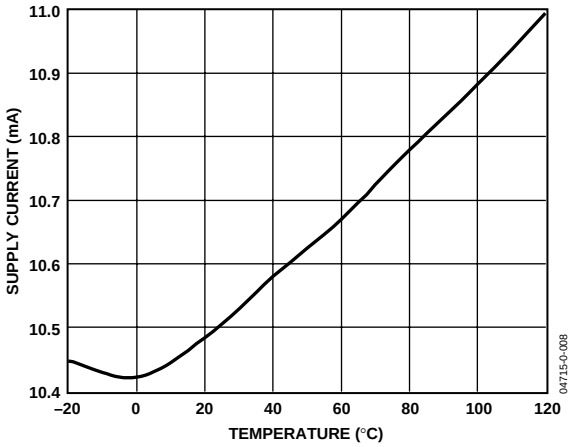

Figure 5. Supply Current vs. Temperature

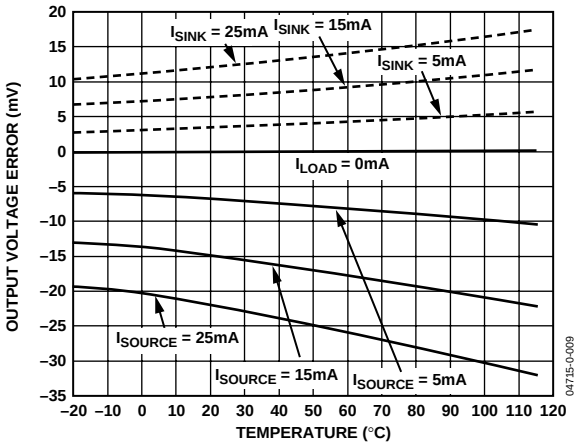

Figure 6. Output Voltage Error vs. Temperature

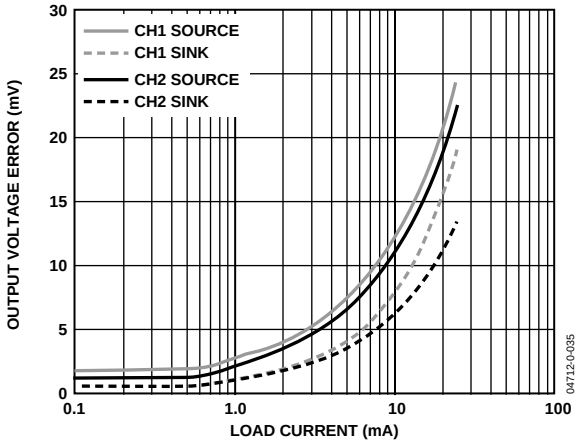

Figure 7. Output Voltage Error vs. Load Current

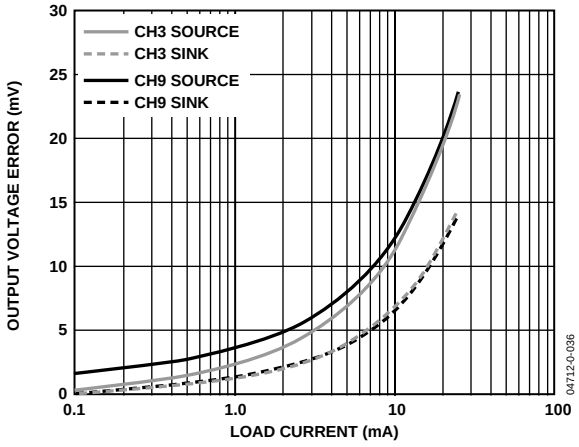

Figure 8. Output Voltage Error vs. Load Current

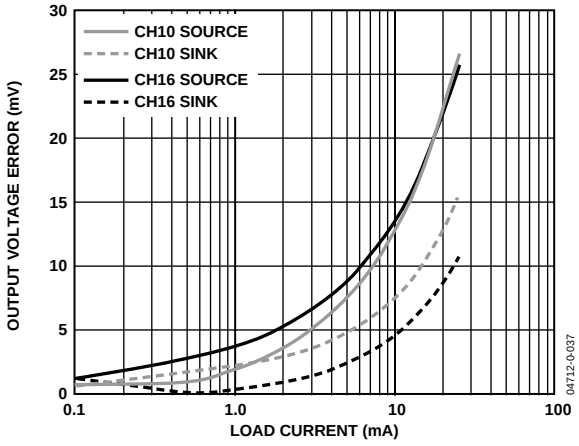

Figure 9. Output Voltage Error vs. Load Current

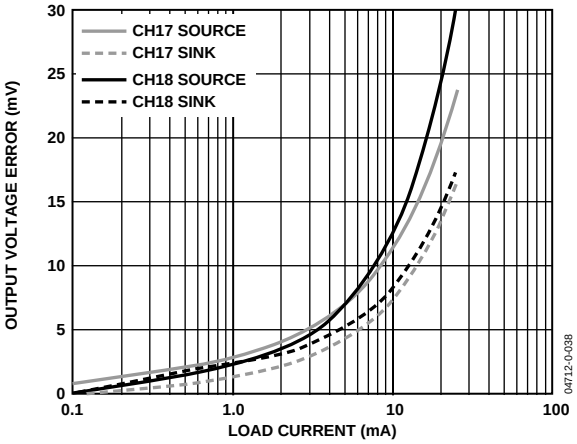

Figure 10. Output Voltage Error vs. Load Current

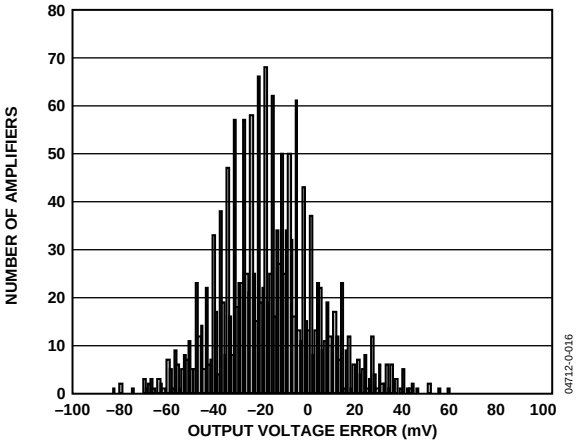

Figure 13. Output Voltage Error/Gamma 10 to 16

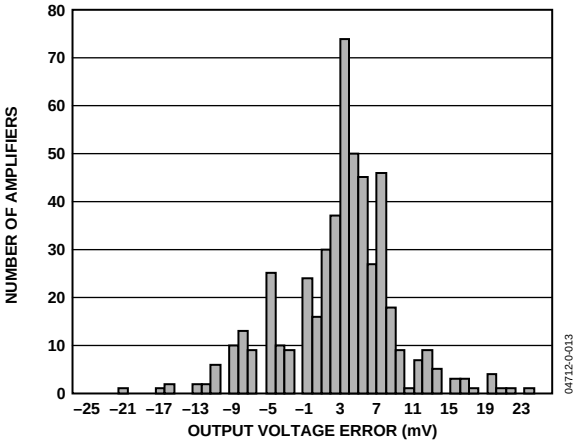

Figure 11. Output Voltage Error/Gamma 1 and 2

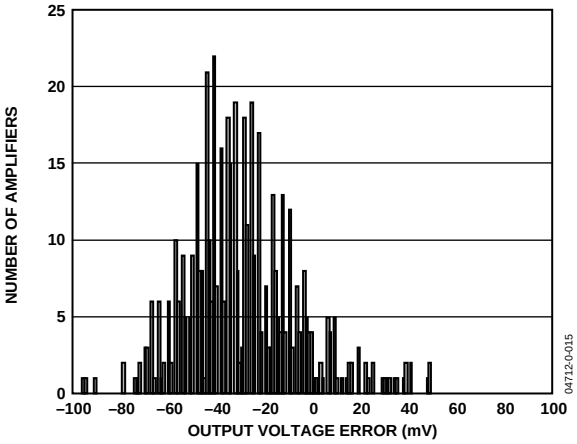

Figure 14. Output Voltage Error/Gamma 17 and 18

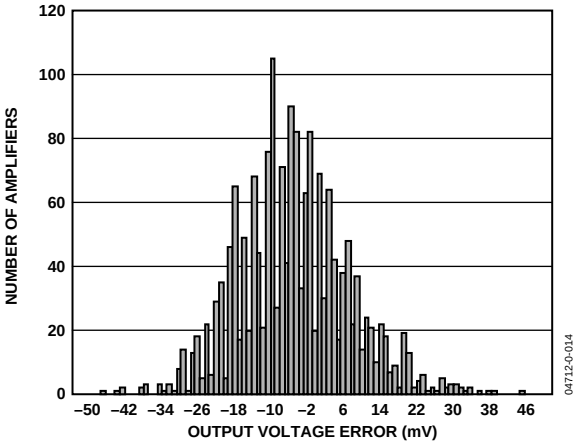

Figure 12. Output Voltage Error/Gamma 3 to 9

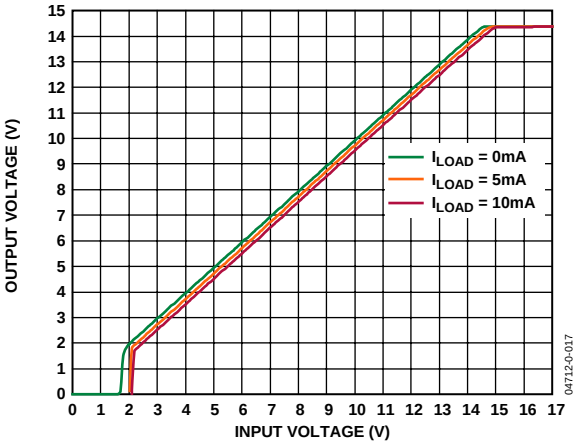

Figure 15. Dropout Characteristics

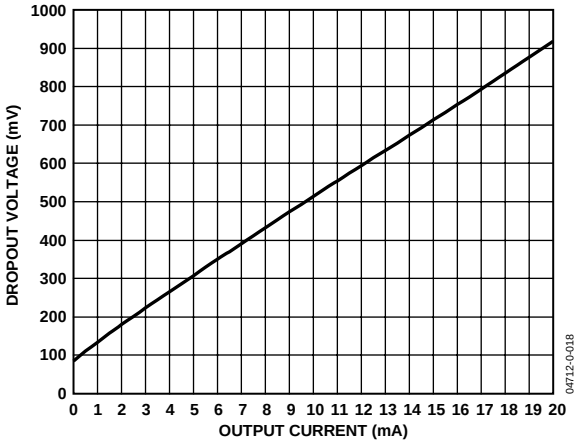

Figure 16. Dropout Voltage vs. Output Current

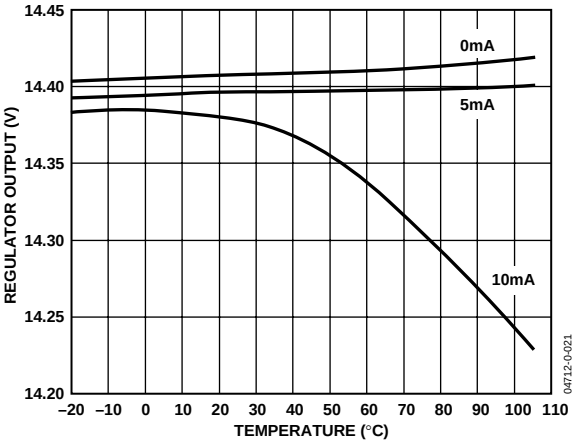

Figure 19. Regulator Output vs. Temperature

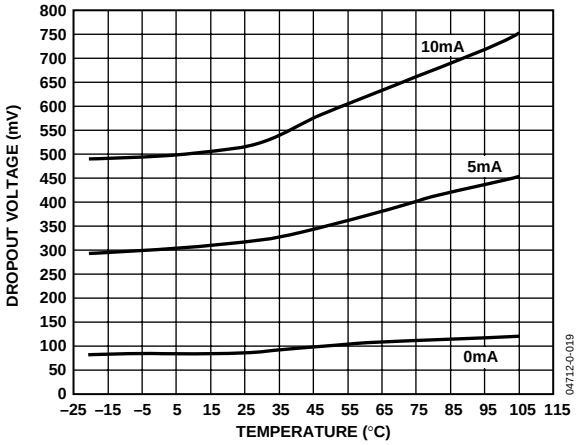

Figure 17. Dropout Voltage vs. Temperature

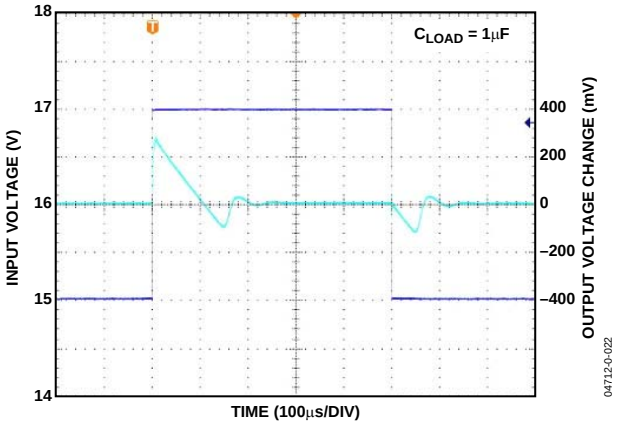

Figure 20. Regulator Line Transient Response

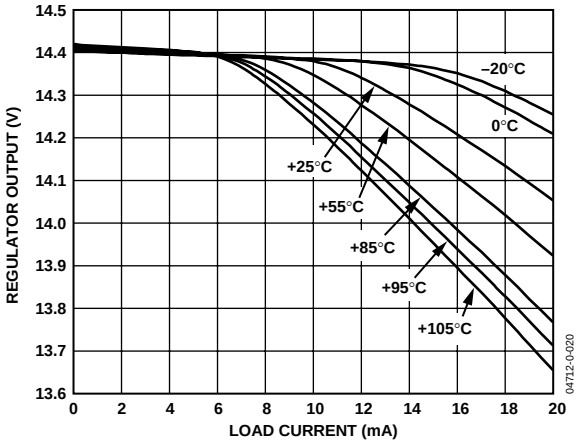

Figure 18. Regulator Output vs. I_{LOAD} Over Temperature

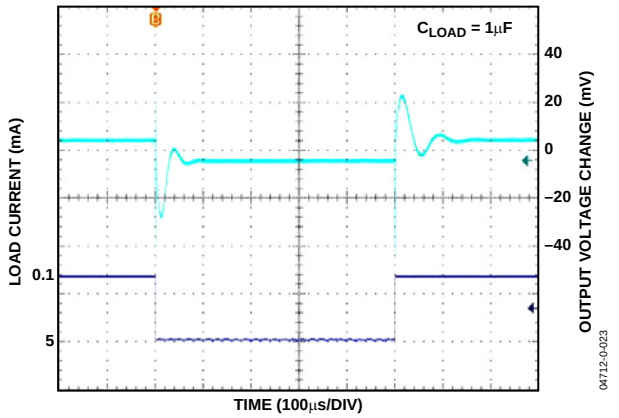

Figure 21. Regulator Load Transient Response

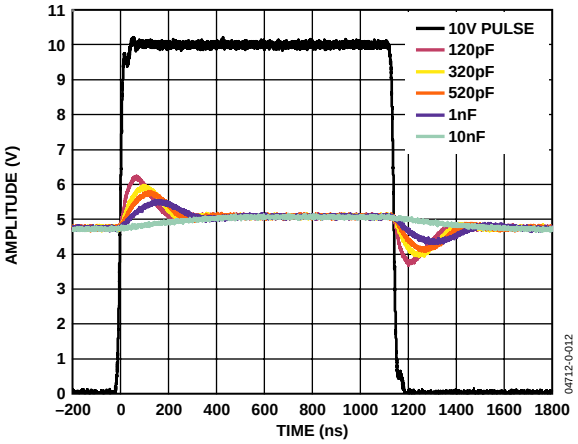

Figure 22. Transient Load Response vs. Capacitive Loading

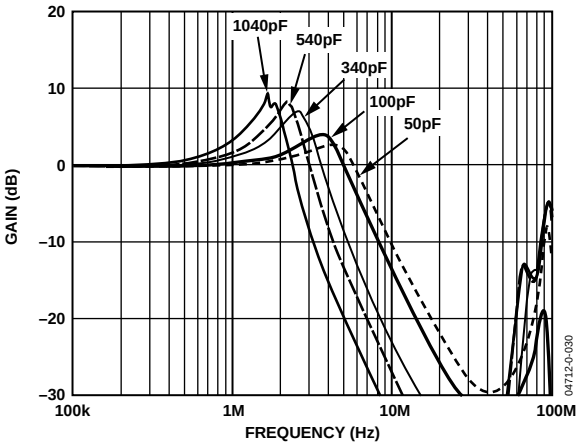

Figure 23. Frequency Response vs. Capacitive Loading

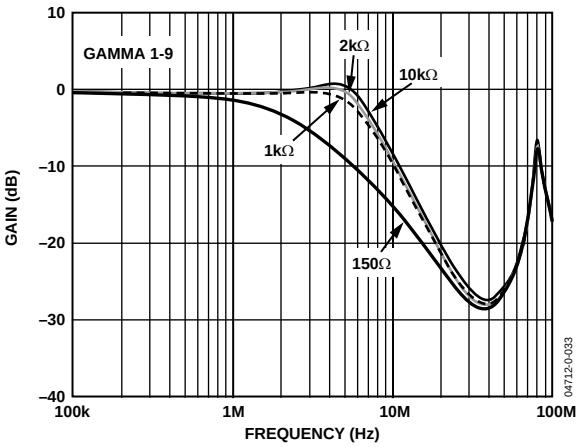

Figure 24. Frequency Response vs. Resistive Loading

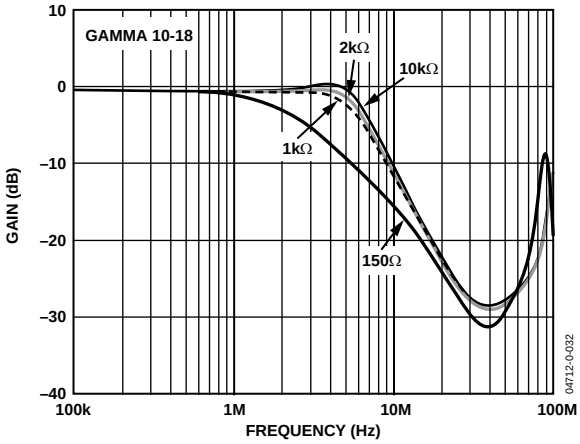

Figure 25. Frequency Response vs. Resistive Loading

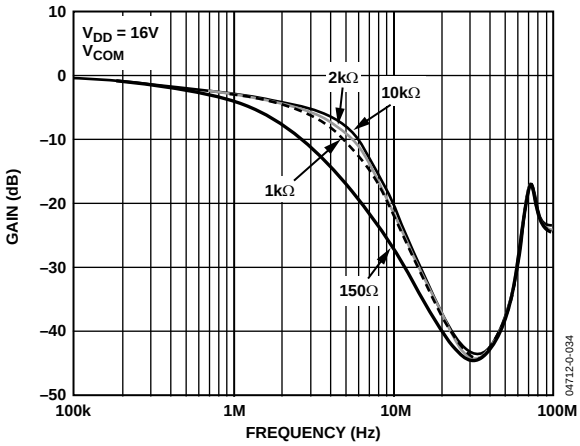

Figure 26. Frequency Response vs. Resistive Loading

APPLICATION NOTES

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADD8709 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADD8709. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing failure.

OPERATING TEMPERATURE RANGE

The maximum junction temperature is as follows:

$$T_J = T_{AMB\,MAX} + \theta_{JA} \times W_{MAX}$$

where:
$T_{AMB\,MAX}$ = maximum ambient temperature specified on the data sheet.
θ_{JA} = junction-to-ambient thermal resistance, in °C/watt.
W_{MAX} = maximum power dissipated in the device, in watts.

For the ADD8709, W_{MAX} can be calculated with the following equation:

$$W_{MAX} = V_{DD} \times I_{SYS} + V_{OUT} \times I_{OUT} + V_{DO} \times I_O$$

where:
$V_{DD} \times I_{SYS}$ = nominal system power requirements
$V_{OUT} \times I_{OUT}$ = amplifier load power dissipation
$V_{DO} \times I_O$ = regulator load power dissipation

Example 1

The estimated power consumption of the ADD8709 in extreme cases is as follows:

$V_{DD} \times I_{SYS} = 15\ V \times 15\ mA$
$V_{OUT} \times I_{OUT} = (8\ V \times 5\ mA/channel) \times 18\ channels$
$V_{DO} \times I_O = 0.6\ V \times 5\ mA$
$W_{MAX} = (15\ V \times 15\ mA) + (8\ V \times 5\ mA/channel \times 18\ channel) + (0.6\ V \times 5\ mA) = 0.948\ W$

$\theta_{JA} = 74.57°C/W$, $T_{AMB\,MAX} = 45°C$

$T_J = 45°C + (74.57°C/W) \times (0.948\ W) = 115.7°C$

Here, 150°C is the maximum junction temperature that is guaranteed before the part breaks down, while 125°C is the maximum process limit. Because T_J is < 150°C and < 125°C, this example demonstrates a condition where the part should perform within process limits.

OUTLINE DIMENSIONS

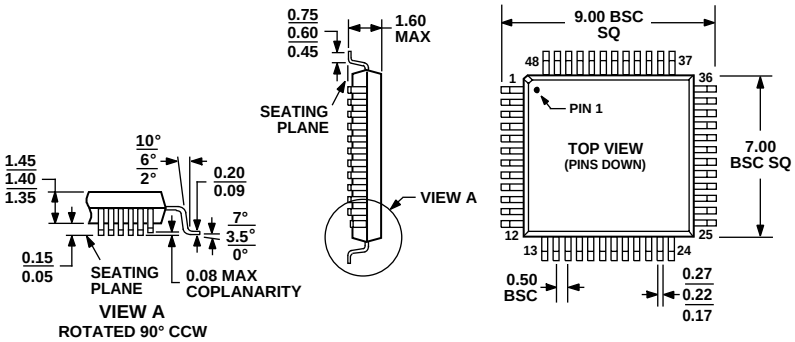

Figure 27. 48-Lead Low Profile Quad Flat Package
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADD8709ASTZ-REEL[2]	–40°C to +100°C	48-Lead Low Profile Quad Flat Package	ST-48
ADD8709ASTZ-REEL7[2]	–40°C to +100°C	48-Lead Low Profile Quad Flat Package	ST-48

[1] Available in reels only.
[2] Z = Pb-free part.

NOTES

NOTES

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