

## DIFFERENTIAL OUTPUT SILICON OSCILLATOR

### Features

- Quartz-free, MEMS-free, and PLL-free all-silicon oscillator
- Any output frequencies from 0.9 to 200 MHz
- Short lead times
- Excellent temperature stability ( $\pm 20$  ppm)
- Highly reliable startup and operation
- High immunity to shock and vibration
- Low jitter:  $< 1.5$  ps rms
- 0 to 85 °C operation includes 10-year aging in hot environments
- Footprint compatible with industry-standard 3.2 x 5.0 mm XOs
- CMOS, SSTL, LVPECL, LVDS, and HCSL versions available
- Driver stopped, tri-state, or powerdown operation
- RoHS compliant
- 1.8, 2.5, or 3.3 V options
- Low power
- More than 10x better fit rate than competing crystal solutions



### Specifications

| Parameters            | Condition                                           | Min  | Typ      | Max       | Units |
|-----------------------|-----------------------------------------------------|------|----------|-----------|-------|
| Frequency Range       |                                                     | 0.9  | —        | 200       | MHz   |
| Frequency Stability   | Temperature stability, 0 to +70 °C                  | —    | $\pm 10$ | —         | ppm   |
|                       | Temperature stability, 0 to +85 °C                  | —    | $\pm 20$ | —         | ppm   |
|                       | Total stability, 0 to +70 °C operation <sup>1</sup> | —    | —        | $\pm 150$ | ppm   |
|                       | Total stability, 0 to +85 °C operation <sup>2</sup> | —    | —        | $\pm 250$ | ppm   |
| Operating Temperature | Commercial                                          | 0    | —        | 70        | °C    |
|                       | Extended commercial                                 | 0    | —        | 85        | °C    |
| Storage Temperature   |                                                     | -55  | —        | +125      | °C    |
| Supply Voltage        | 1.8 V option                                        | 1.71 | —        | 1.98      | V     |
|                       | 2.5 V option                                        | 2.25 | —        | 2.75      | V     |
|                       | 3.3 V option                                        | 2.97 | —        | 3.63      | V     |

#### Notes:

1. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, first-year aging at 25 °C, shock, vibration, and one solder reflow.
2. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, ten-year aging at 85 °C, shock, vibration, and one solder reflow.
3. See "AN409: Output Termination Options for the Si500S and Si500D Silicon Oscillators" for further details regarding output clock termination recommendations.
4.  $V_{TT} = .5 \times V_{DD}$ .
5.  $V_{TT} = .45 \times V_{DD}$ .

| Parameters                                                                         | Condition                                                      | Min                          | Typ  | Max                          | Units    |
|------------------------------------------------------------------------------------|----------------------------------------------------------------|------------------------------|------|------------------------------|----------|
| Supply Current                                                                     | LVPECL                                                         | —                            | 34.0 | 36.0                         | mA       |
|                                                                                    | Low Power LVPECL                                               | —                            | 19.3 | 22.2                         | mA       |
|                                                                                    | LVDS                                                           | —                            | 14.9 | 16.5                         | mA       |
|                                                                                    | HCSL                                                           | —                            | 25.3 | 29.3                         | mA       |
|                                                                                    | Differential CMOS(3.3 V option, 10 pF on each output, 200 MHz) | —                            | 33   | 36                           | mA       |
|                                                                                    | Differential CMOS(3.3 V option, 1 pF on each output, 40 MHz)   | —                            | 16   | —                            | mA       |
|                                                                                    | Differential SSTL-3.3                                          | —                            | 24.5 | 27.7                         | mA       |
|                                                                                    | Differential SSTL-2.5                                          | —                            | 24.3 | 26.7                         | mA       |
|                                                                                    | Differential SSTL-1.8                                          | —                            | 22.2 | 25                           | mA       |
|                                                                                    | Tri-State                                                      | —                            | 9.7  | 10.7                         | mA       |
|                                                                                    | Powerdown                                                      | —                            | 1.0  | 1.9                          | mA       |
| Output Symmetry                                                                    | $V_{DIFF} = 0$                                                 | $46 - 13 \text{ ns}/T_{CLK}$ | —    | $54 + 13 \text{ ns}/T_{CLK}$ | %        |
| Rise and Fall Times (20/80%) <sup>3</sup>                                          | LVPECL/LVDS                                                    | —                            | —    | 460                          | ps       |
|                                                                                    | HCSL/Differential SSTL                                         | —                            | —    | 800                          | ps       |
|                                                                                    | Differential CMOS, 15 pF, ≥80 MHz                              | —                            | 1.1  | 1.6                          | ns       |
| LVPECL Output Option (DC coupling, 50 Ω to $V_{DD} - 2.0 \text{ V}$ ) <sup>3</sup> | Mid-level                                                      | $V_{DD} - 1.5$               | —    | $V_{DD} - 1.34$              | V        |
|                                                                                    | Diff swing                                                     | .720                         | —    | .880                         | $V_{PK}$ |
| Low Power LVPECL Output Option (AC coupling, 100 Ω Differential Load) <sup>3</sup> | Mid-level                                                      | —                            | N/A  | —                            | V        |
|                                                                                    | Diff swing                                                     | .68                          | —    | .95                          | $V_{PK}$ |
| LVDS Output Option (2.5/3.3 V) ( $R_{TERM} = 100 \Omega$ diff) <sup>3</sup>        | Mid-level                                                      | 1.15                         | —    | 1.26                         | V        |
|                                                                                    | Diff swing                                                     | 0.25                         | —    | 0.45                         | $V_{PK}$ |
| LVDS Output Option (1.8 V) ( $R_{TERM} = 100 \Omega$ diff) <sup>3</sup>            | Mid-level                                                      | 0.85                         | —    | 0.96                         | V        |
|                                                                                    | Diff swing                                                     | 0.25                         | —    | 0.45                         | $V_{PK}$ |
| HCSL Output Option <sup>3</sup>                                                    | Mid-level                                                      | 0.35                         | —    | 0.425                        | V        |
|                                                                                    | Diff swing                                                     | 0.65                         | —    | 0.82                         | $V_{PK}$ |
|                                                                                    | DC termination per pad                                         | 45                           | —    | 55                           | Ω        |
| CMOS Output Voltage <sup>3</sup>                                                   | $V_{OH}$ , sourcing 9 mA                                       | $V_{DD} - 0.6$               | —    | —                            | V        |
|                                                                                    | $V_{OL}$ , sinking 9 mA                                        | —                            | —    | 0.6                          | V        |
| SSTL-1.8 Output Voltage <sup>4</sup>                                               | $V_{OH}$                                                       | $V_{TT} + 0.375$             | —    | —                            | V        |
|                                                                                    | $V_{OL}$                                                       | —                            | —    | $V_{TT} - 0.375$             |          |
| SSTL-2.5 Output Voltage <sup>4</sup>                                               | $V_{OH}$                                                       | $V_{TT} + 0.48$              | —    | —                            | V        |
|                                                                                    | $V_{OL}$                                                       | —                            | —    | $V_{TT} - 0.48$              |          |
| SSTL-3.3 Output Voltage <sup>5</sup>                                               | $V_{OH}$                                                       | $V_{TT} + 0.48$              | —    | —                            | V        |
|                                                                                    | $V_{OL}$                                                       | —                            | —    | $V_{TT} - 0.48$              |          |
| Powerup Time                                                                       | From time $V_{DD}$ crosses min spec supply                     | —                            | —    | 2                            | ms       |
| OE Deassertion to Clk Stop                                                         |                                                                | —                            | —    | $250 + 3 \times T_{CLK}$     | ns       |
| Return from Output Driver Stopped Mode                                             |                                                                | —                            | —    | $250 + 3 \times T_{CLK}$     | ns       |
| Return From Tri-State Time                                                         |                                                                | —                            | —    | $12 + 3 \times T_{CLK}$      | μs       |

## Notes:

1. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, first-year aging at 25 °C, shock, vibration, and one solder reflow.
2. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, ten-year aging at 85 °C, shock, vibration, and one solder reflow.
3. See "AN409: Output Termination Options for the Si500S and Si500D Silicon Oscillators" for further details regarding output clock termination recommendations.
4.  $V_{TT} = .5 \times V_{DD}$ .
5.  $V_{TT} = .45 \times V_{DD}$ .

| Parameters                 | Condition                                                    | Min | Typ | Max | Units     |
|----------------------------|--------------------------------------------------------------|-----|-----|-----|-----------|
| Return From Powerdown Time |                                                              | —   | —   | 2   | ms        |
| Period Jitter (1-sigma)    | Non-CMOS                                                     | —   | 1   | 2   | ps<br>RMS |
|                            | CMOS, $C_L = 7$ pF                                           | —   | 1   | 3   | ps<br>RMS |
| Integrated Phase Jitter    | 1.0 MHz – min(20 MHz,<br>$0.4 \times F_{OUT}$ ), non-CMOS    | —   | 0.6 | 1   | ps<br>RMS |
|                            | 1.0 MHz – min(20 MHz,<br>$0.4 \times F_{OUT}$ ), CMOS format | —   | 0.7 | 1.5 | ps<br>RMS |

**Notes:**

1. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, first-year aging at 25 °C, shock, vibration, and one solder reflow.
2. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, ten-year aging at 85 °C, shock, vibration, and one solder reflow.
3. See “AN409: Output Termination Options for the Si500S and Si500D Silicon Oscillators” for further details regarding output clock termination recommendations.
4.  $V_{TT} = .5 \times V_{DD}$ .
5.  $V_{TT} = .45 \times V_{DD}$ .

## Package Specifications

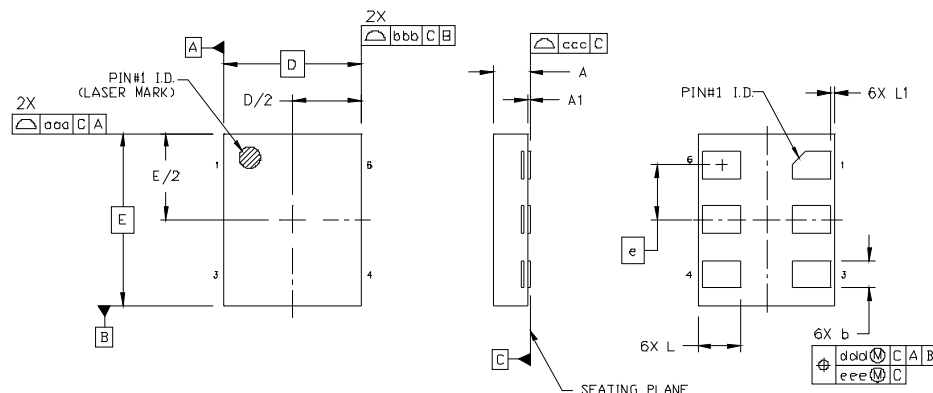


**Table 1. Package Diagram Dimensions (mm)**

| Dimension | Min       | Nom  | Max  |
|-----------|-----------|------|------|
| A         | 0.80      | 0.85 | 0.90 |
| A1        | 0.00      | 0.03 | 0.05 |
| b         | 0.59      | 0.64 | 0.69 |
| D         | 3.20 BSC. |      |      |
| e         | 1.27 BSC. |      |      |
| E         | 4.00 BSC. |      |      |
| L         | 0.95      | 1.00 | 1.05 |

| Dimension | Min  | Nom  | Max  |
|-----------|------|------|------|
| L1        | 0.00 | 0.05 | 0.10 |
| aaa       | —    | —    | 0.10 |
| bbb       | —    | —    | 0.10 |
| ccc       | —    | —    | 0.08 |
| ddd       | —    | —    | 0.10 |
| eee       | —    | —    | 0.05 |

**Table 2. Pad Connections**

|   |                                            |
|---|--------------------------------------------|
| 1 | OE                                         |
| 2 | NC—Make no external connection to this pin |
| 3 | GND                                        |
| 4 | Output                                     |
| 5 | Complementary Output                       |
| 6 | VDD                                        |

**Table 3. Tri-State/Powerdown/Driver Stopped Function on OE (3rd Option Code)**

|         | A         | B         | C          | D          | E              | F              |
|---------|-----------|-----------|------------|------------|----------------|----------------|
| Open    | Active    | Active    | Active     | Active     | Active         | Active         |
| 1 Level | Active    | Tri-State | Active     | Power-down | Active         | Driver Stopped |
| 0 Level | Tri-State | Active    | Power-down | Active     | Driver Stopped | Active         |

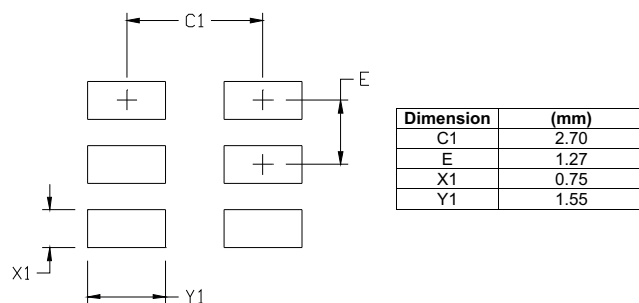
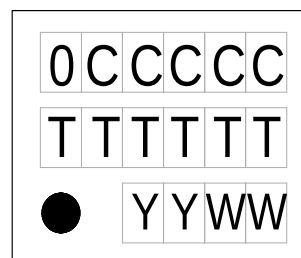


**Figure 1. Recommended Land Pattern**



0 = Si500  
 CCCCC = mark code  
 TTTTTT = assembly manufacturing code  
 YY = year  
 WW = work week

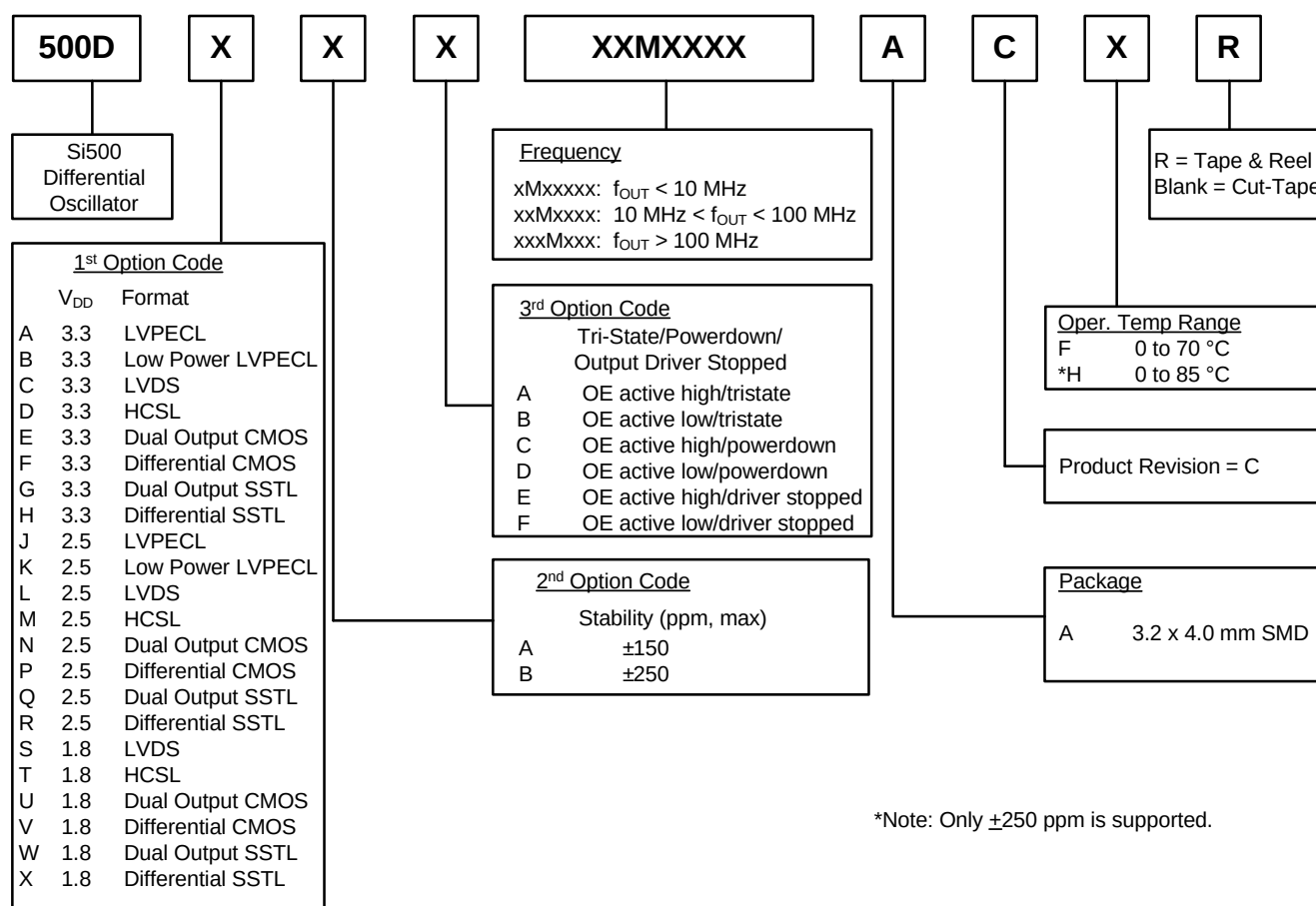
**Figure 2. Top Mark**

## Environmental Compliance

| Parameter                    | Conditions/Test Method            |
|------------------------------|-----------------------------------|
| Mechanical Shock             | MIL-STD-883, Method 2002.4        |
| Mechanical Vibration         | MIL-STD-883, Method 2007.3 A      |
| Resistance to Soldering Heat | MIL-STD-202, 260 C° for 8 seconds |
| Solderability                | MIL-STD-883, Method 2003.8        |
| Damp Heat                    | IEC 68-2-3                        |
| Moisture Sensitivity Level   | J-STD-020, MSL 3                  |

## Ordering Information

The Si500D supports a variety of options including frequency, output format, supply voltage, and tri-state/powerdown. Specific device configurations are programmed into the Si500D at time of shipment. Configurations are specified using the figure below. Silicon Labs provides a web-based part number utility that can be used to simplify part number configuration. Refer to [www.silabs.com/SiliconXOPartnumber](http://www.silabs.com/SiliconXOPartnumber) to access this tool. The Si500D XO series is supplied in a ROHS-compliant, Pb-free, 6-pad, 3.2 x 4.0 mm package. Tape and reel packaging is available as an ordering option.



## DOCUMENT CHANGE LIST

### Revision 0.2 to Revision 0.3

- Revision B to Revision C updated in Ordering Information
- 0 to 85 °C Operating Temperature Range option added

### Revision 0.3 to Revision 1.0

- Clarified SSTL specifications.
- Revised Differential CMOS supply current values.
- Clarified Differential CMOS supply current loading conditions.

### Revision 1.0 to Revision 1.1

- Updated Ordering information for  $\pm 250$  ppm from 0 to +85 °C.
- Updated jitter from 1.5 ps to 1.5 ps rms.
- Updated operating temperature to include extended commercial at 0 to +85 °C.
- Updated features to include LVPECL, LVDS, and HCSL.

**NOTES:**



## ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

[www.silabs.com/CBPro](http://www.silabs.com/CBPro)



**Timing Portfolio**  
[www.silabs.com/timing](http://www.silabs.com/timing)



**SW/HW**  
[www.silabs.com/CBPro](http://www.silabs.com/CBPro)



**Quality**  
[www.silabs.com/quality](http://www.silabs.com/quality)



**Support and Community**  
[community.silabs.com](http://community.silabs.com)

### Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

### Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOmodem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
USA

<http://www.silabs.com>