NEC
NEC Electronics Inc.

μPC4064
QUAD J-FET INPUT LOW-POWER OPERATIONAL AMPLIFIER

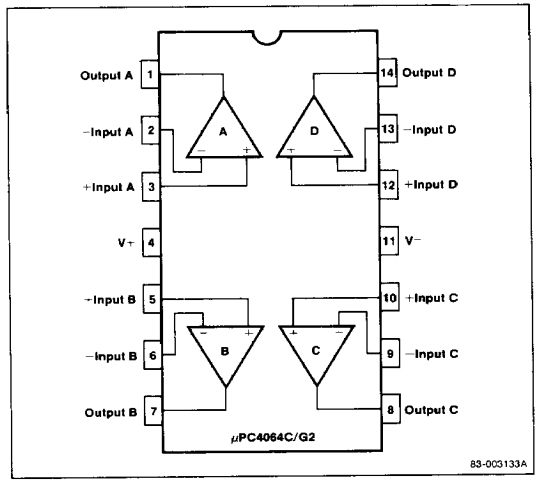
Description

The μPC4064 is a low power J-FET input quad operational amplifier that will operate at voltage levels as low as ±2.0 V. Input current is typically less than 1 mA. With input bias and offset currents as low as a few pA, the μPC4064 is an excellent choice for hand-held measurement equipment.

Features

- ☐ Low supply current
- ☐ Very low input bias and offset currents
- ☐ High slew rate
- ☐ High input impedance
- ☐ Output short circuit protection
- ☐ Internal frequency compensation
- ☐ TL064 direct replacement

Pin Configuration

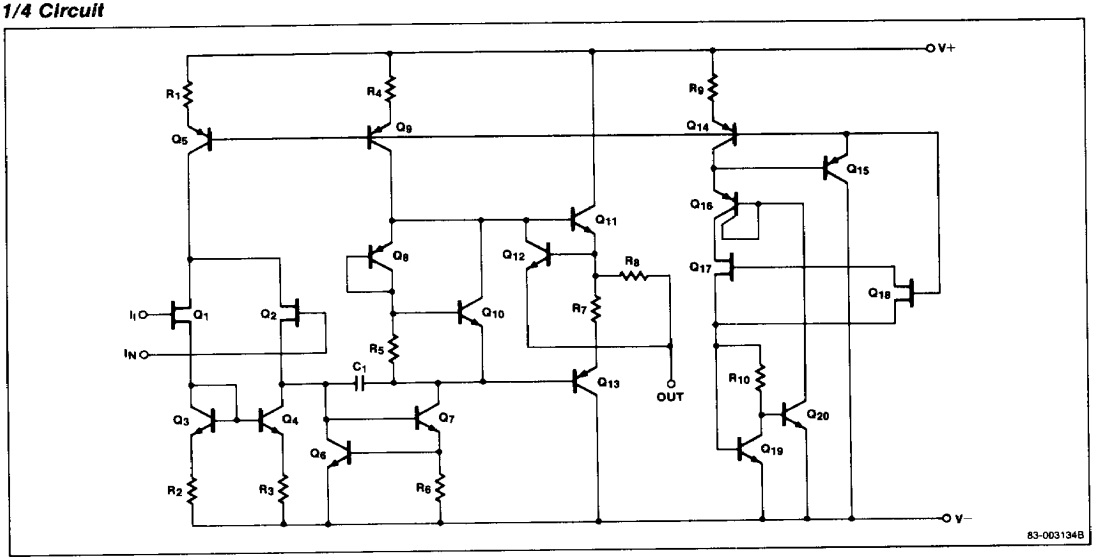


Ordering Information

Part Number	Package	Operating Temperature Range
μPC4064C	14-pin plastic DIP	−20 to +70°C
μPC4064G2	14-pin Miniflat	−20 to +70°C

Equivalent Circuit

1/4 Circuit



Absolute Maximum Ratings

$T_A = 25°C$

Supply Voltage Differential	36 V
Power Dissipation, C Package (Note 1)	570 mW
Power Dissipation, G2 Package (Note 2)	550 mW
Differential Input Voltage (Note 3)	±30 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−20 to 70°C

Note:

1. Derate at 8 mW/°C when $T_A > 25°C$.
2. Derate at 5.5 mW/°C when $T_A > 25°C$.
3. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Recommended Operating Conditions

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply Voltage	V_{SUPP}	±2		±16	V
Output Current	I_O			5	mA
Load Capacitance	C_L			220	pF

Electrical Characteristics

$T_A = +25°C$, $V_{SUPP} = ±15$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Offset Voltage	V_{io}		2	10	mV	$R_S = 50Ω$
Input Offset Voltage	V_{io}			15	mV	$R_S = 50\ Ω$, $T_A = T_{opt}$
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		10		μV/°C	$R_S = 50\ Ω$, $T_A = T_{opt}$
Input Offset Current	I_{io}		5	50	pA	
Input Offset Current	I_{io}			1.5	nA	$T_A = T_{opt}$
Input Bias Current	I_b		10	100	pA	
Input Bias Current	I_b			3	nA	$T_A = T_{opt}$
Large Signal Voltage Gain	A_{VOL}	70	76		dB	$R1 = 10k$, $V_O = 10$ V
Supply Current	I_{SUPP}		800	1000	μA	
Common Mode Rejection Ratio	CMRR	70	95		dB	
Power Supply Rejection Ratio	PSRR	70	95		dB	
Output Voltage Swing	$±V_O$	±12	±14		V	$R1 = 10k$
Common Mode Input Voltage	V_{cm}	±12	+15 −13		V	
Output Current	I_O	5 −3.5			mA	$±V_O = ±10$ V
Slew Rate	SR		3		V/μs	$R1 = 10k$
Input Noise Voltage	en		30		nV/√Hz	f = 1 kHz
Gain Bandwidth Product	GBW		1		MHz	
Channel Separation	CS		120		dB	f = 1 to 20 kHz

Electrical Characteristics

$T_A = +25°C$, $V_{SUPP} = ±5$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Large Signal Voltage Gain	A_{VOL}	20			dB	
Common Mode Rejection Ratio	CMRR	70	90		dB	
Power Supply Rejection Ratio	PSRR	70	90		dB	
Output Voltage Swing	$±V_O$	±3.8	±4.1		V	$R1 = 10k$
Common Mode Input Voltage	V_{cm}	+4.7 −2.8	+5.2 −3.5		V	