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FDMS6673BZ

P-Channel PowerTrench[®] MOSFET

-30 V, -82 A, 6.8 mΩ

Features

- Max $r_{DS(on)}$ = 6.8 mΩ at $V_{GS} = -10$ V, $I_D = -15.2$ A
- Max $r_{DS(on)}$ = 12.5 mΩ at $V_{GS} = -4.5$ V, $I_D = -11.2$ A
- Advanced Package and Silicon Combination for Low $r_{DS(on)}$
- HBM ESD Protection Level of 8 kV Typical(Note 3)
- MSL1 Robust Package Design
- RoHS Compliant

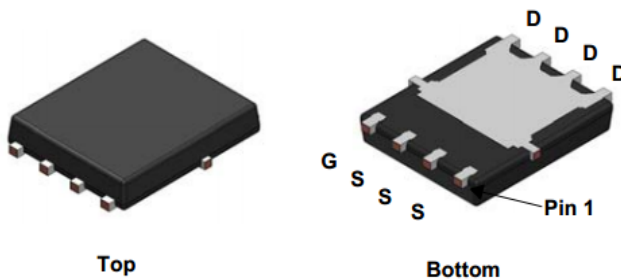


General Description

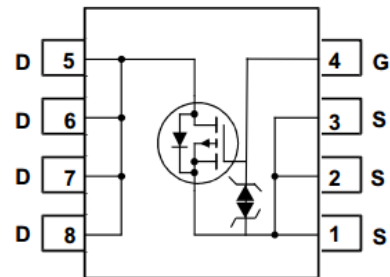
The FDMS6673BZ has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ and ESD protection.

Applications

- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management



Power 56



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-30	V
V_{GS}	Gate to Source Voltage	± 25	V
I_D	Drain Current -Continuous $T_C = 25^\circ\text{C}$ (Note 5)	-82	A
	-Continuous $T_C = 100^\circ\text{C}$ (Note 5)	-52	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	-15.2	
	-Pulsed (Note 4)	-422	
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	73	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS6673BZ	FDMS6673BZ	Power 56	13 "	12 mm	3000 units



Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-18		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\text{ }\mu\text{A}$	-1.0	-1.8	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{ V}$, $I_D = -15.2\text{ A}$		5.2	6.8	m Ω
		$V_{GS} = -4.5\text{ V}$, $I_D = -11.2\text{ A}$		7.8	12.5	
		$V_{GS} = -10\text{ V}$, $I_D = -15.2\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		7.5	9.8	
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}$, $I_D = -15.2\text{ A}$		76		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		4444	5915	pF
C_{oss}	Output Capacitance			781	1040	pF
C_{rss}	Reverse Transfer Capacitance			695	1045	pF
R_g	Gate Resistance			4.5		Ω

Switching Characteristics

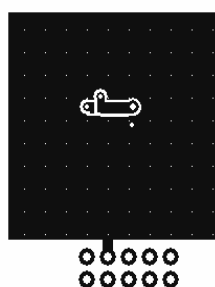
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}$, $I_D = -15.2\text{ A}$, $V_{GS} = -10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		14	26	ns
t_r	Rise Time			28	45	ns
$t_{d(off)}$	Turn-Off Delay Time			97	156	ns
t_f	Fall Time			79	127	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to -10 V	$V_{DD} = -15\text{ V}$, $I_D = -15.2\text{ A}$	93	130	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to -5 V		52	73	nC
Q_{gs}	Gate to Source Charge			13		nC
Q_{gd}	Gate to Drain "Miller" Charge			26		nC

Drain-Source Diode Characteristics

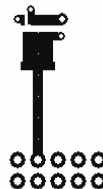
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -2.1\text{ A}$ (Note 2)		0.7	1.20	V
		$V_{GS} = 0\text{ V}$, $I_S = -15.2\text{ A}$ (Note 2)		0.8	1.25	
t_{rr}	Reverse Recovery Time	$I_F = -15.2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		33	53	ns
Q_{rr}	Reverse Recovery Charge			20	32	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $125\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2: Pulse Test: Pulse Width $< 300\text{ }\mu\text{s}$, Duty cycle $< 2.0\%$.

3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

4: Pulsed I_D please refer to Fig 11 SOA graph for more details.

5: Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal/electro-mechanical application board design.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

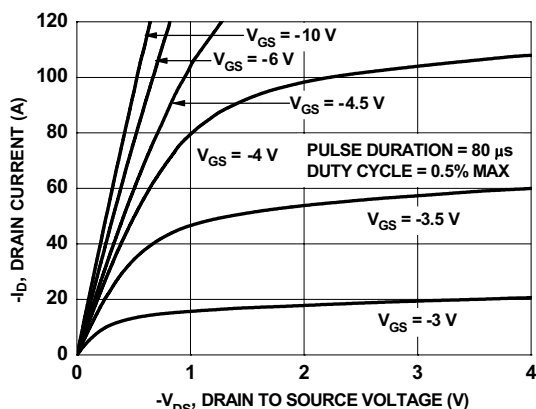


Figure 1. On Region Characteristics

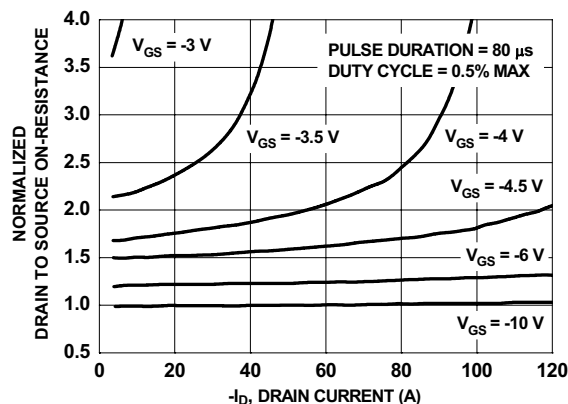


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

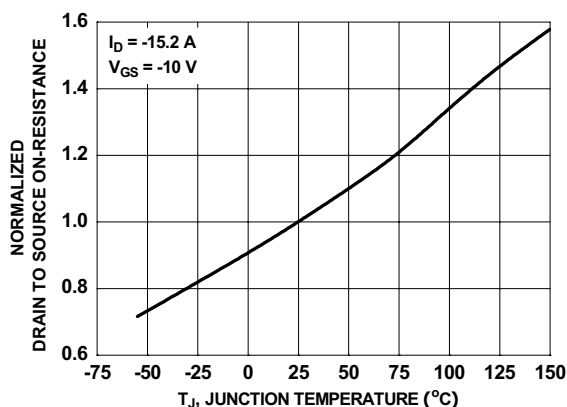


Figure 3. Normalized On Resistance vs. Junction Temperature

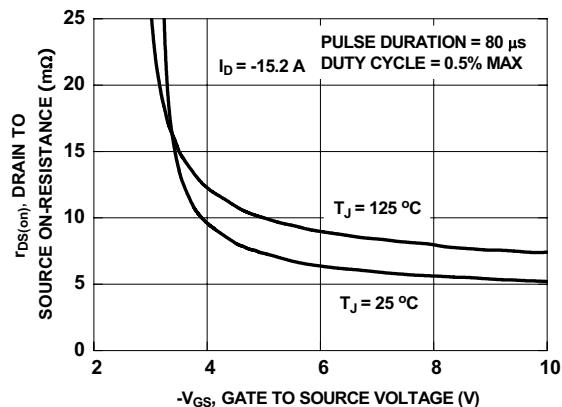


Figure 4. On-Resistance vs. Gate to Source Voltage

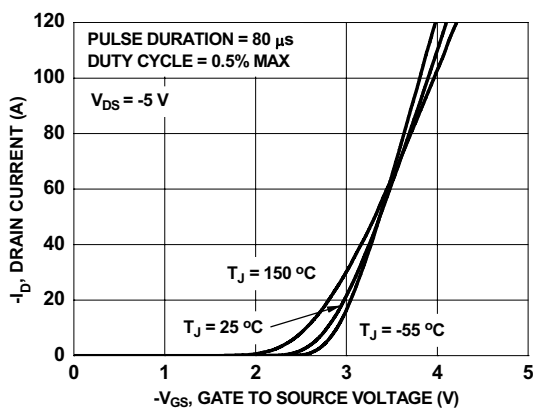


Figure 5. Transfer Characteristics

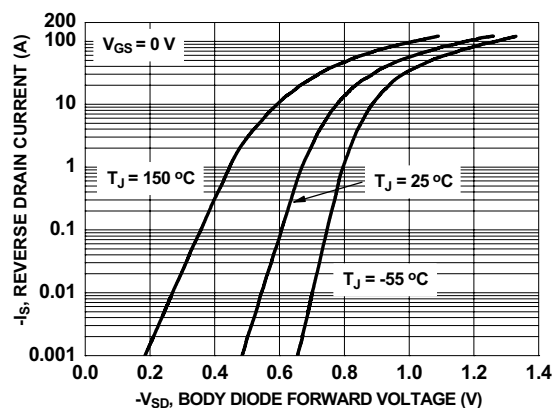


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

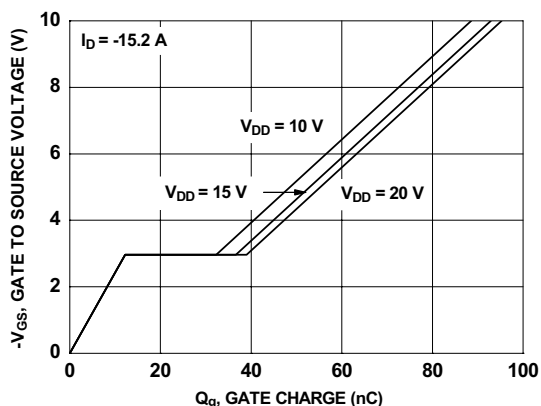


Figure 7. Gate Charge Characteristics

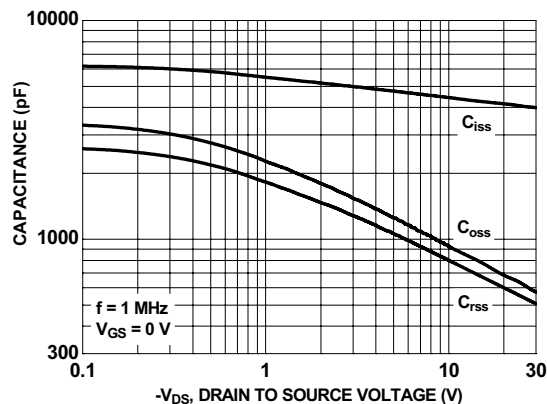


Figure 8. Capacitance vs. Drain to Source Voltage

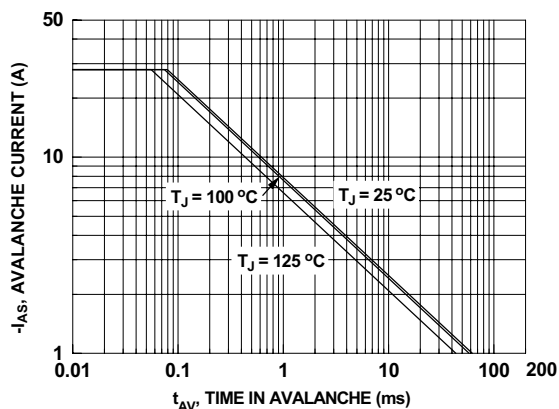


Figure 9. Unclamped Inductive Switching Capability

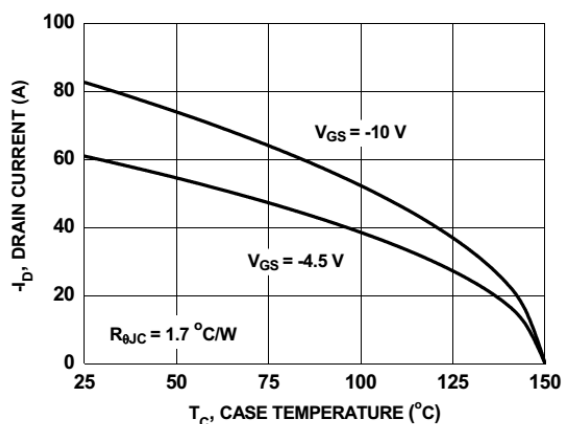


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

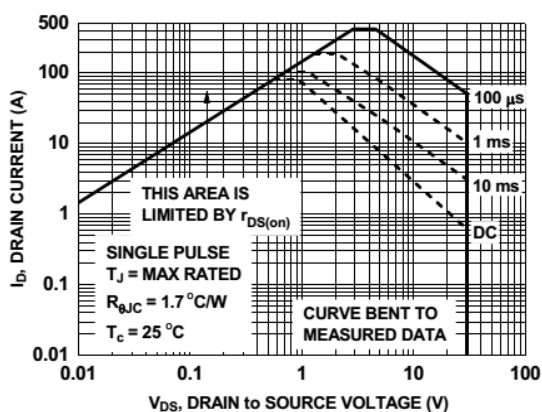


Figure 11. Forward Bias Safe Operating Area

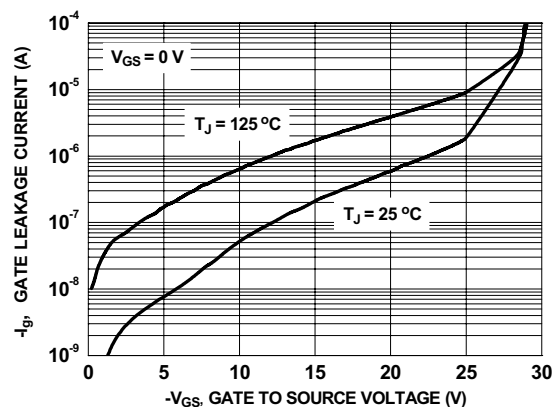


Figure 12. I_{gss} vs. V_{gss}

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

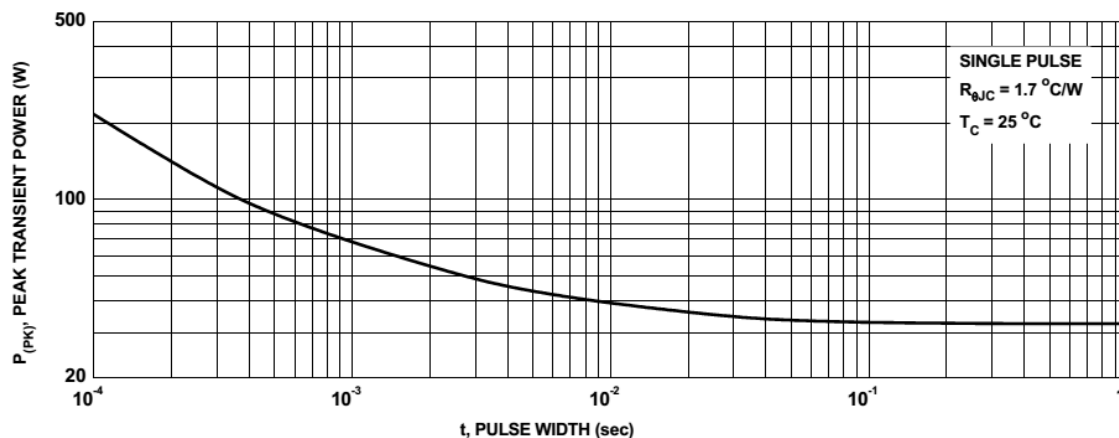


Figure 13. Single Pulse Maximum Power Dissipation

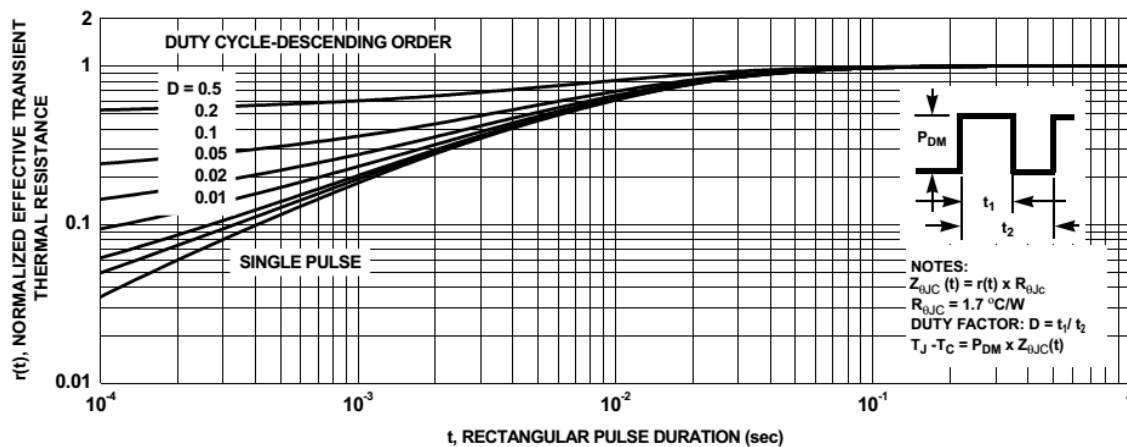
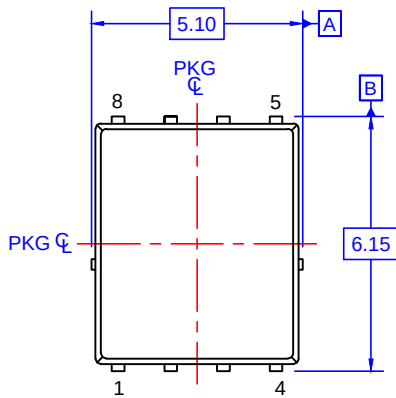
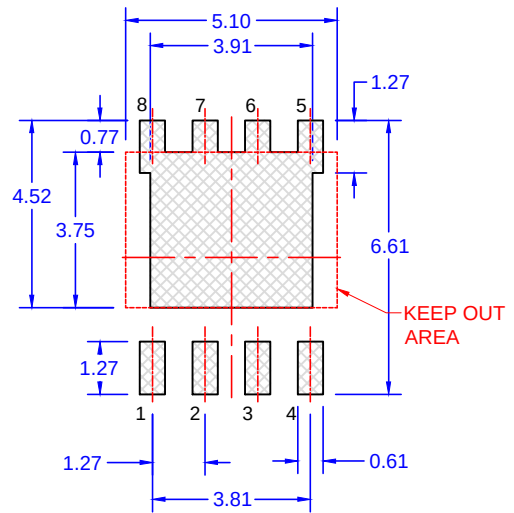
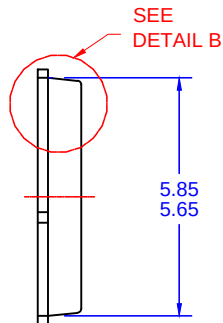


Figure 14. Junction-to-Case Transient Thermal Response Curve

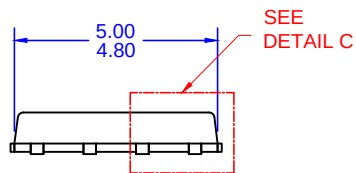
PQFN8 5X6, 1.27P
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ISSUE A



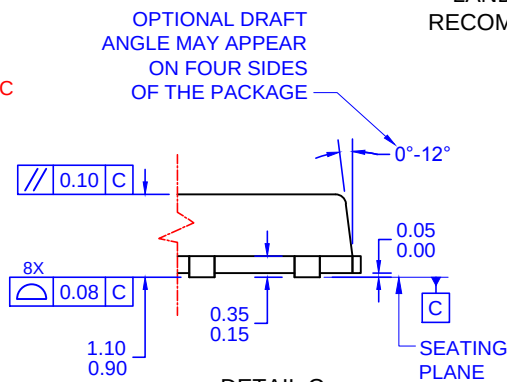
TOP VIEW



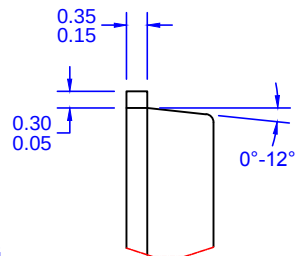
LAND PATTERN
RECOMMENDATION



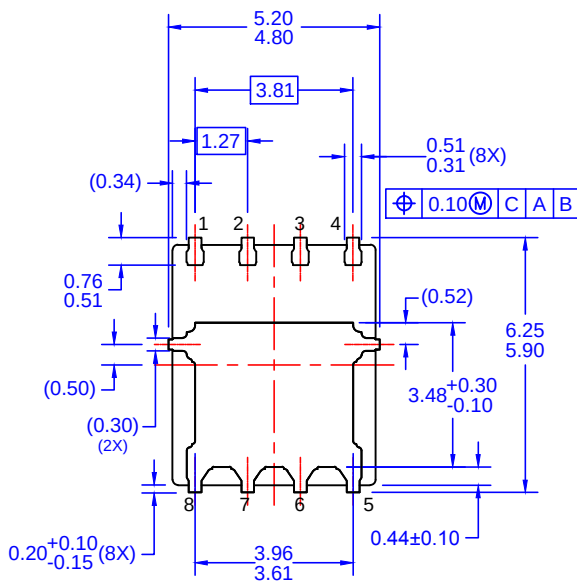
SIDE VIEW



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,.
- DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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