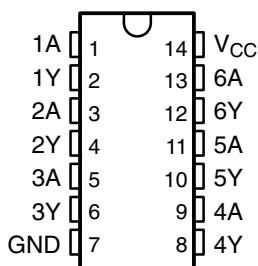
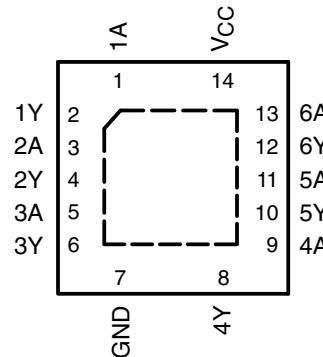


- Operating Range 2-V to 5.5-V  $V_{CC}$
- Unbuffered Outputs
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

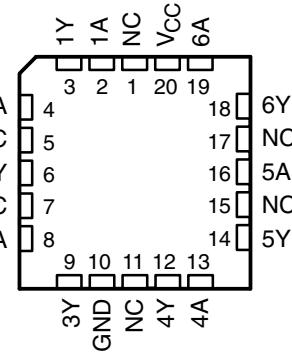
SN54AHCU04 . . . J OR W PACKAGE  
SN74AHCU04 . . . D, DB, DGV, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74AHCU04 . . . RGY PACKAGE  
(TOP VIEW)



SN54AHCU04 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'AHCU04 devices contain six independent inverters. These devices perform the Boolean function  $Y = \bar{A}$ . Internal circuitry consists of single-stage inverters that can be used in analog applications such as crystal oscillators.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74AHCU04RGYR	HD04
	PDIP – N	Tube	SN74AHCU04N	SN74AHCU04N
	SOIC – D	Tube	SN74AHCU04D	AHCU04
		Tape and reel	SN74AHCU04DR	
	SOP – NS	Tape and reel	SN74AHCU04NSR	AHCU04
	SSOP – DB	Tape and reel	SN74AHCU04DBR	HD04
	TSSOP – PW	Tube	SN74AHCU04PW	HD04
		Tape and reel	SN74AHCU04PWR	
-55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHCU04DGVR	HD04
	CDIP – J	Tube	SNJ54AHCU04J	SNJ54AHCU04J
	CFP – W	Tube	SNJ54AHCU04W	SNJ54AHCU04W
LCCC – FK	LCCC – FK	Tube	SNJ54AHCU04FK	SNJ54AHCU04FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

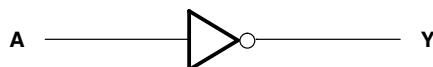
## **SN54AHCU04, SN74AHCU04 HEX INVERTERS**

SCLS234K – OCTOBER 1995 – REVISED JULY 2003

## FUNCTION TABLE (each inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.
  3. The package thermal impedance is calculated in accordance with JESD 51-5.

**recommended operating conditions (see Note 4)**

			SN54AHCU04		SN74AHCU04		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub> Supply voltage			2	5.5	2	5.5	V
V <sub>IH</sub> High-level input voltage	V <sub>CC</sub> = 2 V		1.7	1.7			V
	V <sub>CC</sub> = 3 V		2.4	2.4			
	V <sub>CC</sub> = 5.5 V		4.4	4.4			
V <sub>IL</sub> Low-level input voltage	V <sub>CC</sub> = 2 V		0.3	0.3			V
	V <sub>CC</sub> = 3 V		0.6	0.6			
	V <sub>CC</sub> = 5.5 V		1.1	1.1			
V <sub>I</sub> Input voltage			0	5.5	0	5.5	V
V <sub>O</sub> Output voltage			0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub> High-level output current	V <sub>CC</sub> = 2 V		-50	-50			µA
	V <sub>CC</sub> = 3.3 V ± 0.3 V		-4	-4			mA
	V <sub>CC</sub> = 5 V ± 0.5 V		-8	-8			
I <sub>OL</sub> Low-level output current	V <sub>CC</sub> = 2 V		50	50			µA
	V <sub>CC</sub> = 3.3 V ± 0.3 V		4	4			mA
	V <sub>CC</sub> = 5 V ± 0.5 V		8	8			
T <sub>A</sub> Operating free-air temperature			-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCU04		SN74AHCU04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.8	2		1.8		1.8		V
		3 V	2.7	3		2.7		2.7		
		4.5 V	4	4.5		4		4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V		0.2		0.2		0.2		V
		3 V		0.3		0.3		0.3		
		4.5 V		0.5		0.5		0.5		
	I <sub>OL</sub> = 4 mA	3 V		0.36		0.5		0.44		
	I <sub>OL</sub> = 8 mA	4.5 V		0.36		0.5		0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1		±1*		±1		µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2		20		20		µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	2	10				10		pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

# SN54AHCU04, SN74AHCU04 HEX INVERTERS

SCLS234K – OCTOBER 1995 – REVISED JULY 2003

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCU04		SN74AHCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$		5*	7.1*	1*	8.5*	1	8.5	ns
$t_{PHL}$					5*	7.1*	1*	8.5*	1	8.5	
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$		7.5	10.6	1	12	1	12	ns
$t_{PHL}$					7.5	10.6	1	12	1	12	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCU04		SN74AHCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$		3.5*	5.5*	1*	6*	1	6.5	ns
$t_{PHL}$					3.5*	5.5*	1*	6*	1	6.5	
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$		5	7	1	8	1	8	ns
$t_{PHL}$					5	7	1	8	1	8	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**noise characteristics,  $V_{CC} = 5 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)**

PARAMETER	SN74AHCU04			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.5		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.5		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4.3		V
$V_{IH(D)}$ High-level dynamic input voltage		4		V
$V_{IL(D)}$ Low-level dynamic input voltage		1		V

NOTE 5: Characteristics are for surface-mount packages only.

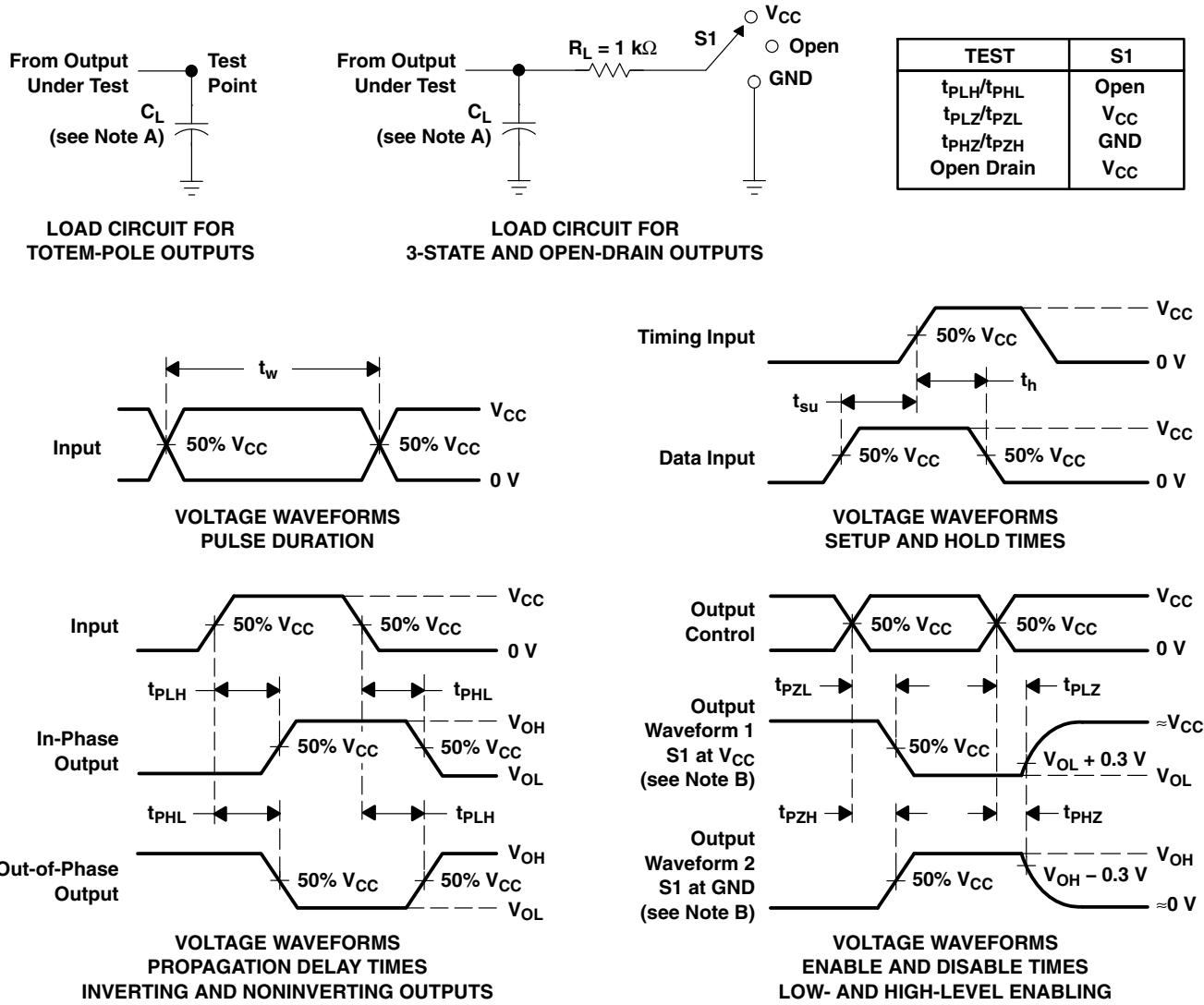
**operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1 \text{ MHz}$	7.3	pF



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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - The outputs are measured one at a time with one input transition per measurement.
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9680301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9680301Q2A SNJ54AHCU04FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9680301QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9680301QC A SNJ54AHCU04J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9680301QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9680301QD A SNJ54AHCU04W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04DBLE	OBsolete	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCU04DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04DGVR	OBsolete	TVSOP	DGV	14		TBD	Call TI	Call TI	-40 to 85	HD04	
SN74AHCU04DGVRE4	OBsolete	TVSOP	DGV	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCU04DGVRG4	OBsolete	TVSOP	DGV	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCU04DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCU04N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCU04NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCU04N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04PWLE	OBsolete	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCU04PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCU04RGYRG4	ACTIVE	VQFN	RGY	14		TBD	Call TI	Call TI	-40 to 85	HD04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AHCU04FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9680301Q2A SNJ54AHCU04FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AHCU04J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9680301QC A SNJ54AHCU04J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AHCU04W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9680301QD A SNJ54AHCU04W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54AHCU04, SN74AHCU04 :**

- Catalog: [SN74AHCU04](#)
- Automotive: [SN74AHCU04-Q1](#), [SN74AHCU04-Q1](#)
- Enhanced Product: [SN74AHCU04-EP](#), [SN74AHCU04-EP](#)
- Military: [SN54AHCU04](#)

NOTE: Qualified Version Definitions:



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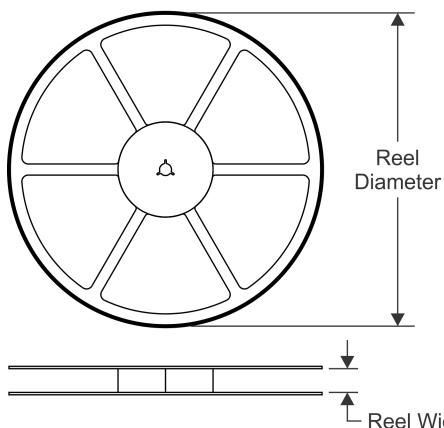
## PACKAGE OPTION ADDENDUM

25-Sep-2013

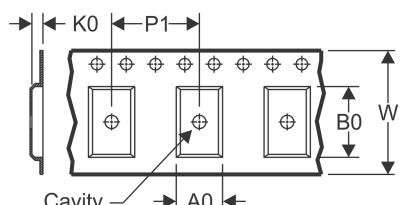
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

## REEL DIMENSIONS

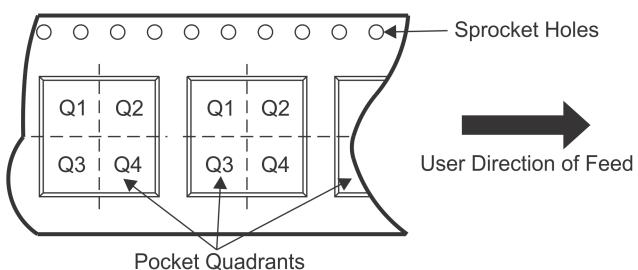


## TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

All dimensions are nominal													
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	
SN74AHCU04DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1	
SN74AHCU04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1	
SN74AHCU04NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1	
SN74AHCU04PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1	

**TAPE AND REEL BOX DIMENSIONS**

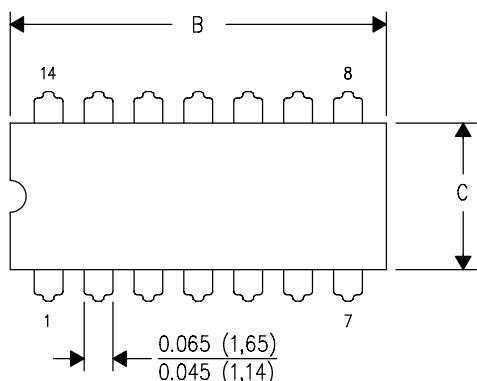

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCU04DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74AHCU04DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AHCU04NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74AHCU04PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

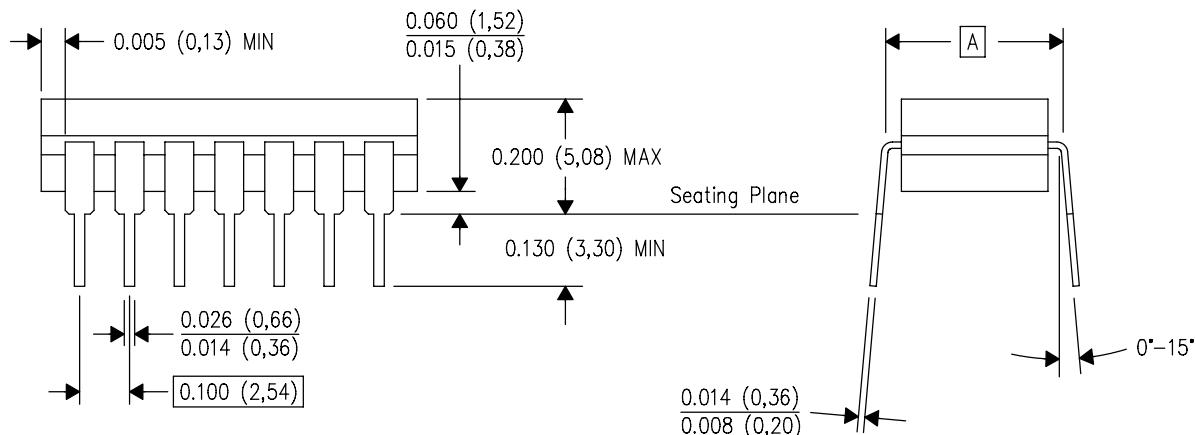
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

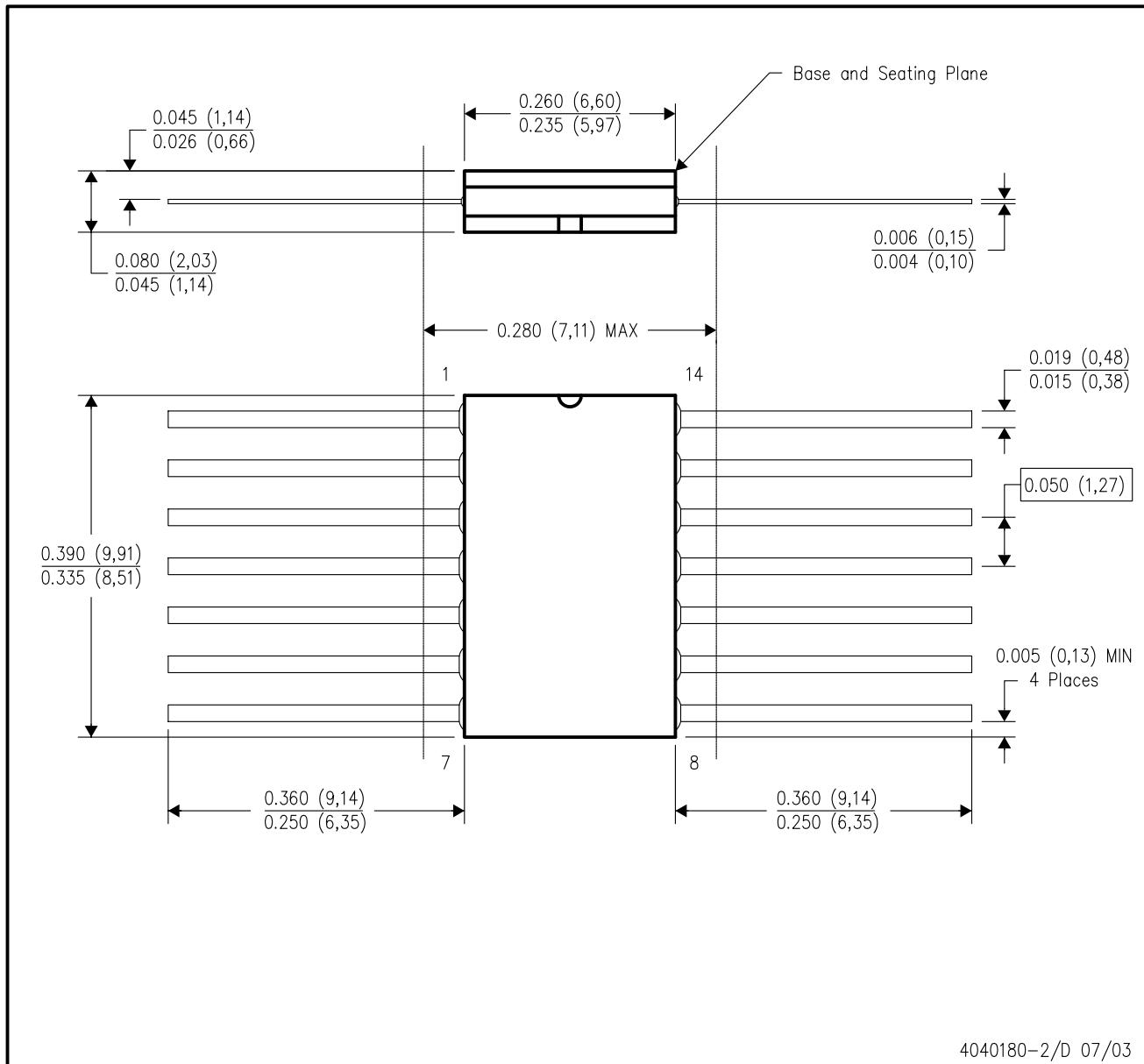


4040083/F 03/03

- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

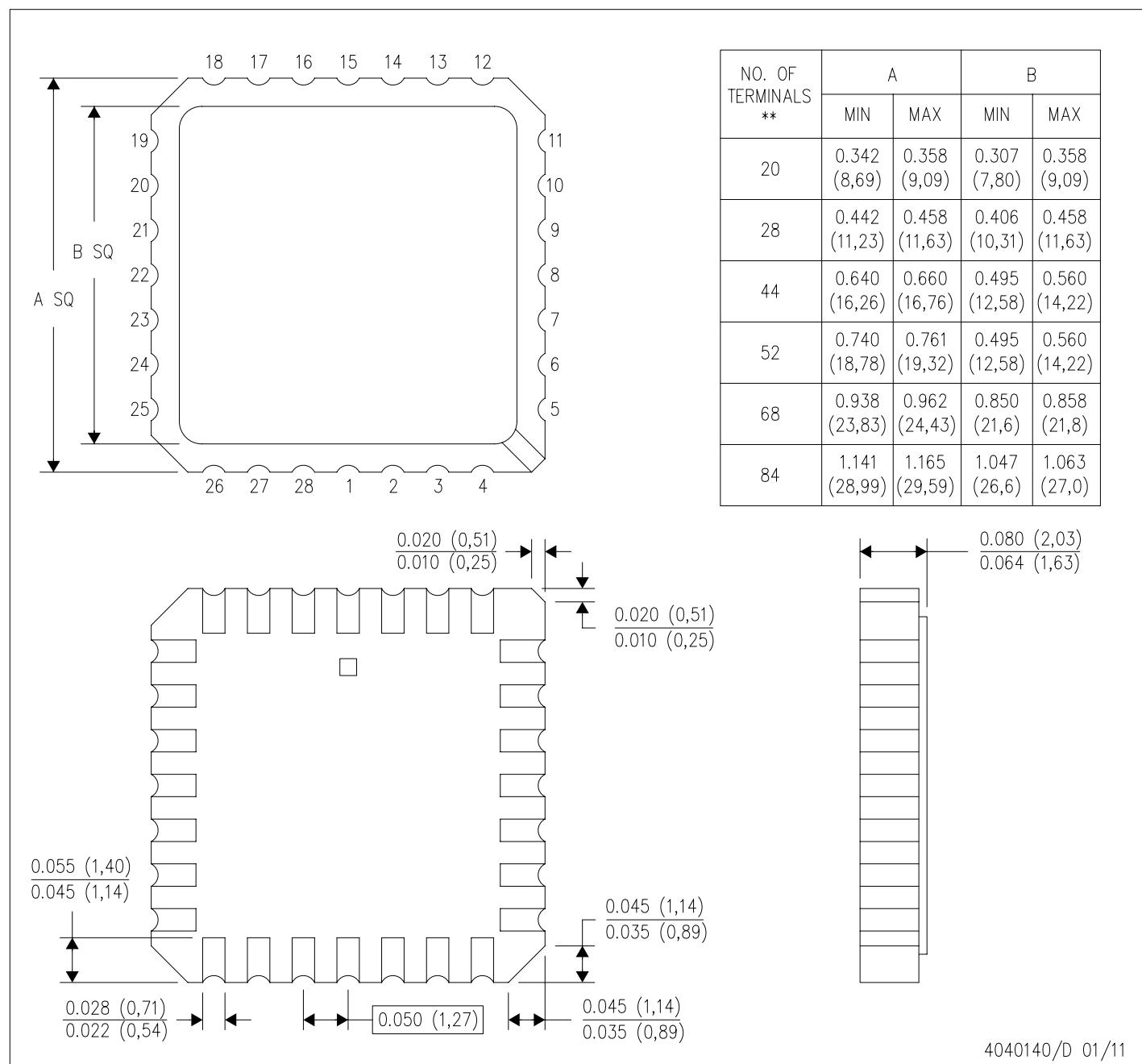


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL-STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



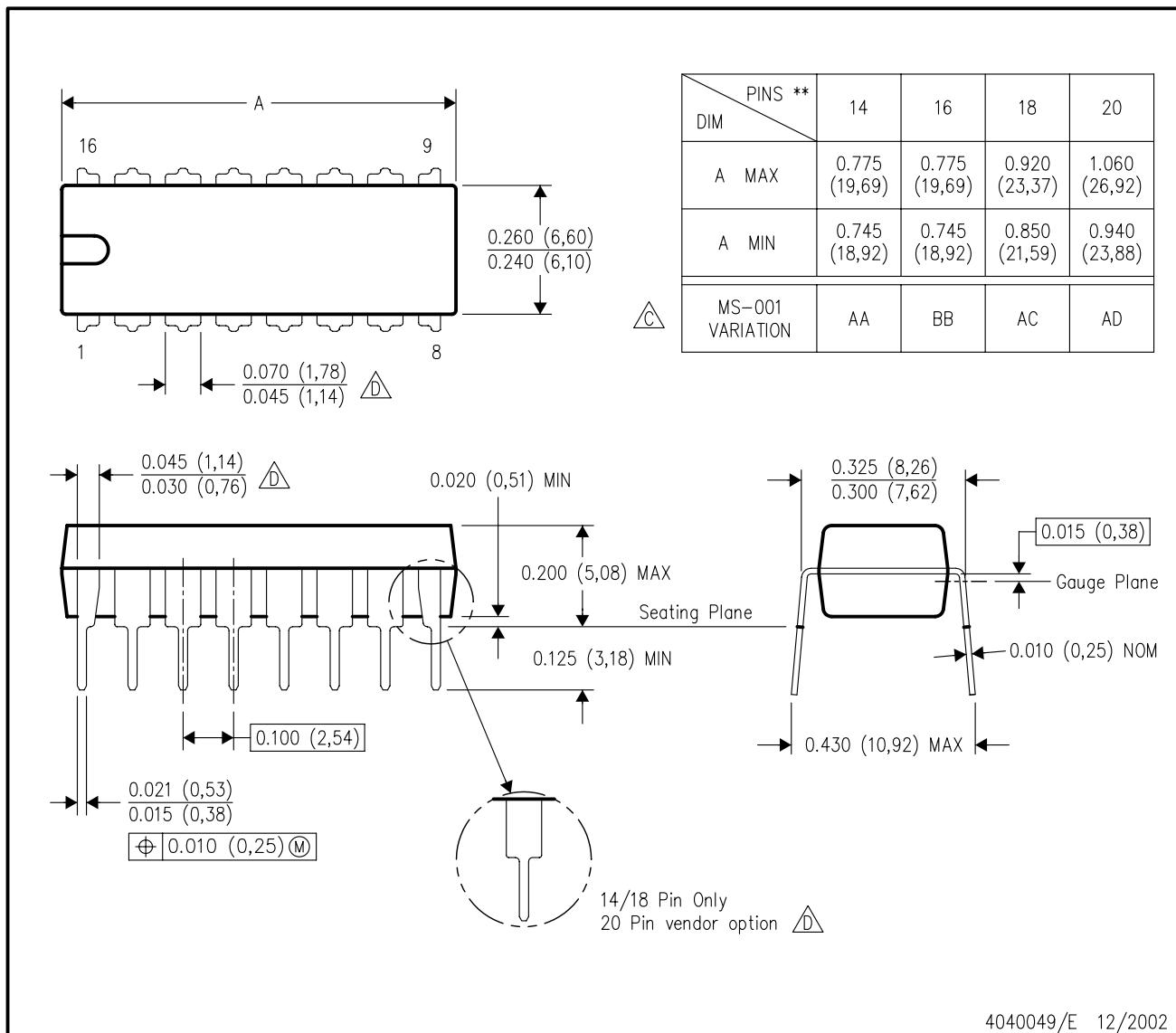
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. Falls within JEDEC MS-004

4040140/D 01/11

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

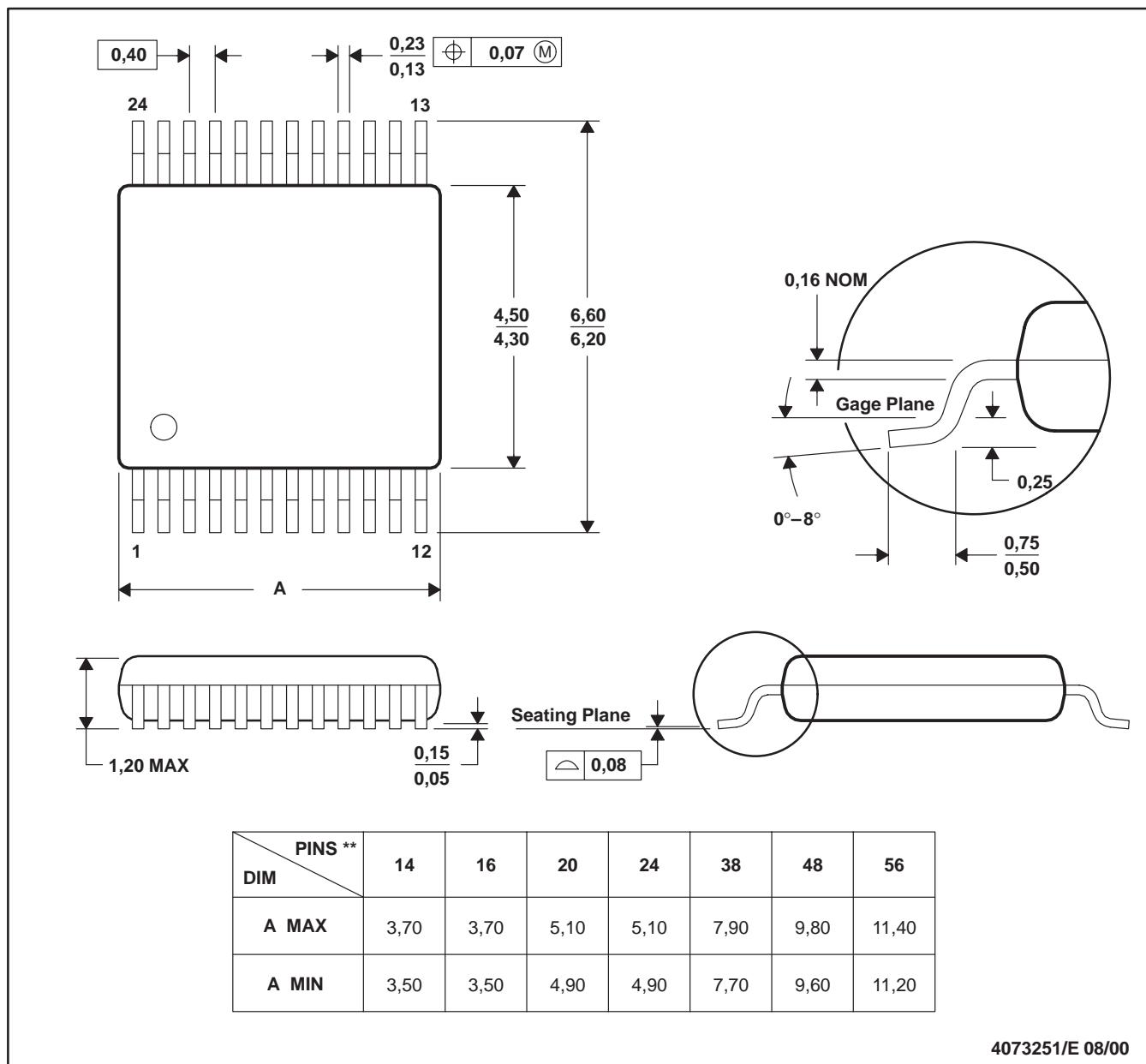
△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

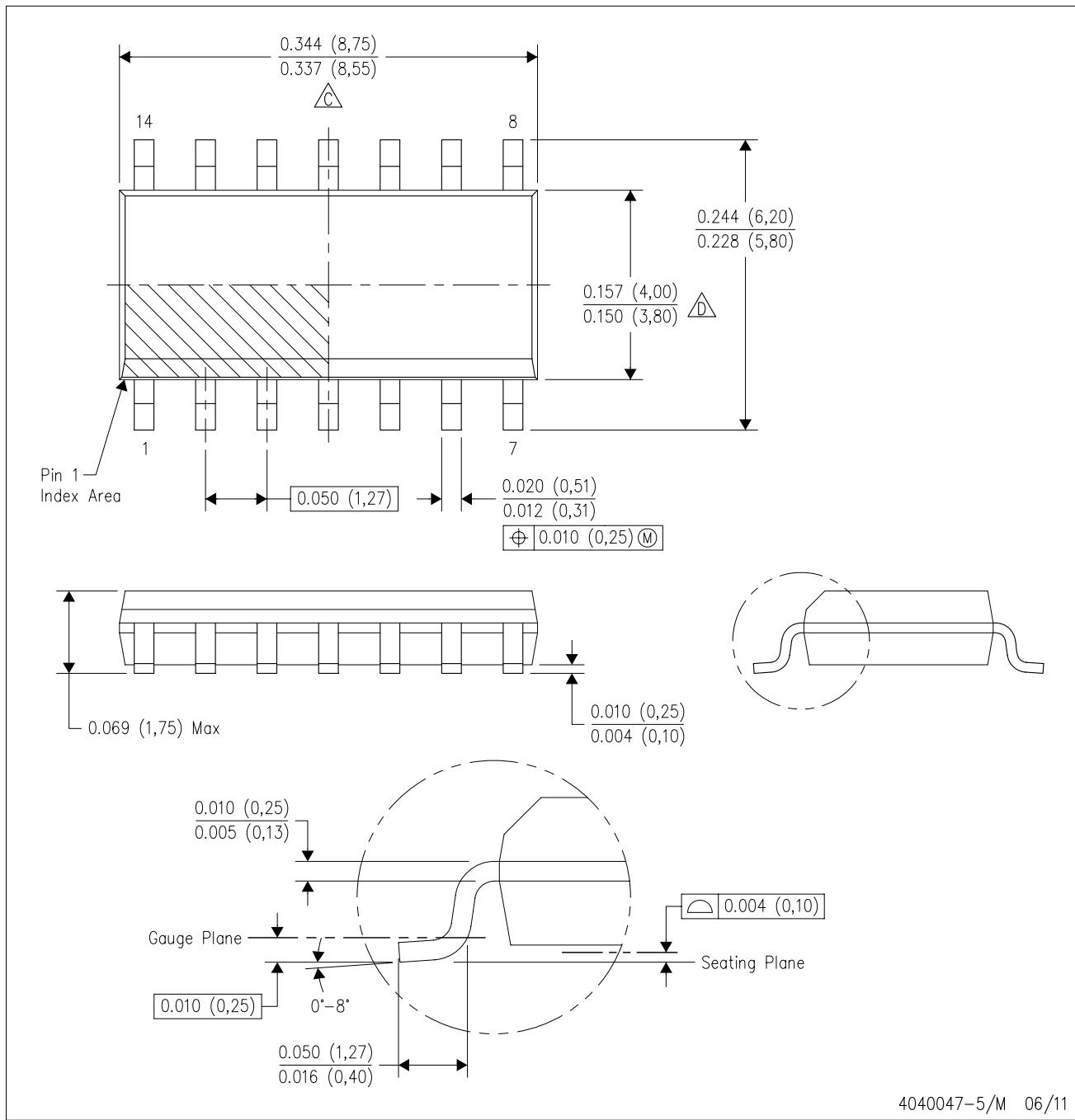
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

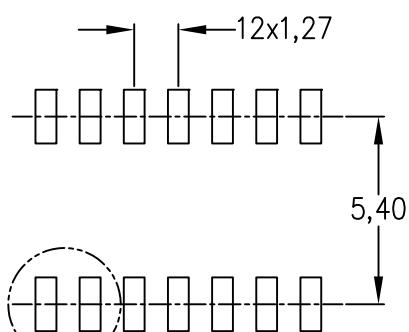
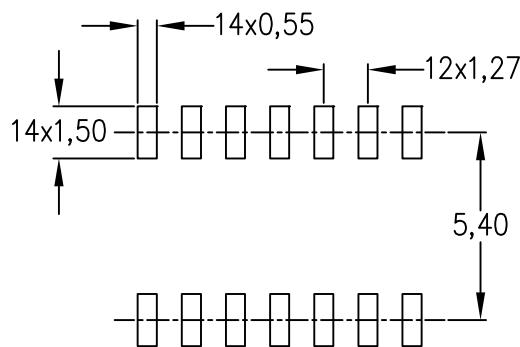
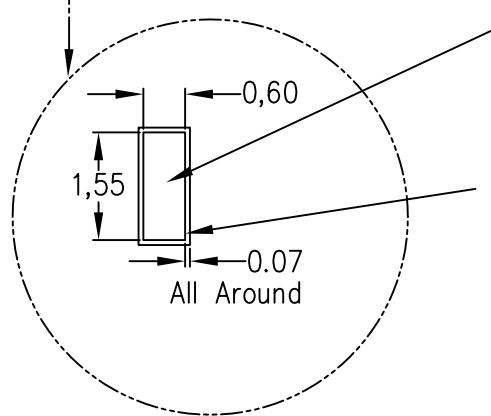
D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AB.

4040047-5/M 06/11

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

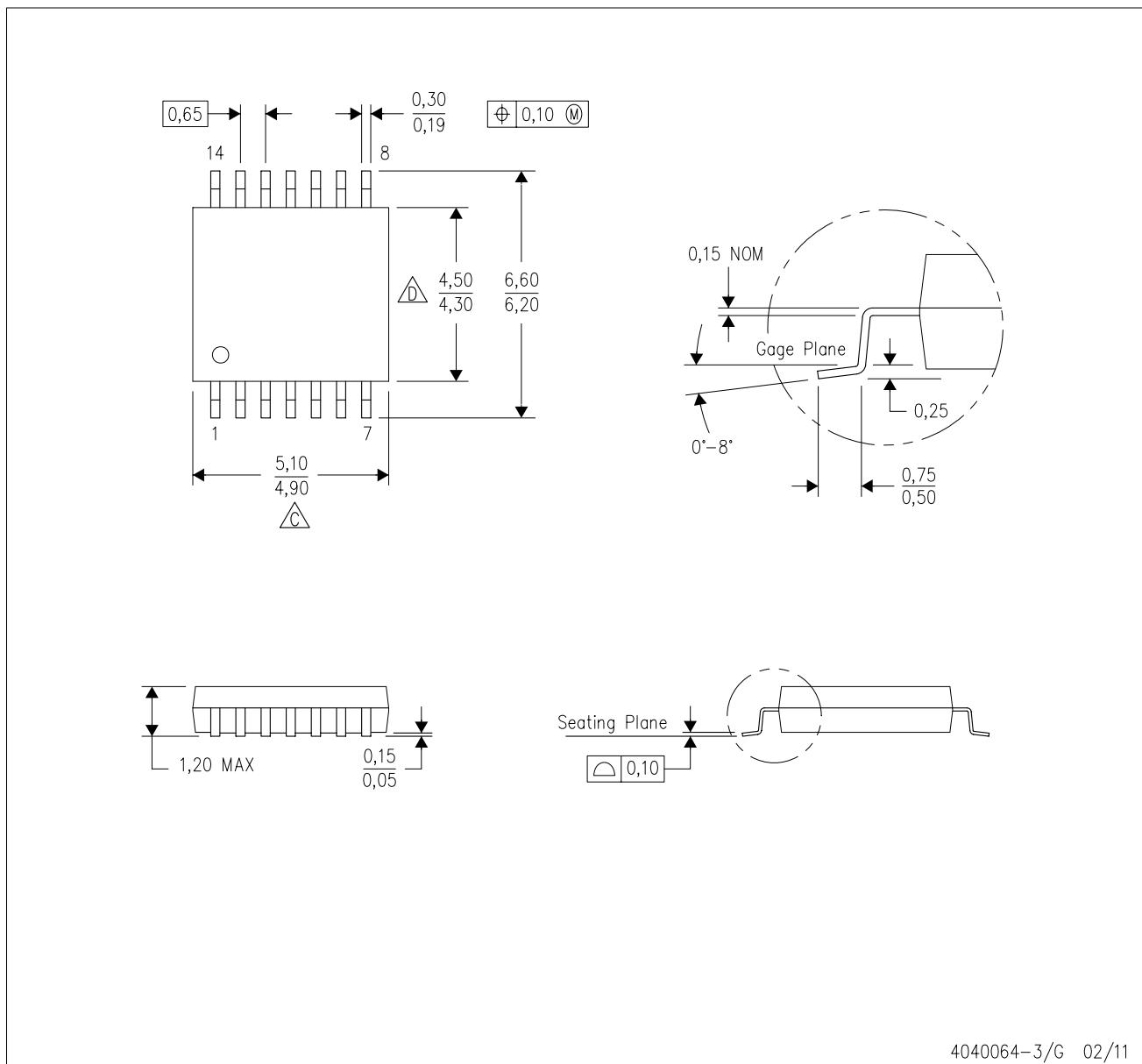
Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

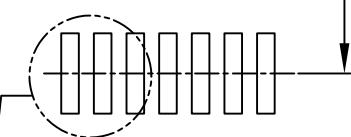
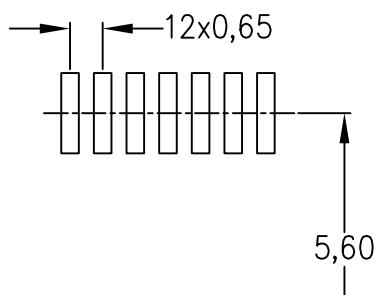
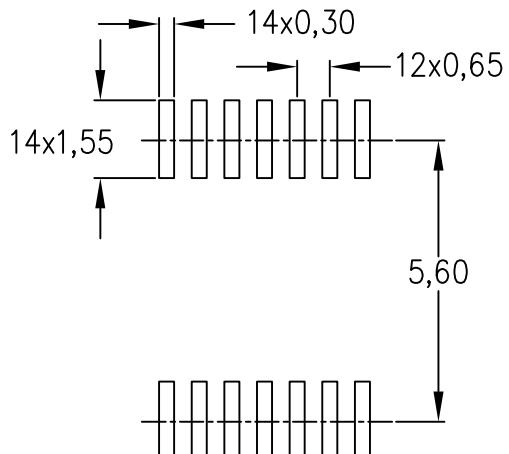
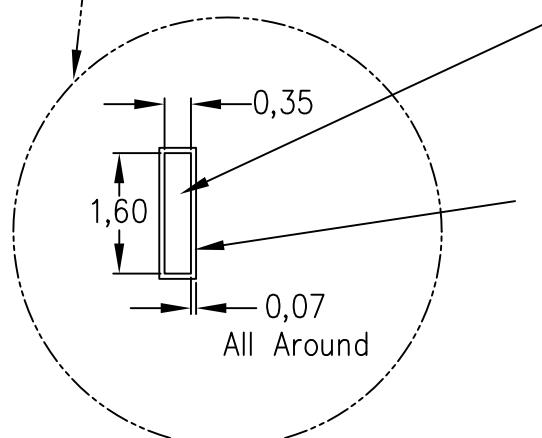
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

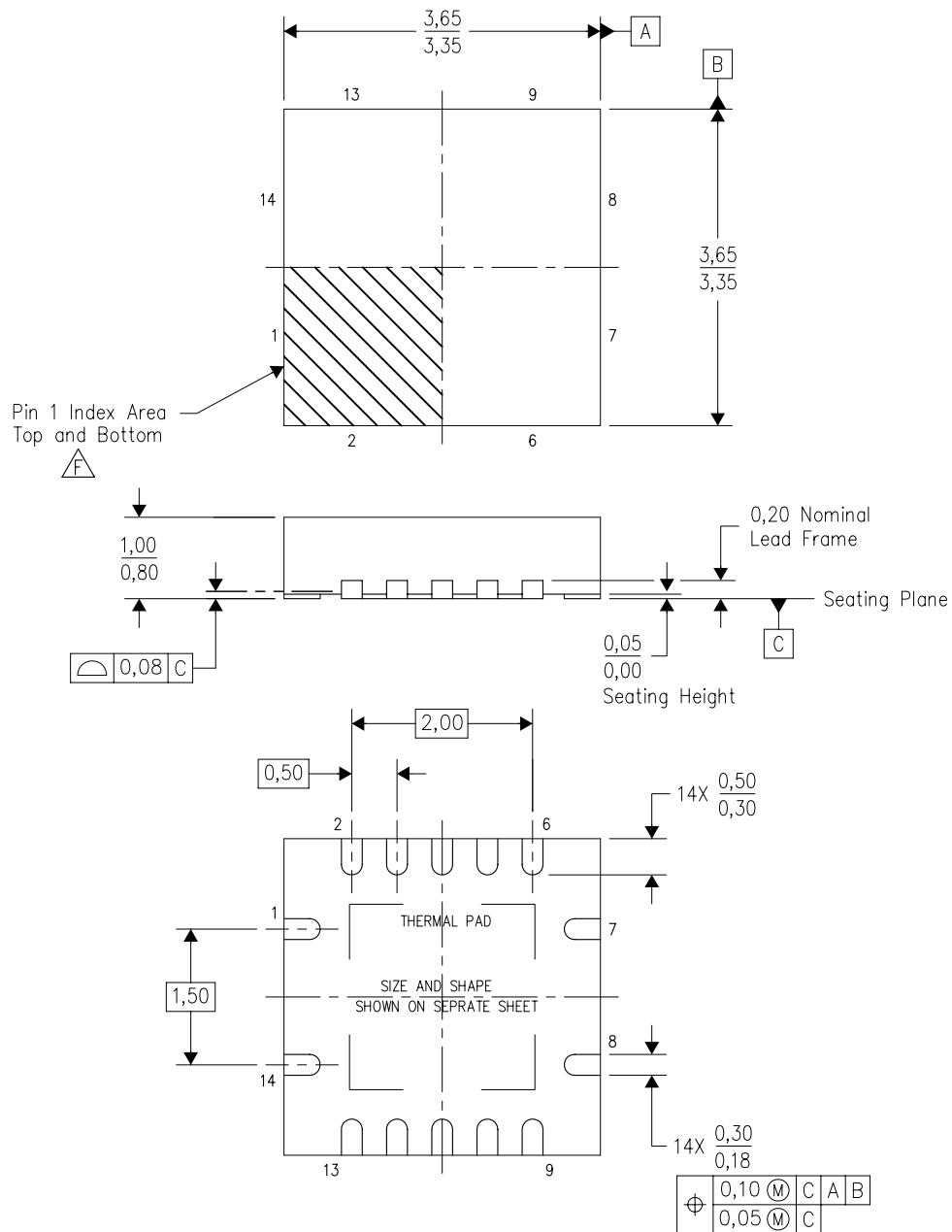
4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-2/l 06/2011

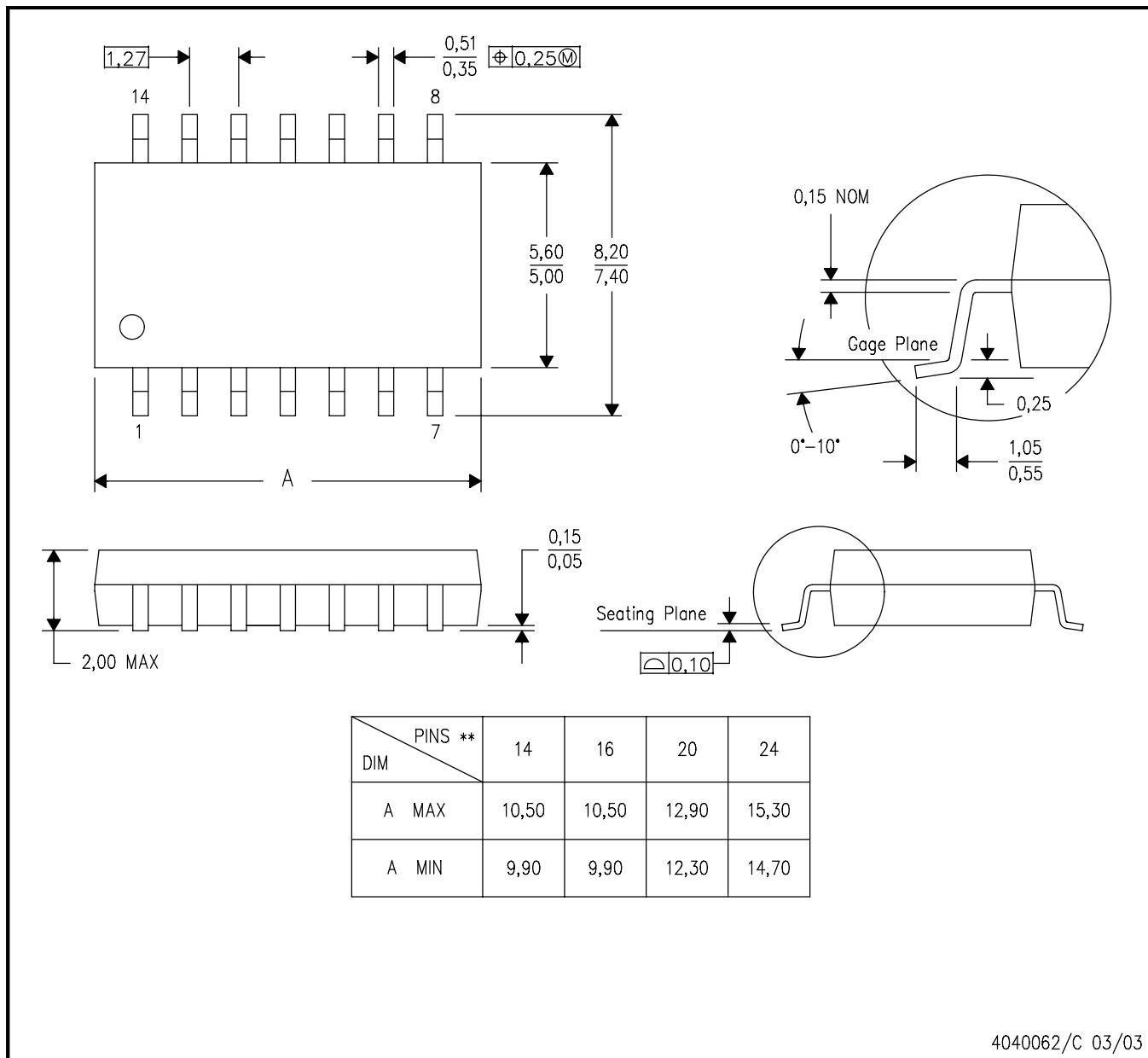
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



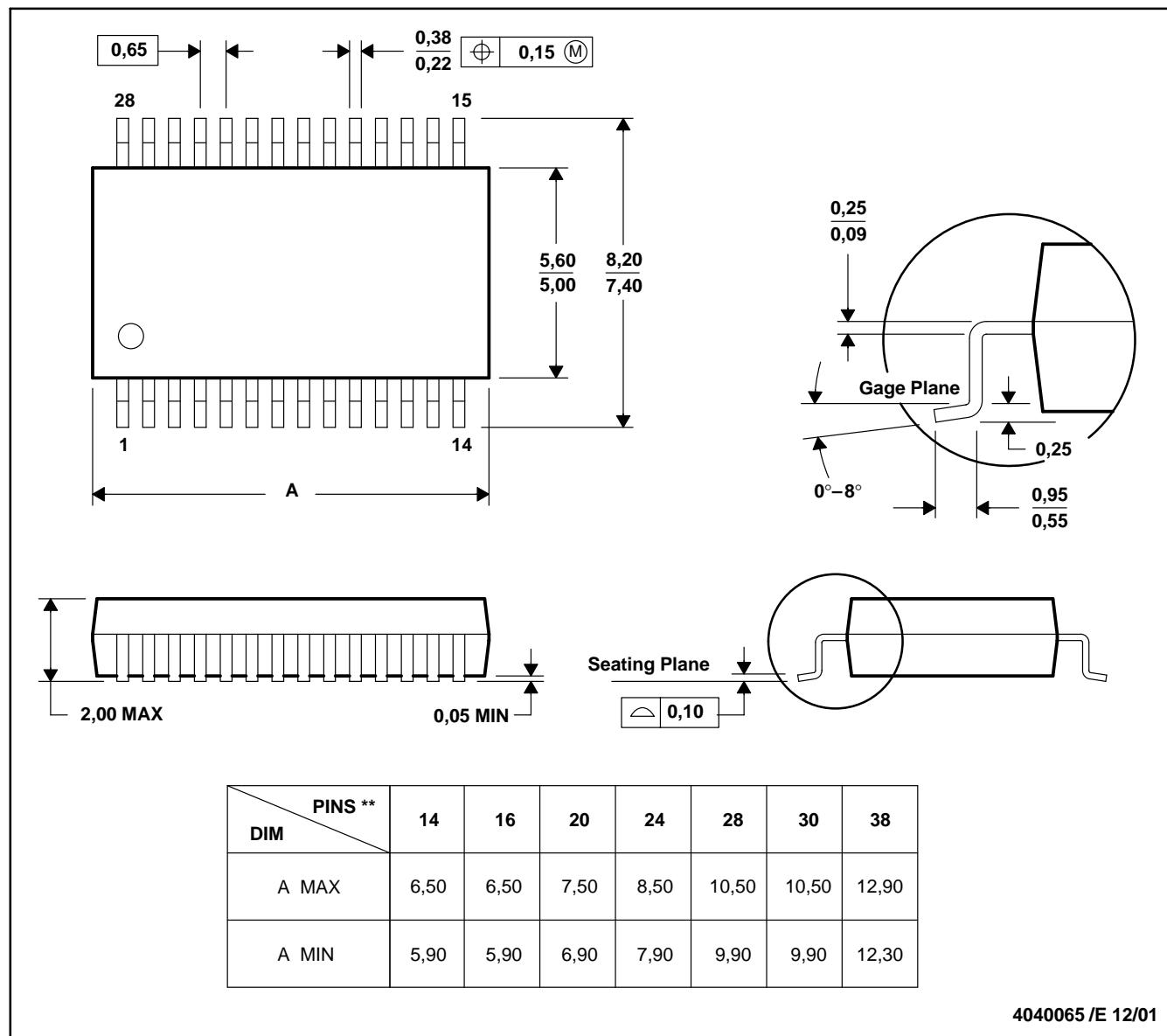
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
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OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>
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