

## LPV511 Micropower, Rail-to-Rail Input and Output Operational Amplifier

Check for Samples: [LPV511](#)

### FEATURES

(Typical at 3V Supply Unless Otherwise Noted)

- Wide Supply Voltage Range 2.7V to 12V
- Slew Rate 7.7 V/ms
- Supply Current 880 nA
- Output Short Circuit Current 1.35 mA
- Rail-to-Rail Input
- Rail-to-Rail Output 100 mV from Rails
- Bandwidth (C<sub>L</sub> = 50 pF, R<sub>L</sub> = 1 MΩ) 27 kHz
- Unity Gain Stable

### APPLICATIONS

- Battery Powered Systems
- Security Systems
- Micropower Thermostats
- Solar Powered Systems
- Portable Instrumentation
- Micropower Filter
- Remote Sensor Amplifier

### Typical Application

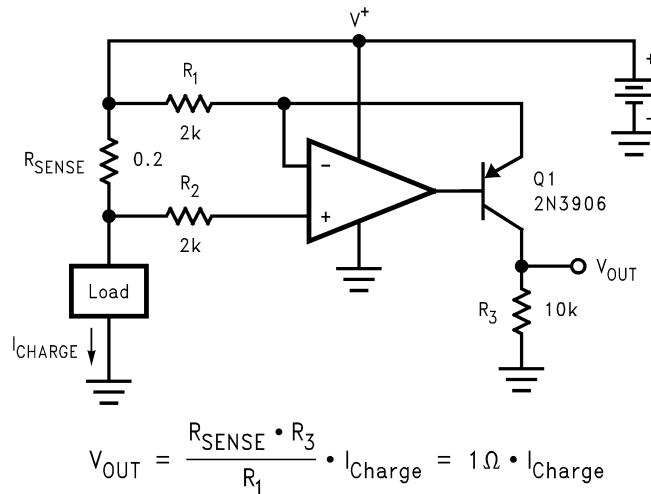


Figure 1. High Side Battery Current Sensor

### DESCRIPTION

The LPV511 is a micropower operational amplifier that operates from a voltage supply range as wide as 2.7V to 12V with ensured specifications at 3V, 5V and 12V. The LPV511 exhibits an excellent speed to power ratio, drawing only 880 nA of supply current with a bandwidth of 27 kHz. These specifications make the LPV511 an ideal choice for battery powered systems that require long life through low supply current, such as instrumentation, sensor conditioning and battery current monitoring.

The LPV511 has an input range that includes both supply rails for ground and high side battery sensing applications. The LPV511 output swings within 100 mV of either rail to maximize the signal's dynamic range in low supply applications. In addition, the output is capable of sourcing 650 μA of current when powered by a 12V battery.

The LPV511 is fabricated on TI's advanced VIP50C process.

The LPV511 is available in the space saving SC70 package which makes it ideal for portable electronics with area constrained PC boards.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	Human Body	2 kV
	Machine Model	200V
V <sub>IN</sub> Differential		2.1V
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )		13.2V
Voltage at Input/Output pins		V <sup>+</sup> +0.3V, V <sup>-</sup> -0.3V
Storage Temperature Range		-65°C to +150°C
Short Circuit Duration		See <sup>(4)</sup>
Junction Temperature <sup>(5)</sup>		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp. (10 sec)	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model: 1.5 kΩ in series with 100 pF. Machine Model: 0Ω in series with 200 pF.
- (4) Output short circuit duration is infinite for V<sup>+</sup> < 6V at room temperature and below. For V<sup>+</sup> > 6V, allowable short circuit duration is 1.5 ms.
- (5) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC board.

## Operating Ratings<sup>(1)</sup>

Temperature Range <sup>(2)</sup>		-40°C to +85°C
Supply Voltage (V <sup>+</sup> – V <sup>-</sup> )		2.7V to 12V
Package Thermal Resistance (θ <sub>JA</sub> ) <sup>(2)</sup>	5-Pin SC70	456°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
- (2) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC board.

### 3V Electrical Characteristics<sup>(1)</sup>

Unless otherwise specified, all limits are specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$ , and  $R_L = 100\text{ k}\Omega$  to  $V^+/2$ . **Boldface limits apply to the temperature range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .**

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$V_{\text{OS}}$	Input Offset Voltage			$\pm 0.2$	$\pm 3$ <b><math>\pm 3.8</math></b>	$\text{mV}$
$\text{TC } V_{\text{OS}}$	Input Offset Voltage Drift	See <sup>(4)</sup>		$\pm 0.3$	<b><math>\pm 15</math></b>	$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current <sup>(5)</sup>	$V_{\text{CM}} = 0.5\text{V}$	$-1000$ <b><math>-1600</math></b>	-320		$\text{pA}$
		$V_{\text{CM}} = 2.5\text{V}$		110	<b>800</b> <b>1900</b>	
$I_{\text{OS}}$	Input Offset Current			$\pm 10$		$\text{pA}$
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}}$ Stepped from $0\text{V}$ to $1.5\text{V}$	<b>77</b> <b>70</b>	100		$\text{dB}$
		$V_{\text{CM}}$ Stepped from $2.4\text{V}$ to $3\text{V}$	<b>75</b> <b>68</b>	115		
		$V_{\text{CM}}$ Stepped from $0.5\text{V}$ to $2.5\text{V}$	<b>60</b> <b>56</b>	80		
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7\text{V}$ to $5\text{V}$ , $V_{\text{CM}} = 0.5\text{V}$	<b>72</b> <b>68</b>	114		$\text{dB}$
		$V^+ = 3\text{V}$ to $5\text{V}$ , $V_{\text{CM}} = 0.5\text{V}$	<b>76</b> <b>72</b>	115		
		$V^+ = 5\text{V}$ to $12\text{V}$ , $V_{\text{CM}} = 0.5\text{V}$	<b>84</b> <b>80</b>	117		
CMVR	Input Common-Mode Voltage Range	$\text{CMRR} \geq 50 \text{ dB}$	$-0.1$ <b>0</b>		<b>3.1</b> <b>3.0</b>	$\text{V}$
$A_{\text{VOL}}$	Large Signal Voltage Gain	Sinking, $V_O = 2.5\text{V}$	<b>75</b>	105		$\text{dB}$
		Sourcing, $V_O = 0.5\text{V}$	<b>70</b>			
$V_O$	Output Swing High	$V_{\text{ID}} = 100 \text{ mV}$	<b>2.85</b> <b>2.8</b>	2.90		$\text{V}$
	Output Swing Low	$V_{\text{ID}} = -100 \text{ mV}$		100	<b>150</b> <b>200</b>	$\text{mV}$
$I_{\text{SC}}$	Output Short Circuit Current <sup>(6)</sup>	Sourcing $V_{\text{ID}} = 100 \text{ mV}$		-500	<b>-225</b>	$\mu\text{A}$
		Sinking $V_{\text{ID}} = -100 \text{ mV}$	225	1350		
$I_S$	Supply Current			0.88	<b>1.2</b> <b>1.5</b>	$\mu\text{A}$
SR	Slew Rate <sup>(7)</sup>	$A_V = +1$ , $V_O$ ramps from $0.5\text{V}$ to $2.5\text{V}$	<b>5.25</b> <b>3.10</b>	7.7		$\text{V}/\text{ms}$
GBW	Gain Bandwidth Product	$R_L = 1 \text{ M}\Omega$ , $C_L = 50 \text{ pF}$		27		$\text{kHz}$
	Phase Margin	$R_L = 1 \text{ M}\Omega$ , $C_L = 50 \text{ pF}$		53		$\text{deg}$
$e_n$	Input-Referred Voltage Noise	$f = 100 \text{ Hz}$		320		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 10 \text{ Hz}$		.02		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1 \text{ kHz}$		.01		

- (1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
- (2) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
- (3) Typical values represent the most likely parametric norm at the time of characterization.
- (4) Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in  $V_{\text{OS}}$  at temperature extremes into the total temperature change.
- (5) Positive current corresponds to current flowing into the device.
- (6) The Short Circuit Test is a momentary test. See [Note 4](#) in the Absolute Maximum Ratings Table.
- (7) Slew rate is the average of the rising and falling slew rates.

## 5V Electrical Characteristics<sup>(1)</sup>

Unless otherwise specified, all limits are specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$ , and  $R_L = 100\text{ k}\Omega$  to  $V^+/2$ .  
**Boldface limits apply to the temperature range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .**

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$V_{\text{OS}}$	Input Offset Voltage			$\pm 0.2$	$\pm 3$ <b><math>\pm 3.8</math></b>	$\text{mV}$
$\text{TC } V_{\text{OS}}$	Input Offset Voltage Drift	See <sup>(4)</sup>		$\pm 0.3$	<b><math>\pm 15</math></b>	$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current <sup>(5)</sup>	$V_{\text{CM}} = 0.5\text{V}$	<b>-1000</b> <b>-1600</b>	-320		$\text{pA}$
		$V_{\text{CM}} = 4.5\text{V}$		110	<b>800</b> <b>1900</b>	
$I_{\text{OS}}$	Input Offset Current			$\pm 10$		$\text{pA}$
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}}$ Stepped from 0V to 2.5V	<b>80</b> <b>73</b>	115		$\text{dB}$
		$V_{\text{CM}}$ Stepped from 4.4 to 5V	<b>75</b> <b>68</b>	107		
		$V_{\text{CM}}$ Stepped from 0.5 to 4.5V	<b>65</b> <b>62</b>	87		
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7\text{V}$ to 5V, $V_{\text{CM}} = 0.5\text{V}$	<b>72</b> <b>68</b>	114		$\text{dB}$
		$V^+ = 3\text{V}$ to 5V, $V_{\text{CM}} = 0.5\text{V}$	<b>76</b> <b>72</b>	115		
		$V^+ = 5\text{V}$ to 12V, $V_{\text{CM}} = 0.5\text{V}$	<b>84</b> <b>80</b>	117		
CMVR	Input Common-Mode Voltage Range	$\text{CMRR} \geq 50 \text{ dB}$	<b>-0.1</b> <b>0</b>		<b>5.1</b> <b>5</b>	$\text{V}$
$A_{\text{VOL}}$	Large Signal Voltage Gain	Sinking, $V_O = 4.5\text{V}$	<b>78</b>	110		$\text{dB}$
		Sourcing, $V_O = 0.5\text{V}$	<b>73</b>			
$V_O$	Output Swing High	$V_{\text{ID}} = 100 \text{ mV}$	<b>4.8</b> <b>4.75</b>	4.89		$\text{V}$
	Output Swing Low	$V_{\text{ID}} = -100 \text{ mV}$		110	<b>200</b> <b>250</b>	$\text{mV}$
$I_{\text{SC}}$	Output Short Circuit Current <sup>(6)</sup>	Sourcing to $V^-$ $V_{\text{ID}} = 100 \text{ mV}$		-550	-225	$\mu\text{A}$
		Sinking to $V^+$ $V_{\text{ID}} = -100 \text{ mV}$	225	1350		
$I_S$	Supply Current			0.97	<b>1.2</b> <b>1.5</b>	$\mu\text{A}$
SR	Slew Rate <sup>(7)</sup>	$A_V = +1$ , $V_O$ ramps from 0.5V to 4.5V	<b>5.25</b> <b>3.10</b>	7.5		$\text{V}/\text{ms}$
GBW	Gain Bandwidth Product	$R_L = 1 \text{ M}\Omega$ , $C_L = 50 \text{ pF}$		27		$\text{kHz}$
	Phase Margin	$R_L = 1 \text{ M}\Omega$ , $C_L = 50 \text{ pF}$		53		$\text{deg}$
$e_n$	Input-Referred Voltage Noise	$f = 100 \text{ Hz}$		320		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 10 \text{ Hz}$		.02		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1 \text{ kHz}$		.01		

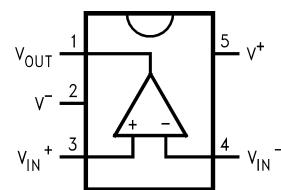
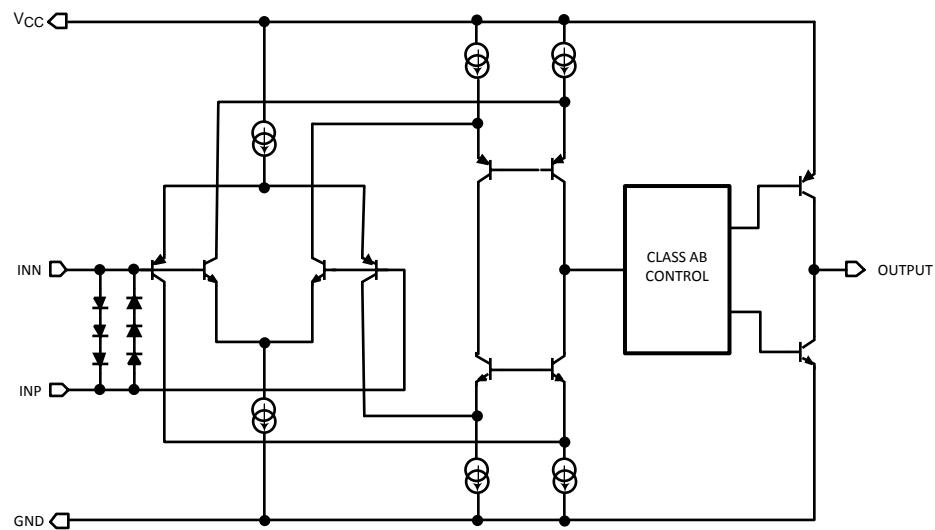
- (1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
- (2) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
- (3) Typical values represent the most likely parametric norm at the time of characterization.
- (4) Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in  $V_{\text{OS}}$  at temperature extremes into the total temperature change.
- (5) Positive current corresponds to current flowing into the device.
- (6) The Short Circuit Test is a momentary test. See Note 4 in the Absolute Maximum Ratings Table.
- (7) Slew rate is the average of the rising and falling slew rates.

## 12V Electrical Characteristics <sup>(1)</sup>

Unless otherwise specified, all limits are specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 12\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V_O = V^+/2$ , and  $R_L = 100\text{ k}\Omega$  to  $V^+/2$ . **Boldface limits apply to the temperature range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .**

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$V_{OS}$	Input Offset Voltage			$\pm 0.2$	$\pm 3$ <b><math>\pm 3.8</math></b>	$\text{mV}$
$\text{TC } V_{OS}$	Input Offset Voltage Drift	See <sup>(4)</sup>		$\pm 0.3$	<b><math>\pm 15</math></b>	$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current <sup>(5)</sup>	$V_{CM} = 0.5\text{V}$	<b>-1000</b> <b>-1600</b>	-320		$\text{pA}$
		$V_{CM} = 11.5\text{V}$		110	<b>800</b> <b>1900</b>	
$I_{OS}$	Input Offset Current			$\pm 10$		$\text{pA}$
CMRR	Common Mode Rejection Ratio	$V_{CM}$ Stepped from $0\text{V}$ to $+6\text{V}$	<b>75</b> <b>70</b>	115		$\text{dB}$
		$V_{CM}$ Stepped from $11.4\text{V}$ to $12\text{V}$	<b>75</b> <b>68</b>	110		
		$V_{CM}$ Stepped from $0.5\text{V}$ to $11.5$	<b>70</b> <b>65</b>	97		
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7\text{V}$ to $5\text{V}$ , $V_{CM} = 0.5\text{V}$	<b>72</b> <b>68</b>	114		$\text{dB}$
		$V^+ = 3\text{V}$ to $5\text{V}$ , $V_{CM} = 0.5\text{V}$	<b>76</b> <b>72</b>	115		
		$V^+ = 5\text{V}$ to $12\text{V}$ , $V_{CM} = 0.5\text{V}$	<b>84</b> <b>80</b>	117		
CMVR	Input Common-Mode Voltage Range	$\text{CMRR} \geq 50\text{ dB}$	<b>-0.1</b> <b>0</b>		<b>12.1</b> <b>12</b>	$\text{V}$
$A_{VOL}$	Large Signal Voltage Gain	Sinking, $V_O = 0.5\text{V}$	<b>89</b>			$\text{dB}$
		Sourcing, $V_O = 11.5\text{V}$	<b>84</b>	110		
$V_O$	Output Swing High	$V_{ID} = 100\text{ mV}$	<b>11.8</b> <b>11.72</b>	11.85		$\text{V}$
	Output Swing Low	$V_{ID} = -100\text{ mV}$		150	<b>200</b> <b>280</b>	$\text{mV}$
$I_{SC}$	Output Short Circuit Current <sup>(6)</sup>	Sourcing $V_{ID} = 100\text{ mV}$		-650	-200	$\mu\text{A}$
		Sinking $V_{ID} = -100\text{ mV}$	200	1300		
$I_S$	Supply Current			1.2	<b>1.75</b> <b>2.5</b>	$\mu\text{A}$
SR	Slew Rate <sup>(7)</sup>	$A_V = +1$ , $V_O$ ramped from $1\text{V}$ to $11\text{V}$	<b>5.25</b> <b>3.10</b>	7.0		$\text{V}/\text{ms}$
GBW	Gain Bandwidth Product	$R_L = 1\text{ M}\Omega$ , $C_L = 50\text{ pF}$		25		$\text{kHz}$
	Phase Margin	$R_L = 1\text{ M}\Omega$ , $C_L = 50\text{ pF}$		52		$\text{deg}$
$e_n$	Input-Referred Voltage Noise	$f = 100\text{ Hz}$		320		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 10\text{ Hz}$		.02		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		.01		

- (1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
- (2) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
- (3) Typical values represent the most likely parametric norm at the time of characterization.
- (4) Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in  $V_{OS}$  at temperature extremes into the total temperature change.
- (5) Positive current corresponds to current flowing into the device.
- (6) The Short Circuit Test is a momentary test. See [Note 4](#) in the Absolute Maximum Ratings Table.
- (7) Slew rate is the average of the rising and falling slew rates.

**Connection Diagram****Figure 2. SC70-5  
Top View****Simplified Schematic**

### Typical Performance Characteristics

At  $T_J = 25^\circ\text{C}$ , unless otherwise specified.

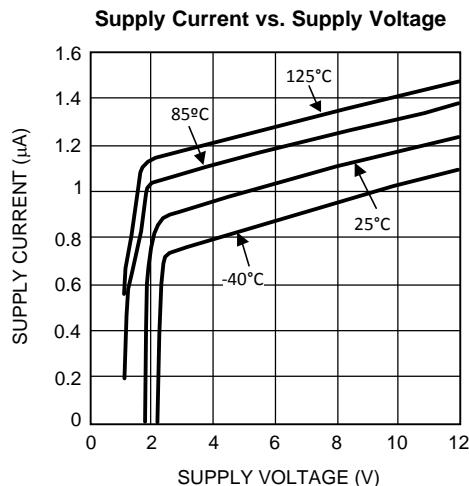


Figure 3.

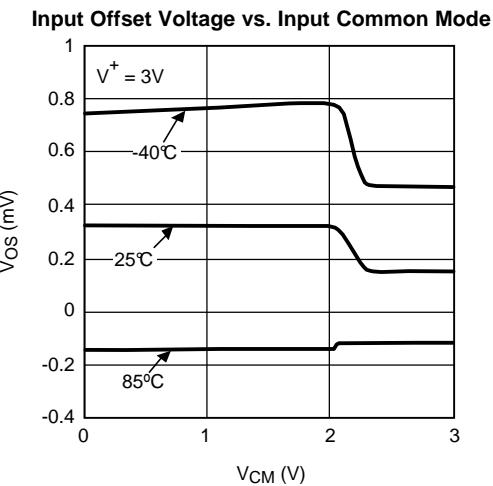


Figure 4.

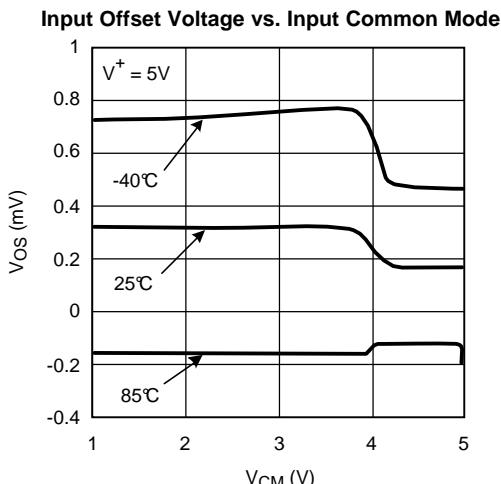


Figure 5.

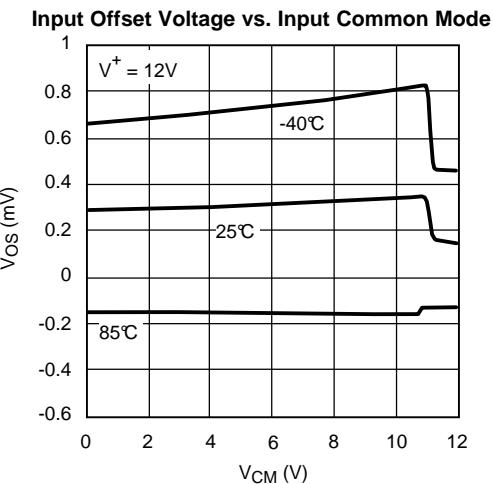


Figure 6.

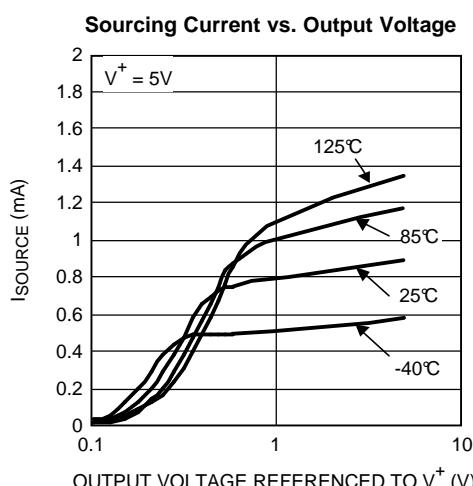


Figure 7.

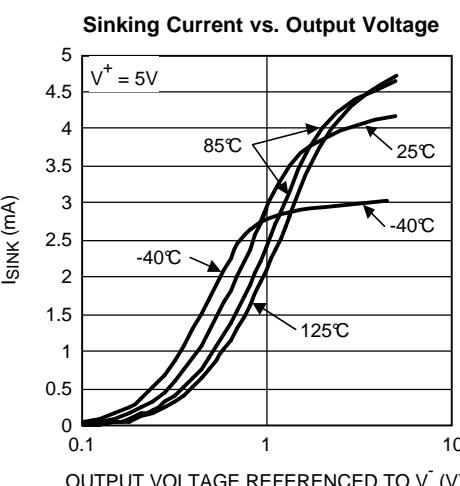


Figure 8.

### Typical Performance Characteristics (continued)

At  $T_J = 25^\circ\text{C}$ , unless otherwise specified.

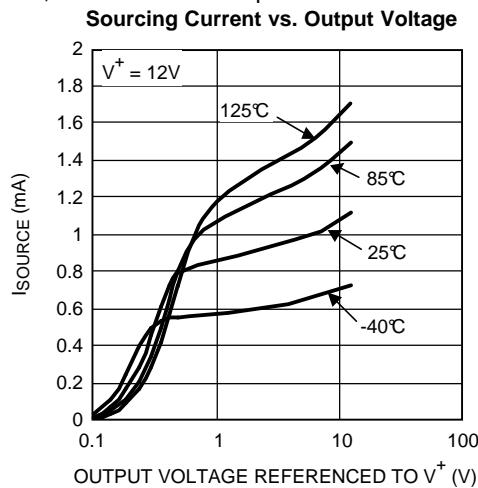


Figure 9.

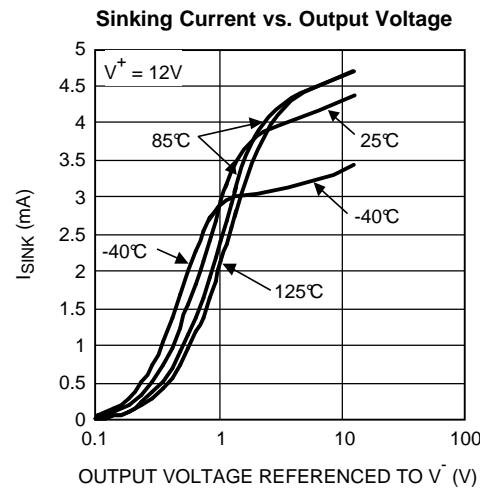


Figure 10.

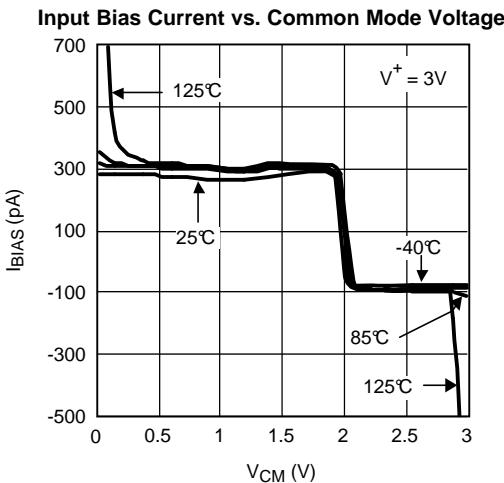


Figure 11.

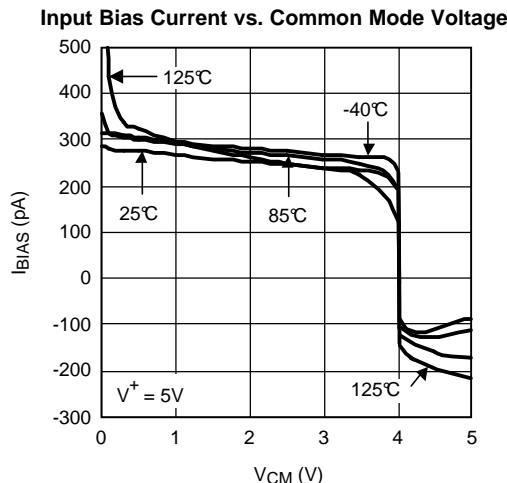


Figure 12.

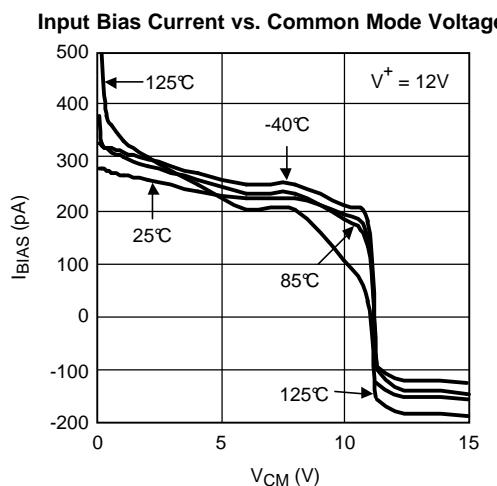


Figure 13.

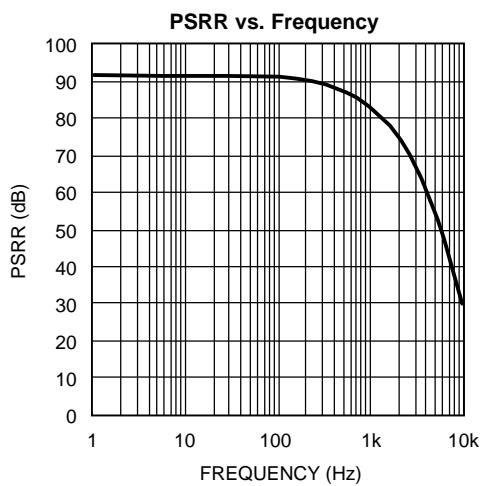
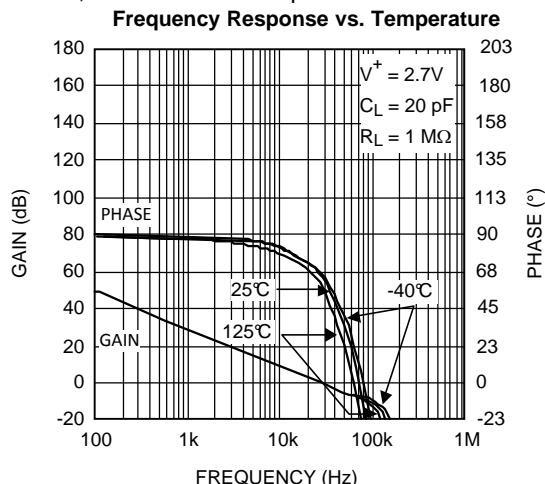


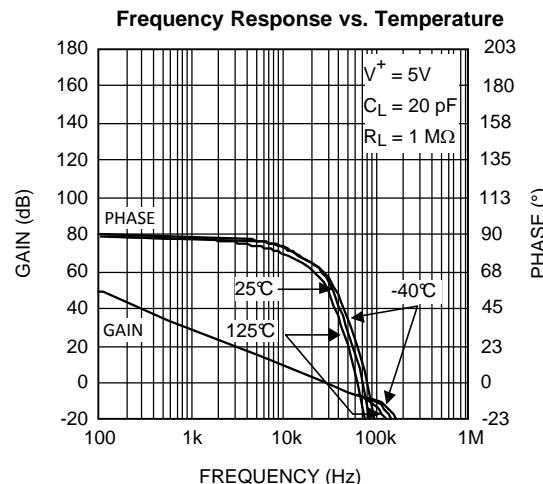
Figure 14.

### Typical Performance Characteristics (continued)

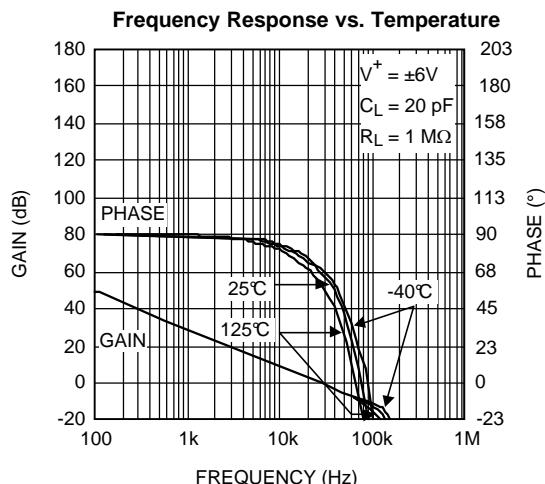
At  $T_J = 25^\circ\text{C}$ , unless otherwise specified.



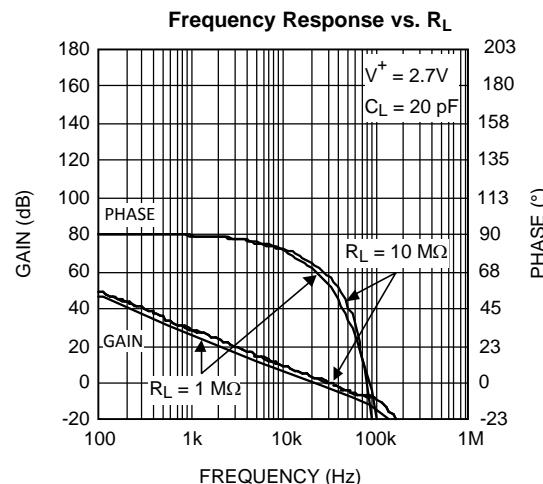
**Figure 15.**



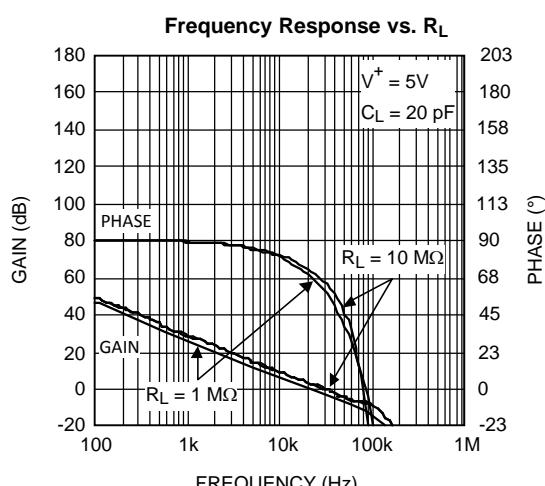
**Figure 16.**



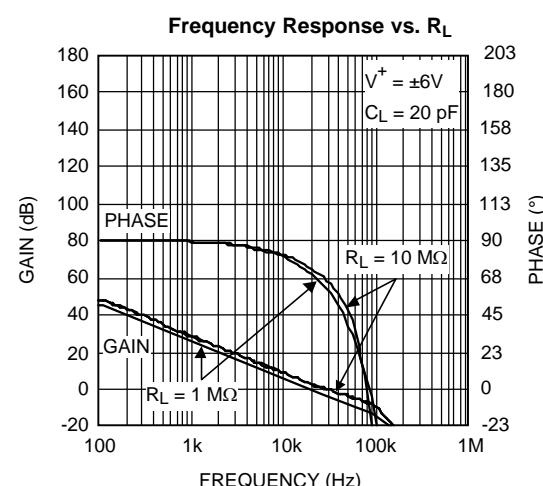
**Figure 17.**



**Figure 18.**



**Figure 19.**



**Figure 20.**

### Typical Performance Characteristics (continued)

At  $T_J = 25^\circ\text{C}$ , unless otherwise specified.

Frequency Response vs.  $C_L$

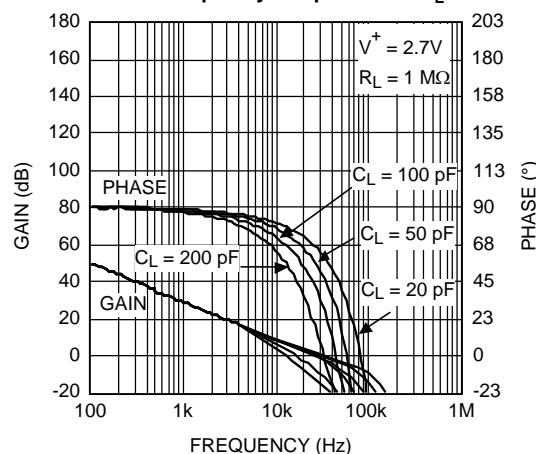


Figure 21.

Frequency Response vs.  $C_L$

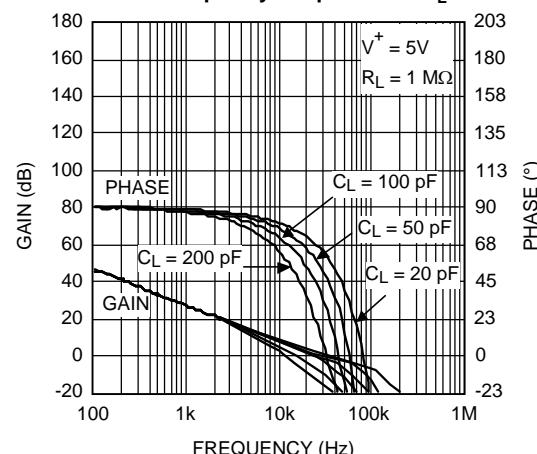


Figure 22.

Frequency Response vs.  $C_L$

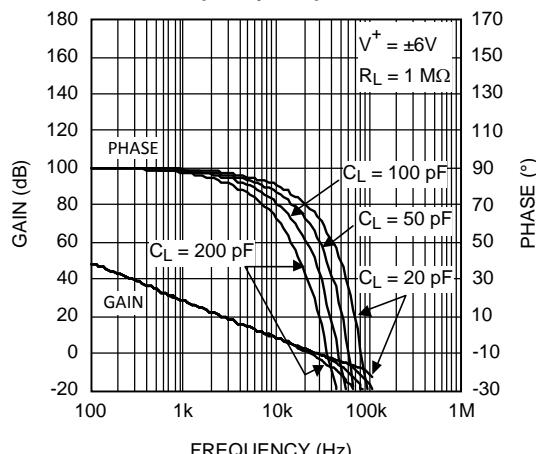


Figure 23.

Voltage Noise vs. Frequency

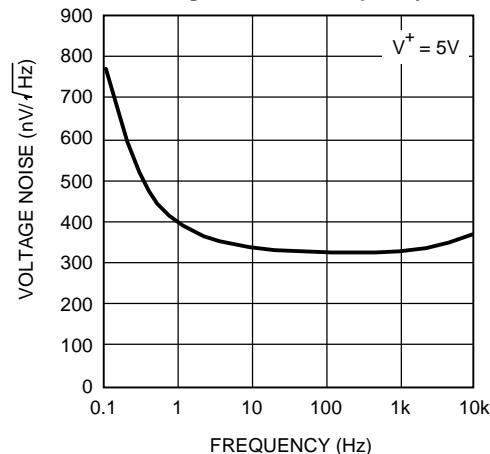


Figure 24.

Non-Inverting Small Signal Pulse Response

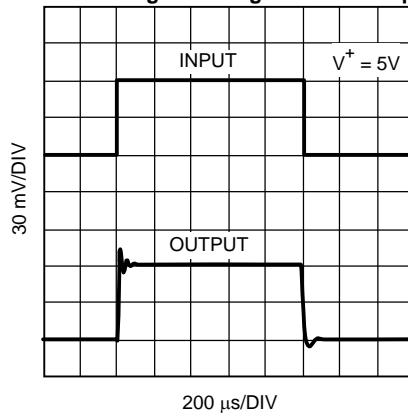


Figure 25.

Non-Inverting Large Signal Pulse Response

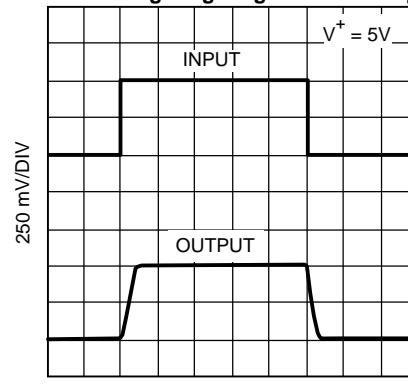
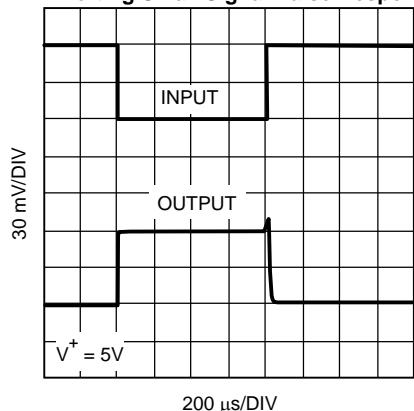


Figure 26.

### Typical Performance Characteristics (continued)

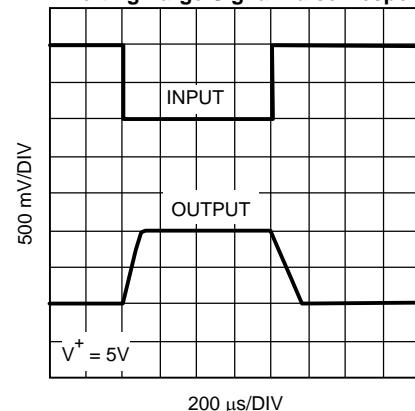
At  $T_J = 25^\circ\text{C}$ , unless otherwise specified.

#### Inverting Small Signal Pulse Response



**Figure 27.**

#### Inverting Large Signal Pulse Response



**Figure 28.**

## APPLICATION NOTES

The LPV511 is fabricated with Texas Instrument's state-of-the-art VIP50C process.

### INPUT STAGE

The LPV511 has a rail-to-rail input which provides more flexibility for the system designer. As can be seen from the simplified schematic, rail-to-rail input is achieved by using in parallel, one PNP differential pair and one NPN differential pair. When the common mode input voltage ( $V_{CM}$ ) is near  $V^+$ , the NPN pair is on and the PNP pair is off. When  $V_{CM}$  is near  $V^-$ , the NPN pair is off and the PNP pair is on. When  $V_{CM}$  is between  $V^+$  and  $V^-$ , internal logic decides how much current each differential pair will get. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

Because both input stages have their own offset voltage ( $V_{OS}$ ) characteristic, the offset voltage of the LPV511 becomes a function of  $V_{CM}$ .  $V_{OS}$  has a crossover point at 1.0V below  $V^+$ . Refer to the ' $V_{OS}$  vs.  $V_{CM}$ ' curve in the [Typical Performance Characteristics](#) section. Caution should be taken in situations where the input signal amplitude is comparable to the  $V_{OS}$  value and/or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point.

The input bias current,  $I_B$  will change in value and polarity as the input crosses the transition region. In addition, parameters such as PSRR and CMRR which involve the input offset voltage will also be affected by changes in  $V_{CM}$  across the differential pair transition region.

Differential input voltage is the difference in voltage between the non-inverting (+) input and the inverting input (-) of the op amp. Due to the three series diodes across the two inputs, the absolute maximum differential input voltage is  $\pm 2.1V$ . This may not be a problem to most conventional op amp designs; however, designers should avoid using the LPV511 as a comparator.

### OUTPUT STAGE

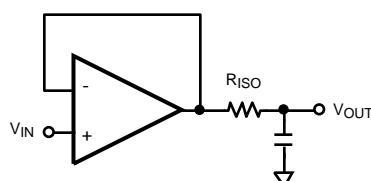
The LPV511 output voltage swing 100 mV from rails @ 3V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV511 Maximum Output Voltage Swing defines the maximum swing possible under a particular output load. The LPV511 output swings 110 mV from the rail @ 5V supply with an output load of 100 k $\Omega$ .

### DRIVING CAPACITIVE LOAD

The LPV511 is internally compensated for stable unity gain operation, with a 27 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of the op amp. When the output is required to drive a large capacitive load, greater than 100 pF, a small series resistor at the output of the amplifier improves the phase margin (see [Figure 29](#)).

In [Figure 29](#), the isolation resistor  $R_{ISO}$  and the load capacitor  $C_L$  form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of  $R_{ISO}$ . The bigger the  $R_{ISO}$  resistor value, the more stable  $V_{OUT}$  will be. But the DC accuracy is degraded when the  $R_{ISO}$  gets bigger. If there were a load resistor in [Figure 29](#), the output voltage would be divided by  $R_{ISO}$  and the load resistor.



**Figure 29. Resistive Isolation of Capacitive Load**

## POWER SUPPLIES AND LAYOUT

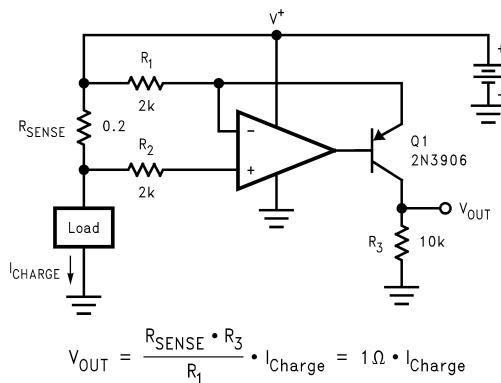
The LPV511 operates from a single 2.7V to 12V power supply. It is recommended to bypass the power supplies with a 0.1  $\mu$ F ceramic capacitor placed close to the V<sup>+</sup> and V<sup>-</sup> pins.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the op amp's inputs and outputs. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components close to the op amps's pins.

## Typical Applications

### BATTERY CURRENT SENSING

The rail-to-rail common mode input range and the very low quiescent current make the LPV511 ideal to use in high side and low side battery current sensing applications. The high side current sensing circuit in [Figure 30](#) is commonly used in a battery charger to monitor the charging current in order to prevent over charging. A sense resistor R<sub>SENSE</sub> is connected to the battery directly.



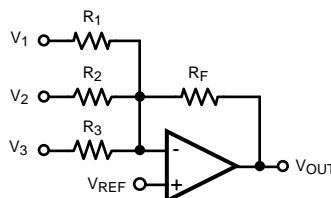
**Figure 30. High Side Current Sensing**

### SUMMING AMPLIFIER

The LPV511 operational amplifier is a perfect fit in a summing amplifier circuit because of the rail-to-rail input and output and the sub-micro Amp quiescent current. In this configuration, the amplifier outputs the sum of the three input voltages.

The ratio of the sum and the output voltage is defined using feedback and input resistors.

$$V_{OUT} = R_F \left( \frac{V_{REF} - V_1}{R_1} + \frac{V_{REF} - V_2}{R_2} + \frac{V_{REF} - V_3}{R_3} \right) + V_{REF} \quad (1)$$



**Figure 31. Summing Amplifier Circuit**

## REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format .....	13

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV511MG	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	A91	
LPV511MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A91	Samples
LPV511MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A91	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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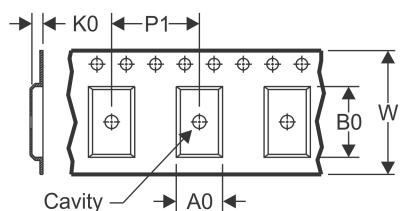
1-Nov-2013

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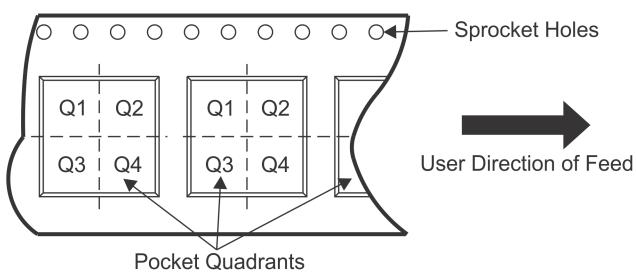
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV511MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV511MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV511MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

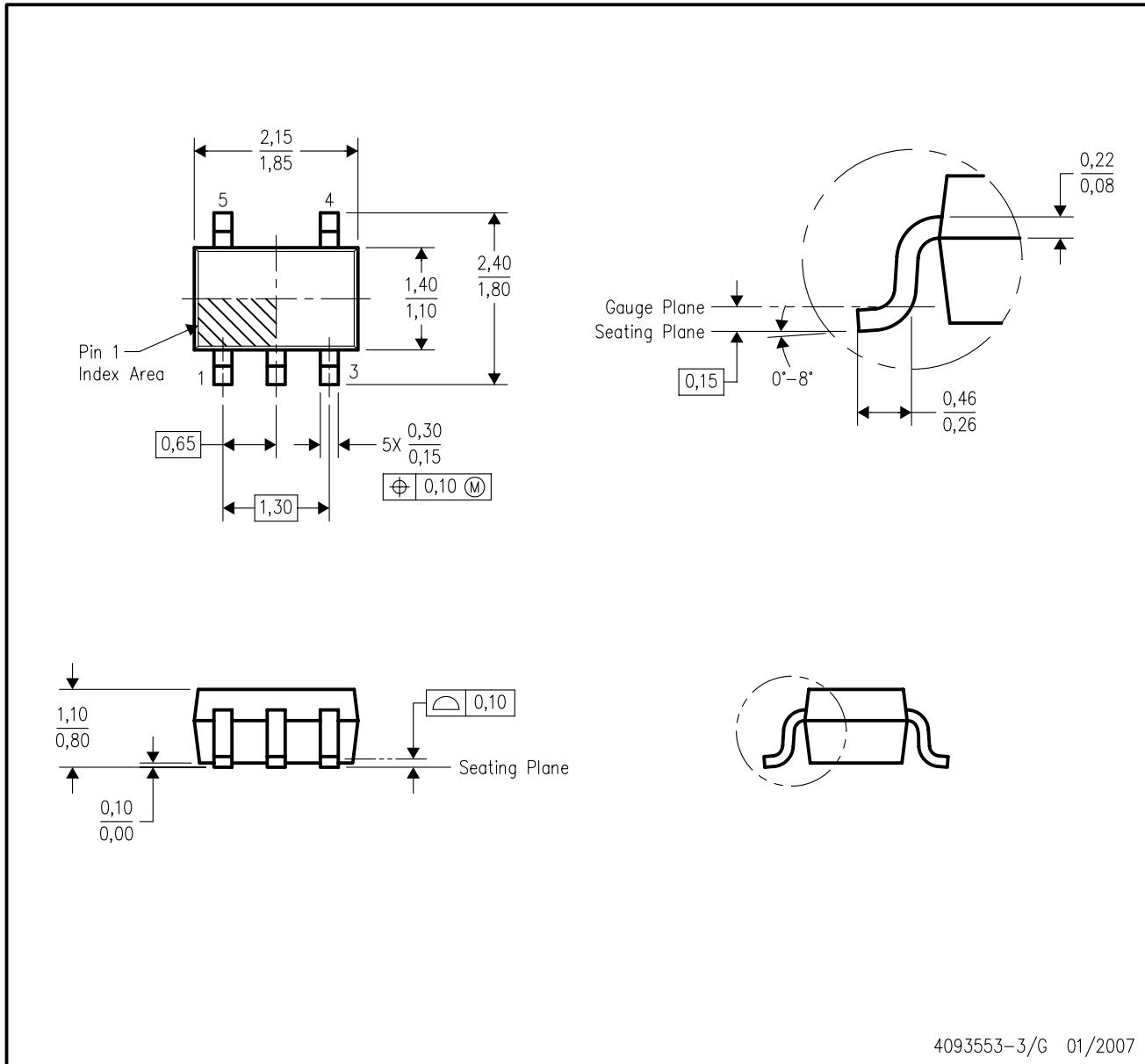
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV511MG	SC70	DCK	5	1000	210.0	185.0	35.0
LPV511MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LPV511MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AA.

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